The SPICE Handbook of 50 Basic Circuits

Steven M. Sandler and Analytical Engineering, Inc.

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Introduction

Since the introduction of SPICE in 1971, the simulation program has become one of the most popular analog simulation tools. In the last 10 years, we have seen explosive growth of SPICE, with the addition of SPICE 3 syntax, providing support for mixed mode simulation [Kielkowski, 1994]. We have also seen many new companies emerge as manufacturer's of SPICE simulation software, most of which is currently available for the PC platform.

Each vender of SPICE simulation software has added features, such as Monte Carlo functions, Schematic editor and Post Graphic processing, as well as substantial component libraries. In some cases, the manufacturers have modified the algorithms for controlling convergence and have added new parameters or syntax for component models.

We have also seen component manufacturer's providing their support. Many component manufacturer's provide models of components such as Mosfet's, transistors, Operational Amplifiers. Most of these models are available, free, via Internet Web sites.

The abilities of computers to model electronic circuits are increasing every day. The often quoted "Moore's Law" states that the speed of microprocessors doubles nearly every 18 months. As computers are becoming more powerful and more capable, computer simulation can become a more important tool in the design process.

Unfortunately, there is an unwillingness in the electronic design community to embrace the abilities of computers to model circuits. Many engineers still think of SPICE (Simulation Program of Integrated Circuit Electronics) simulation as a toy. The typical attitude of the design engineer, upon being shown a SPICE model of the impeding failure of his/her circuit will reply, "That's nice, but lets see what the hardware does." Even when the hardware fails, the engineer is more likely to investigate the charred and smoking breadboard than the SPICE model that predicted the result.

The purpose of this book is to show the abilities of SPICE and equivalent circuit simulation tools to accurately predict the behavior of electronic hardware circuitry. The emphasis of this book is on how well the simulation stacks up against real measured hardware. The uses of circuit simulation are well documented (Sandler 1996).

The speed a simulation can be performed is orders of magnitude faster than building the circuit on a lab breadboard.

The simulation can be run through any number of environments with ease.

Circuit tolerances and the effect on the operation of the functionality of the circuit can be easily evaluated.

There are still limitations to the capabilities of SPICE and similar circuit simulators. While the sophistication of simulation increases, the lab breadboard will still remain a necessary step in the design process. This book will aid the engineer in using SPICE simulation as a very powerful **tool** in the design process.

Simply, this book is a compilation of all manners of electronic circuits. Such compilations are not unusual, in fact, there are several excellent circuit encyclopedias on bookshelves. However, this book goes one step further. Instead of simply presenting the circuit to the reader, a SPICE schematic and the equivalent hardware performance is also provided, along with an explanation of the intricacies of the development of an accurate SPICE model for the circuit in question. This format benefits the reader in numerous ways. The reader can emulate the correlation techniques introduced in this book in order to make their own specific SPICE models accurately mimic the behavior of their hardware.

SPICE as a tool can give the design engineer a vast array of data that can ensure a successful and optimal design for their hardware. The designer has a hardware design that they know operates correctly, and they also have a SPICE model that can accurately reflect that designs behavior at the click of a mouse button. Clearly, SPICE modeling can be a much more integral step in the design process and prove its worth to engineers of any circuit discipline.

The book is structured intuitively, minimizing searching time and maximizing efficiency. The beginning of the book concentrates on the basics of computer simulation of circuits. An overview of the three most popular SPICE programs are provided, along with their differences and peculiarities.

We have selected a broad cross section of analog and mixed mode designs, which we have simulated as well as constructed. The circuits are grouped into logical chapters. Generic topics such as oscillators, amplifiers/receivers, power converters, filters, etc. all head their own chapter. Each chapter starts with a brief overview of the function of the circuits in that chapter. This is followed by each design type featured in this book that performs that function. For example, in the chapter on Reference Circuits, the beginning of the chapter details what reference circuits are and their uses in the system level. This is followed by a detailed discussion on a single type of reference circuit, the band gap reference.

Each circuit has a discussion of the theory of operation, followed by the SPICE model schematic, the simulation results, and a comparison to laboratory data. Advantages and disadvantages to each circuit are added, along with any tips or hints used to model the circuit accurately. We have attempted to perform each simulation using several manufacturer's versions of SPICE for comparison. Also included are the simulation run times for each circuit.

Three simulation programs were used to simulate the circuits in this book. IsSpice v7.6© , Pspice Evaluation v6.3© , and Micro-Cap V v2.0© .

The simulations in this book were computed using three PC desktop computers. The computers utilized 133 Mhz Intel© Microprocessors, 48 Meg RAM, and Windows NT 4.0© . The computers were connected to a

local network of six computers. The run times of the circuits are dependant on the capabilities of the computers running them as well as the .OPTIONS statements in the simulation. This being said, the simulation times noted after the simulations are **reasonably** accurate. Don't expect your computer will run at these times. Any simulation software can be made to run faster or slower than any other software! Just by changing the .OPTIONS statements, simulations have been shown to run 14 times faster [Sandler, 1996]. Each circuit can be optimized for speed differently. Tricks that speed up simulations in one circuit may not work in another, or even have the opposite effect on speed. SPICE simulations are a trade off between simulation speed, accuracy, and convergence [Kielkowski, 1994]. We have made a reasonable effort to make an apples to apples comparison between the simulation speeds of the software in this book. The reader will notice that it is not predictable which software package will run the fastest on any single circuit. The real purpose of including the run times is to provide the user with a guess as to how long the circuit will take to simulate on their own computer, nothing more.

The reader will also note that in some circumstances, one or more of the simulation software results will not match with the hardware results. We have attempted to explain the reasons for this in each of the circuits where this occurs. Bear in mind, SPICE is one of those tasks in life where you get out of it what you put into it. If you put very little effort into understanding what the model or circuit is doing, chances are your simulation accuracy will reflect that.

The CD ROM contains three folders, one for each of the three simulators. Each folder contains the .CIR files of that particular simulator. The circuit names are provided in the document for that circuit. For example, Circuit #1, a 4^{th} Order Butterworth Low Pass Filter list the file names for that circuit as: lp_fltr (Ispice), lpflt (Micro-Cap), lp_flt (Pspice).

The schematics for most of the circuits contained in this book can be entered into the simulator in several minutes. The .CIR files can be cut and paste into the text editor and ran, or more importantly, the simulation control parameters can be viewed.

The options useful in helping to resolve non-convergence issues.

We have put a great deal of effort into the construction of this book. It is our sincere hope that the reader benefits from our hard work.

References

Kielkowski, Ron M. 1994. Inside Spice. New York: McGraw Hill.

Sandler, Steven M. SMPS simulation with SPICE. 1996. McGraw Hill.

2
Description of Ispice, Pspice, and Micro-Cap Simulators

The development of SPICE was instigated by Ron Rohrer, a junior faculty member at the University of California, Berkely. Rohrer was teaching a class on circuit simulation, in which he and Larry Nagel developed a simulator, in FORTRAN source code, that was to be named CANCER (Computer Analysis of Nonlinear Circuits Excluding Radiation). Due to the difficulties in testing circuits of the small sizes of IC's, SPICE was thought to be an answer to the quick and reliable design of integrated circuits. Larry Nagel increased the capabilities of CANCER by increasing the 400 component/or 100 node limit, adding new and improved components, and macromodels. In 1971, Nagel released this improved version of CANCER as SPICE1 (Simulation Program with Integrated Circuit Emphasis). In 1975 SPICE2 was released, which offered equation formulation for voltage defined elements as well as increased simulation speed. This was achieved through the developments of timestep control algorithms. Eventually, the capabilities of SPICE grew with the capabilities of computers. In 1983, SPICE2G.6 was released, which has become the cornerstone of many vendor-offered versions of SPICE compatible circuit simulation programs. SPICE2G.6 has been the industry standard for many years. Motivated by the increased use of UNIX workstations, SPICE2 was converted into C source code and released as SPICE3. Although SPICE3 is not backwards compatible with SPICE2, the new features far out weigh this drawback. SPICE3 has a technical advantage of being readily modified because it is written in modular C code. SPICE3 also offers more and improved device models and analysis. A major advantage is the addition of a graphical post processor, which graphically presents and facilitates waveform computation of simulation results. As SPICE3 provides more of the features offered in SPICE2G.6, it becomes a more viable replacement of SPICE2G.6. [Kielkowski]

Understanding the development of SPICE is useful in making a worthwhile comparison of vendor-offered simulation software. The foundation of many vender-offered simulators is Berkely SPICE3F.5. This is the simulator engine that dictates the algorithms used to generate a solution for a given simulation.

Three of these software manufacturers: Microsim (Pspice), Intusoft (IsSpice), and Micro-Cap V (Microcap) have their products featured in this book. These software manufacturers took the Berkley core program SPICE3F.5 and created a shell program around it. The shell creates the

schematic using a sophisticated set of CAD tools. The shell then translates the schematic into the language of SPICE. The circuit is processed by SPICE and an answer is generated. The shell then takes the result from SPICE and passes it into a graphics post processor in order to view the answer in a meaningful form.

Because of this symbiotic relationship between the core SPICE program and the shell, each of the three programs have roughly the same structure. Four separate modules are utilized.

The first module is the **schematic capture** program. Originally, using SPICE meant translating a schematic by hand into the SPICE programming language for calculation. The schematic capture program allows the user to pull down parts from a menu, wire the components using a mouse, and click a button to start the simulation. The abilities of the schematic capture program are beginning to approach those of true CAD programs, indeed, Pspice offers a tool for routing printed circuit boards. The schematic building feel of the schematic capture programs helps the SPICE user to quickly translate their circuit ideas into a schematic compatible with SPICE.

A **text editor** is also included with the shell packages. The text editor is invaluable for viewing the text generated output files of SPICE as well as investigating syntax errors and other subtleties of the SPICE programming language. The text output of SPICE is in an excellent format for exporting to other useful engineering tools such as Excel or Mathcad.

The third module is the **simulator** itself. As stated earlier, each of these programs use the core code from Berkely to iterate solutions of the circuit using mesh equations.

The fourth module is the **graphics post processor**. This module has the feel of an oscilloscope, with the output of the SPICE program being translated into waveforms that fit the user's idea of how the circuit should behave. Many different mathematical operations can be performed on these waveforms, making the most use out of the results of SPICE.

Schematic Capture	Text Editor	Simulator	Graphical Post Processor
Allows users to quickly generate SPICE compatable program graphically Allows for the construction of symbols used for generating new circuit models for components and for IC's.	Examine output files from SPICE Examine SPICE code generated by Schematic Capture program	Performs numerical iteration of circuit to determine solutions	Converts output of Simulator into more meaningful graphs and waveforms Has the ability to perform complex numerical calculations on waveforms

Table 2-1: The four Modules and their functions

A difference between these simulators is how the user interfaces with the simulator engine, and the features offered by the other modules of the individual vendor program. A user can create libraries, but most of the time will depend on the libraries that are provided by a vendor.

Libraries are a distinguishing characteristic of a simulator. Libraries may be included or libraries can be purchased that are compatible with the simulator. The libraries of each of the three simulators are unique to that particular simulator. However, in many cases a bulk of the models in the library have been provided by the component manufacturer. These models are available free over the internet. The library governs the accuracy of the simulation in which they are used. It is very important to test and qualify models in a library, rather than assuming that they are accurate. Just because a model is in a library does not mean that it provides correct results.

Each of the three simulators have a schematic editor program, which is used to enter the circuit into the simulator. Accessing the overall quality of a particular schematic editor comes down to preferences. Even though an assessment may be made by the number of keystrokes or clicks of the mouse required to enter a circuit, a users effectiveness is a function of familiarity and comfort. Maximizing the performance of a schematic editor is dependant on the user and is difficult to determine.

The same can be said when evaluating the performance of the post processor of a simulator. Familiarity governs the ability of a user to manipulate the output data into a desirable viewing form. All of the post processors perform similar features and therefore accessing the performance of a particular post processor is inherent to the preferences of the user.

Basic Overview of SPICE

SPICE starts by making an initial guess at the circuits node voltages, and then using nodal equations of the circuit, calculates the mesh currents. The mesh currents are then used to recalculate the node voltages and the cycle begins. This iterative process continues until the nodal equations have been solved within specified limits. These limits can be set by using .OPTION parameters (Reltol, Vntol, and Abstol). As the difference between each iteration approaches zero, the simulation approaches convergence. SPICE uses the Newton-Raphson algorithm to solve the matrix of nodal equations if the circuit contains a nonlinear device. For a circuit containing only linear devices, SPICE use Gaussian elimination to solve the matrix.

SPICE Syntax and Tutorial

The first line of any SPICE text program is the title of the program. This line is completely ignored by SPICE. The next few lines of code usually tell SPICE which analysis will be performed and what the bounds of that analysis will be. For example, we may be requesting a time domain analysis of a circuit (called a transient analysis). The information as to how long, what increments, and what section of the waveform is of interest is defined in this section of the code. Also defined here are global constants, subcircuits (models) used repeatedly in the main circuit, and instructions on which nodes are of interest in the final solution.

```
*EXAMPLE CIRCUIT #1

.TRAN 1U 100U 10U 2U UIC

.OPTIONS METHOD=GEAR

.PRINT TRAN V(2)

.IC V(7)=12
```

Table 2-2: Typical lines of the beginning of a SPICE program

The middle section of the code defines the circuit itself. The structure of each component is roughly similar. The first variable is the reference designator. The next variables are the node numbers that the component is connected to. The remaining variables define the parameters of that component.

A simple example is a resistor:

```
R1 1 2 100K
```

In this line, a resistor with name R1 is defined, connected from node 1 to node 2 with a value of 100 Kohms. Several rules apply to defining components. The node number zero is reserved for ground. All circuits must have at least one ground connection. Also, reference designators are limited to alpha-numeric characters. Longer statements may be continued on the following line by using a + symbol as the first character to indicate a continuation from the previous line.

```
R1 1 0 100K

+ L1 1 2 10U
```

```
Q1 2 3 4 2N2222A

V_INPUT 4 0 10

I_OUT 3 0 PULSE 0 1 1U 100N 100N 10U 20U
```

Table 2-3: Typical lines of the middle of a SPICE program

The final line of any SPICE program must be the **.END** statement.

There are several basic analysis that are primarily used in the this book. An explanation of each is given in the following paragraphs. To modify the simulation controls in Micro-Cap V simply select the options button on the tool bar and select global settings. In Pspice click on the analysis button on the tool bar, select set up, and then choose options. In Ispice Click on the file button on the tool bar, select edit controls, at this point you can write your own .OPTIONS statement, or select the help button in the edit controls box and then click on options for help in selecting a .OPTIONS statement.

DC Analysis

Before SPICE performs any specified simulation, a DC operating point analysis, .OP, is performed. This establishes the DC bias point of the circuit. There must be convergence of this simulation before any other specified simulation can be performed. SPICE calculates the DC operating point by replacing all of the inductors with shorts, and all of the capacitors are open circuit. SPICE must determine the DC operating point within a specified number of iterations, otherwise a nonconvergence warning is generated, and the simulation is aborted. The default .OPTIONS statement used to determine the DC iteration limit is:

```
.OPTIONS ITL1=100
```

For nonconvergence, the value of ITL1 should be increased to greater than 500, which increases the maximum allowed number of iterations to determine the solution.

A . NODESET statement can also be used to reduce the number of iterations required for convergence. The DC voltage of a node can be specified by the user, and will be used by SPICE in the initial guess of the simulation. This can greatly reduce the number of iterations that are required for convergence.

If convergence is not attained through the use of a nodeset and increasing the ITL1 statement, then an ITL6 statement can be used. By setting ITL6=100, or any non-zero value, a source stepping algorithm is used, which decrements the voltages sources down to zero, or until convergence is reached and then they are stepped back up to their assigned voltage level. This appears to be the solution to all DC bias point convergence problems. However, there are bugs associated with the ITL6 function and should be used only as a last resort.

If the circuit contains semiconductor devices, then the circuit contains regions of zero conductance. This can result in a divide by zero error. To eliminate this problem, every PN junction in every SPICE semiconductor device has a GMIN transconductance in parallel with every PN junction. GMIN is assigned globally and has a default value of 100pmhos. The larger the value of GMIN, the faster the Newton-Raphson algorithm will converge to a solution. Raising GMIN decreases the size of the shunt resistor. The accuracy of the simulation is not effected as along as the current generated in the shunt resistors are lower than the relative error tolerance current resolution. [Kielkowski] A suggested value for setting GMIN is given in the following statement:

.OPTIONS GMIN=1n or 1u

Transient Analysis

A transient time domain analysis begins with a DC operating point analysis. SPICE calculates the DC operating point by replacing all of the inductors with shorts, and all of the capacitors are open circuit. SPICE must determine the DC operating point within a specified number of iterations, otherwise a nonconvergence warning is generated, and the simulation is aborted. The solution to the DC operating point determines the node voltages at the time T=0. SPICE then assigns the instantaneous I-V relationship of inductors or capacitors and uses a numeric integration routine to create and equivalent nodal matrix. The nodal matrix changes for every time step in the transient analysis. Each following Newton-Raphson iteration starts with an initial guess consisting of the previous set of node voltages. This expedites the iterative process, which continues until the solution is found or the maximum allowed iterations is exceeded. The maximum number of iterations is determined by the setting .OPTIONS statement ITL4. The default .OPTIONS statement is given below:

.OPTIONS ITL4=10

When the simulation steps to the next point in time, the transient solver determines the operating point at that moment in time. If the simulation does not reach convergence at this point in time, then the time step is reduced by one eighth. This is repeated until convergence is achieved or the maximum number of times that the time step can be reduced, which is specified by ITL4 is reached. A large time step, which is also user defined, in a transient simulation can result in convergence difficulties. This is particularly true for switching circuits. The time step must be small enough to provide enough resolution to identify switching voltage levels. Large voltage transitions, or device model discontinuities must be taken into account when assigning the transient simulation parameters. An Example of a transient simulation statement is given below:

.Tran Tstep Tstop Tstop Tmax UIC

.Tran 10u 10m 0 20u UIC

The Time step Tstep=10u determines each point in time starting from zero that the transient solver will calculate a solution. A safe estimation of the time step is an order of magnitude less than the period of a switching waveform. For example, when selecting the time step for a 100KHz oscillator (period=10usec), the time step should be approximately 1usec. Tmax, the maximum time step can be left out (at default), or specified to increase (decrease TMAX), or decrease (increase TMAX) simulation accuracy. This allows the simulator to take larger steps when the voltage levels in the circuit experience little change. A transient time domain analysis can prove to be the most difficult to get to converge.

AC Analysis

An AC analysis begins by determining the DC bias point of the circuit.

This can be critical, because it determines the state of the active devices. For instance, the output of a linear regulator or operational amplifier is different if it is operating in the linear region, or if it is operating in the saturated region. After SPICE determines the DC operating point, the large signal transistor and diode models are converted into linear small signal models. All nonlinear effects of the circuit will not be accounted for in the AC frequency sweep, which generates a Bode plot/frequency response. Magnitude, phase, real, or imaginary data is produced.

Simulation Types and Data Acquisition

All of the simulators have the ability to perform the following analysis:

DC Operating Point Analysis

DC Small signal Transfer Function

DC Sweep Analysis

Sensitivity Analysis

AC Analysis

Noise Analysis

Distortion Analysis

Pole-Zero Analysis

Transient Analysis

Fourier Analysis

Temperature Analysis

The reference manual that accompanies a particular simulator provides sufficient information to perform any of the above analysis.

Convergence Problems

Convergence problems can be the most perplexing aspect of performing a simulation. There is a methodology that comes with experience. This secton of the text will provide a structured attack that should cure most convergence problems. The convergence suggestions should be performed in the order that they are listed. They are prioritized manner that should be of the most benefit. Begin with the obvious.

Common mistakes:

- Verify that all circuit connections are valid, proper component polarity, and a DC path from every node to ground. RENET, or REDRAW.
- Verify that all components have the correct values (i.e. MEG instead of M(milli) for 1E6). Components with no assigned value may be set to a default value determined by the simulator.
- Verify that all model parameters are realistic; especially if the model was created or altered by you.
- Verify that every node has two connections.
- Verify that voltage or current generators have the correct syntax and appropriate values.
- Use a series equivalent in place of capacitors or current sources that are placed in series.
- Verify that the letter zero was not used in place of zero (0).
- If B elements are used in the circuit, verify that division by zero cannot occur.
- Verify that dependant source gains are correct.

[Hymowitz]

DC Convergence Solutions

1. **Set ITL1= 400 in the . OPTIONS statement.**

   This setting increases the number of iterations that SPICE will perform before

   generating a none convergence warning and aborting the simulation.

2. **Add .NODESETs.**

   Voltages can be assigned to the nodes of the top level schematic. The initial guess

   made by SPICE to determine the DC bias point incorporates the nodsets. This can

   greatly reduce the number of iterations required to converge, increasing the

   probability of a simulation converging. Improper nodesets can result in inaccurate

   results. Care should be taken in setting the .NODESET statements.

3. **Use pulse statements to turn on DC power supplies**

   Example: V1 3 0 5 DC

   Becomes: V1 3 0 PULSE 0 15

   This allows the user to turn on the power supplies. A rise time may also be used to

   provide a realistic turn on.

4. **Set Gmin in the .OPTIONS statement.**

   Set GMIN=1n, or GMIN=1u. This sets the minimum conductance across all

   semiconductor devices.

5. **Set RSHUNT in the .OPTIONS statement.**

   This option places a resistor, with the value assigned globally by RSHUNT, from

   every node in the circuit to ground. A solution obtained using this convergence

   technique could be made at an incorrect operating point. The solution should be

   carefully examined.

6. **Set ILT6=100 in the .OPTIONS statement.**

Source stepping decreases all of the DC stimulus until a DC bias point is

determined, or they are reduced to zero volts. The voltages are then gradually

stepped from the DC bias point that converged, which may be at ground, back to

the assigned value. The source stepping algorithm uses gradual increases in

voltage, to establish a new DC bias point, using the previous DC bias point as the

initial guess. This process continues until a DC bias point has been establish for

the assigned values of the stimulus of the circuit.

Transient Convergence Solutions

1. **Verify that DC convergence has been achieved.**

   View the error statements in the text editor to verify that that the convergence

   problem pertains exclusively to the transient simulation.

2. **Verify that the time step provides an appropriate resolution.**

   The time step must be small enough to provide appropriate resolution of the

   switching waveforms generated by the simulation. The time step should be

   assigned to an order of magnitude smaller than the shortest period in the

   simulation. For example, in a 100KHz oscillator the period is 10uSec. The time

   step should be set to 1uSec.

   .TRAN 1u 3m

   Other factors such as the on time or the duty cycle should be considered when

   determine the time step. Once convergence has been achieved this value can be

   maximized to reduce simulation time.

3. **For oscillating or switching circuits, set METHOD=GEAR in the .OPTIONS statement.**

   This statement selects the type of integration method that SPICE uses to solve the

   transient equations. Gear integration should be used for all switching circuitry.

The default integration, trapezoidal, has a tendency to produce oscillations.

4. **Add UIC (Use Initial Conditions) to the .TRAN statement.**

   This statement causes SPICE to bypass the DC operating point analysis. Initial

   conditions should be placed on capacitors at there expected operating voltage. Just

   as with the use of nodesets, initial condition statements can produce incorrect

   solutions. Results should be verified for validity.

5. **Set ITL4=500 in the .OPTIONS statement.**

   This statement increases the number of iterations performed by SPICE, before a

   nonconvergence warning is issued and the simulation is aborted.

6. **Set RELTOL=.01 in the .OPTIONS statement.**

   This statement decreases the accuracy of the simulation by increasing the relative

   error tolerance required for convergence. This statement should not be set lower

   than .01. The simulation run time is also reduced by increasing RELTOL. As a

   general rule, every order of magnitude decrease of the relative tolerance results in

   doubling the simulation run time.

7. **Reduce the rise and fall times of PULSE sources.**

   Drastic changes in voltage can result in nonconvergence problems. Soften the

   edges of the pulse source by increasing the rise time and fall time of the pulse

   waveform.

8. **Set TRTOL=40 in the .OPTIONS statement.**

   This statement is proportional to the step size used when performing a transient

   simulation. The accuracy of the simulation can be compromised by changing the

   TRTOL from the default of setting of TRTOL=7.

9. **Reduce the accuracy of ABSTOL/VNTOL if current and/or voltage levels permit.**

   The default value of ABSTOL=1pA, and VNTOL=1uV, should be

set to about

eight orders of magnitude below the level of the maximum current and voltage.

10. **Set the RAMPTIME=10nS in the .OPTIONS statement.**

This statement ramps all independent sources up from zero at the beginning of the

transient analysis. This statement is beneficial if the transient analysis will not

begin. Take care to allow enough time for sources to ramp up, otherwise this

statement could do more harm than good.

AC Convergence Solutions

1. **Do not use steps 3-5 of the DC convergence solutions.**

Using these steps may not produce a valid DC operating point, which is essential for SPICE to linearize the circuit. See the AC analysis description. Once DC convergence is achieved, the AC analysis will also converge.

Convergence failures are not always a function of SPICE, and can not be fixed using .OPTIONS statements or other convergence techniques. Convergence failures may result from hardware problems.

References

Sandler, Steven M. SMPS simulation with SPICE. 1996. McGraw Hill.

Kielkowski, Ron. Inside SPICE. 1995. McGraw Hill.

3
Filter Circuits

Filter circuits form the initial building block for many different circuits. Communications circuits require only certain frequency signals be passed onto transmitter and receiver circuits. Power converters use filters on the input bus to filter out spurious noise and on the output line to smooth the rectified signal. Digital logic circuits use bypass capacitors and RC networks to filter supply voltages that must travel some distance before reaching the IC. Delays required in some circuitry can be provided by filters. Filter circuits are so important to these and many other circuits because of the simple function they perform. Filters allow signals of desirable frequencies to pass, while blocking signals of undesirable frequencies. For most of the circuits, the transient response of the filter is matched to hardware results. For a select few filters a network analyzer was utilized to measure the response of the filter.

Although filters perform a simple function, the amount of circuits and design parameters used to design filters are much more complex. Filters can be optimized for a low Q in the pass band (Butterworth type) or a high attenuation in the stop band and steeper rolloff near the cutoff frequency (Chebyshev type). Filters that are used primarily for delays in circuitry might use the Bessel-Thomson type of filter. The large applications of the filter circuit equates to the equally large filter design types for the engineer.

#1: 4th order butterworth low pass filter

The first filter of the chapter is one of the most popular. The schematic of the 4th order butterworth response low pass filter is shown in Figure 1-1. The response of the filter to an AC sweep is shown in Figure 1-2. Notice the flat response in the pass band and the stop band frequency of 100 Khz.

Figure 1-1: Schematic of 4th order Butterworth low pass filter

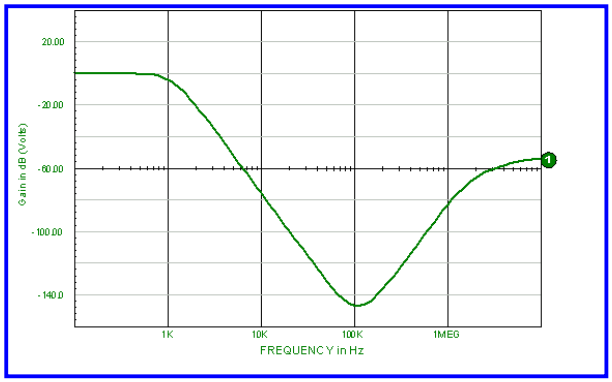


Figure 1-2: AC filter response

Unfortunately, the lab used in the creation of the circuits in this book closely resembles the lab of other engineering companies around the world. We use 5% tolerance resistors and 10 % tolerance capacitors either soldered to a vector board or plugged into a solderless breadboard. This introduces various paracitics and inaccuracies to our result. In order to more capably show the use of SPICE simulation software, we will frequently run the simulations with the exact values of the resistors or capacitors being used in our lab breadboard. The measured resistors and capacitors of Figure 3-1 are shown in our breadboard configuration in Figure 1-3.

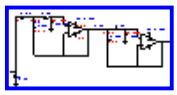


Figure 1-3: Breadboard configuration of 4th order Butterworth filter

In order to correlate the breadboard to the SPICE circuit, a 5 volt pulse was applied with a 100 nSec rise time using the following command in a V source:

order butterworth low pass filter

PULSE 0 5 750U .1U

This creates a delay of 750 uSec to allow the filter to be at steady state when the pulse is applied. The step response of the breadboard circuit is shown in Figure 1-4A, while that of the IsSpice model is shown in Figure 1-4B. The top trace is the 5 volt pulse, while the bottom trace is the filter response measured at the output of the X5 Op-Amp.

- Spice tip: Some convergence problems or problems in results are caused by attempting to run two different types of analyses in the same model at the same time. This phenomenon was noticed while simulating this circuit. If the AC simulation was performed at the same time in IsSpice, the operating point caused a convergence problem in the transient simulation. This can sometimes be remedied by manipulating .OPTIONS lines and adding IC (Initial Condition) statements to parts.

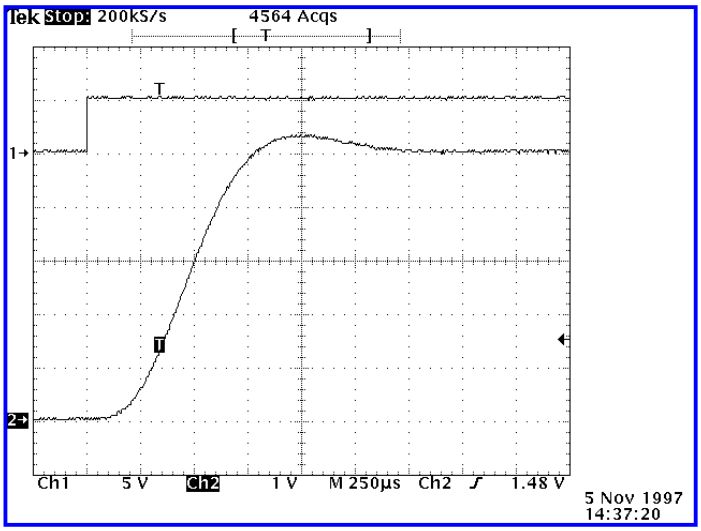


Figure 1-4A: Breadboard filter response to step input

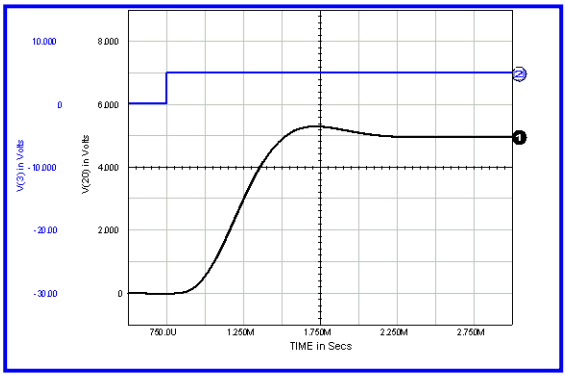


Figure 1-4B: IsSpice filter response to step input

The circuit was also simulated on Microcap and Pspice. The Microcap results are

shown in Figure 1-5A and 1-5B, while the Pspice results are shown in Figure 1-6A and 1-6B.

- Simulation tip: Notice in the results of the Microcap voltage step response simulation the magnitude of the output voltage was incorrect. The reason for this is unknown, however the lesson here is you must know the limitations of your models. Many times, these libraries can be provided by IC manufacturers or the software company. It is very important to remember that these models may not be accurate for the parameter that you are interested in. People make models to model different aspects of the part. For example, some models may have noise rejection modeled accurately, or AC characteristics, or input current draw, or some may not model any of these. If the model does not accurately reflect the characteristic you are interested in, this does not necessarily mean the model is useless or wrong (although this is a possibility).

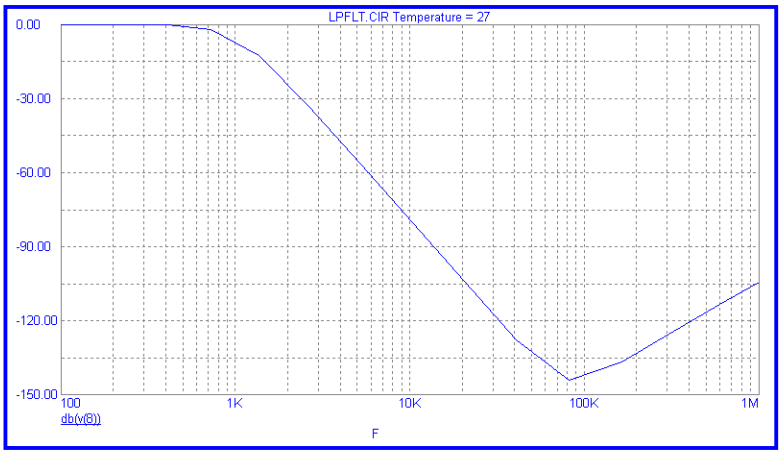


Figure 1-5A: Microcap AC filter response

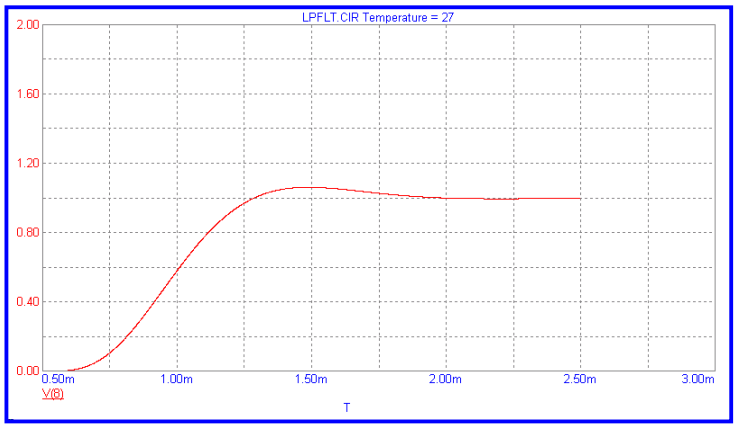


Figure 1-5A: Microcap filter response to step input

order butterworth low pass filter

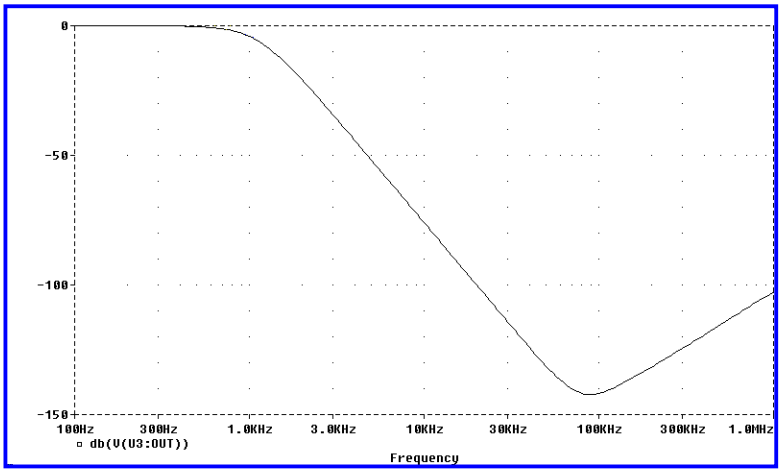


Figure 1-6A: Pspice AC filter response

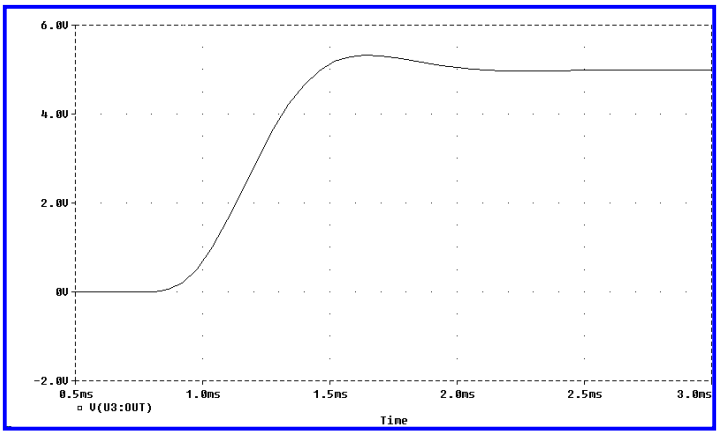


Figure 1-6B: Pspice filter response to step input

Run Time Summary		
IsSpice v 7.6	PsPice v 6.3	Micro-Cap V v2
17.016 Sec	1.36 Sec	30.59 Sec
Advantages: Moderate parts count, flat response in the pass band		
Disadvantages: Filter Q greater than other filter types		

Filenames: lp_fltr (IsSpice) lpflt (Micro-cap) lp_flt (Pspice)

order butterworth low pass filter

#2: 4th order butterworth high pass filter

A quick modification to the circuit in figure 2-1 produces a high pass filter response. The schematic for the high pass filter is shown in figure 2-1 and the AC response of the filter is shown in figure 2-2.

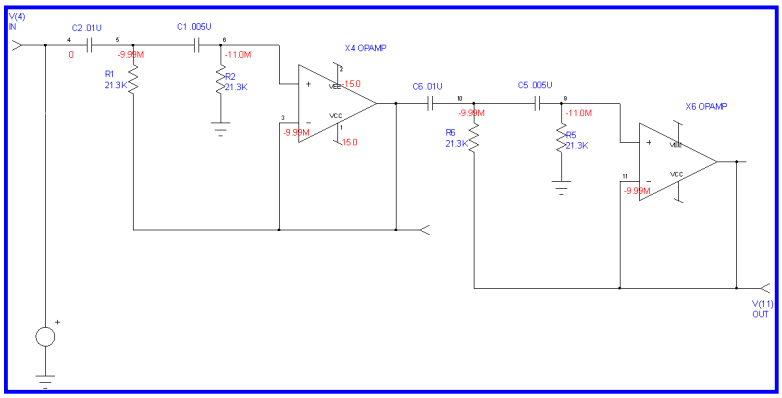


Figure 2-1: Schematic of 4th order Butterworth high pass filter

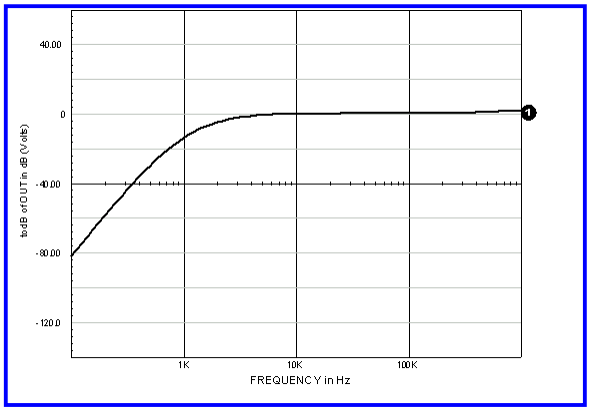


Figure 2-2: AC filter response

The same pulse in the low pass filter was applied to the high pass filter. The breadboard results are shown in figure 2-3. These may be compared to the IsSpice results shown in figure 2-4. The top trace is the 5 volt pulse, while the bottom trace is the filter response measured at the output of the X6 Op-Amp.

order butterworth high pass filter

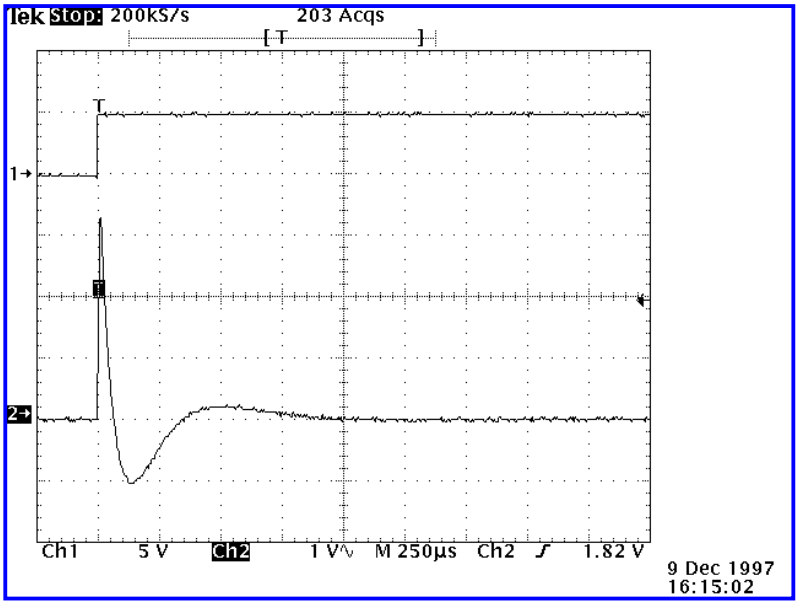


Figure 2-3: Breadboard filter response to step input

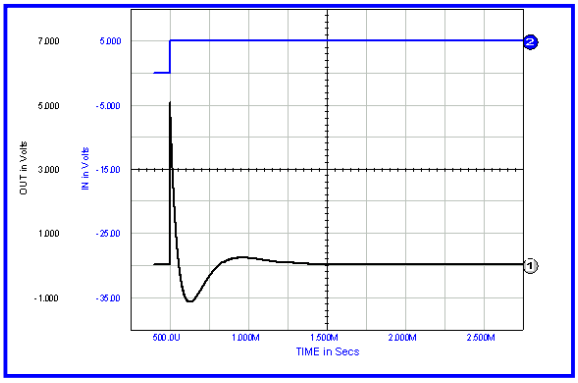


Figure 2-4: IsSpice filter response to step input

This circuit was also simulated using Microcap and Pspice. The results of these simulations are shown below.

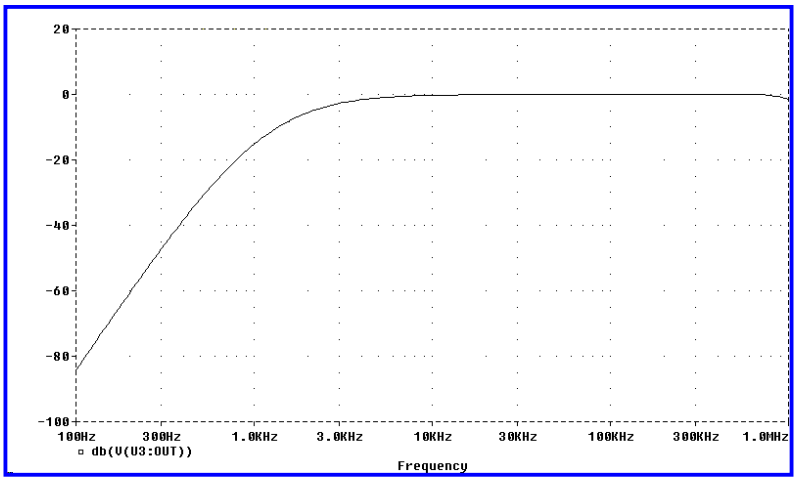


Figure 2-5: Pspice AC filter response

order butterworth high pass filter

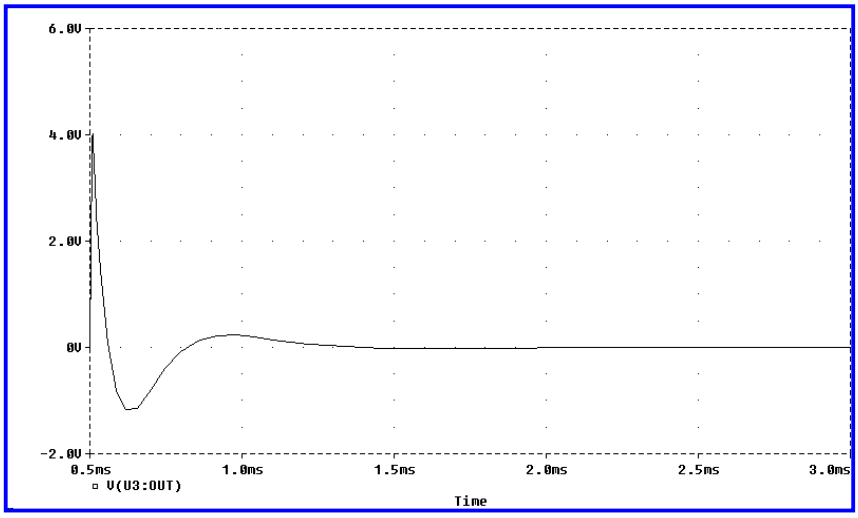


Figure 2-6: Pspice filter response to step input

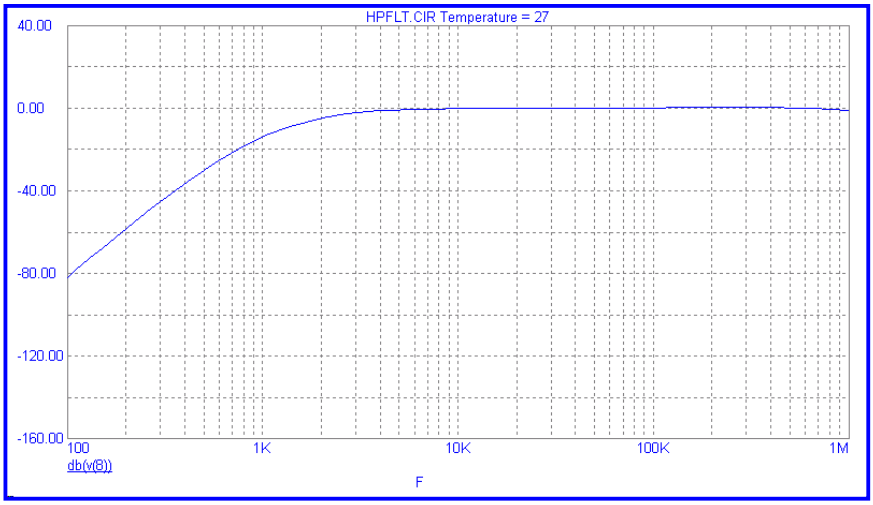


Figure 2-7: Microcap AC filter response

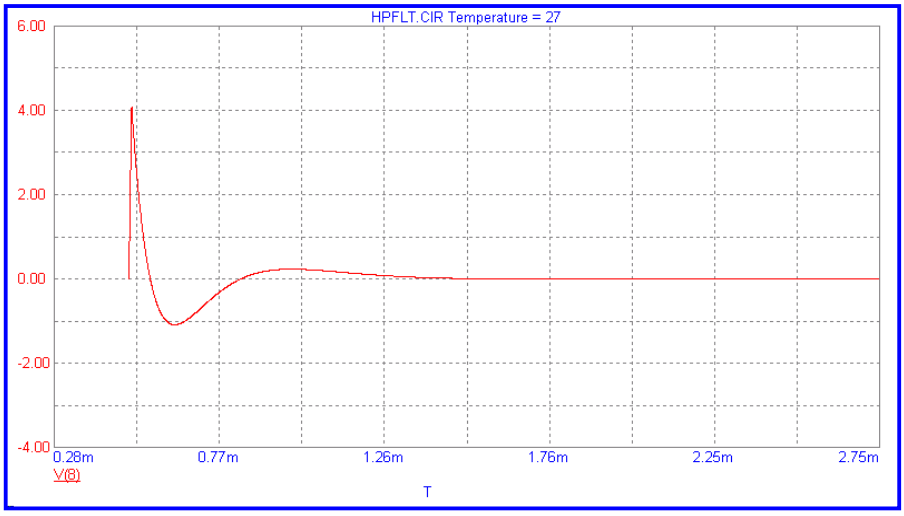
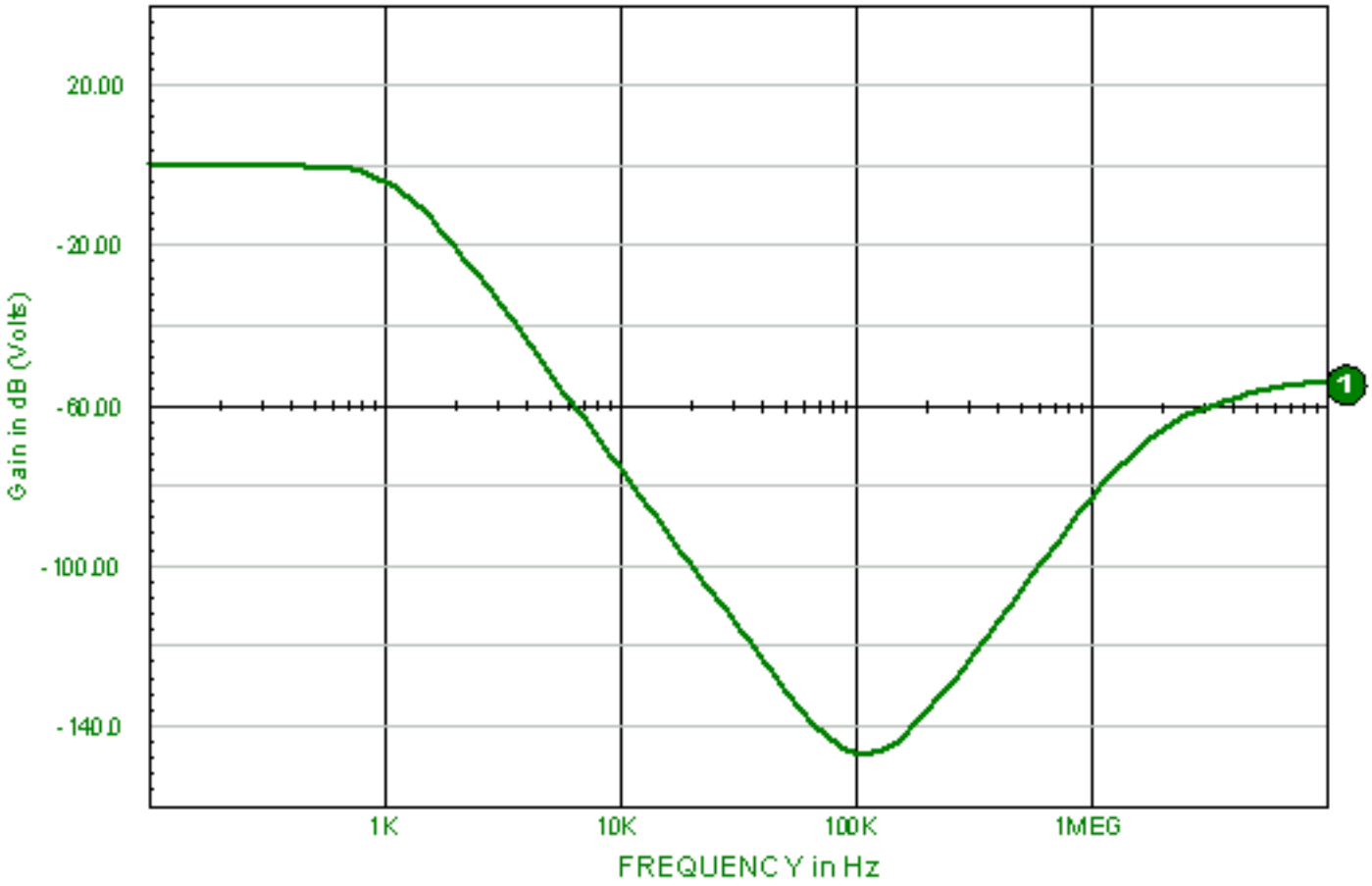


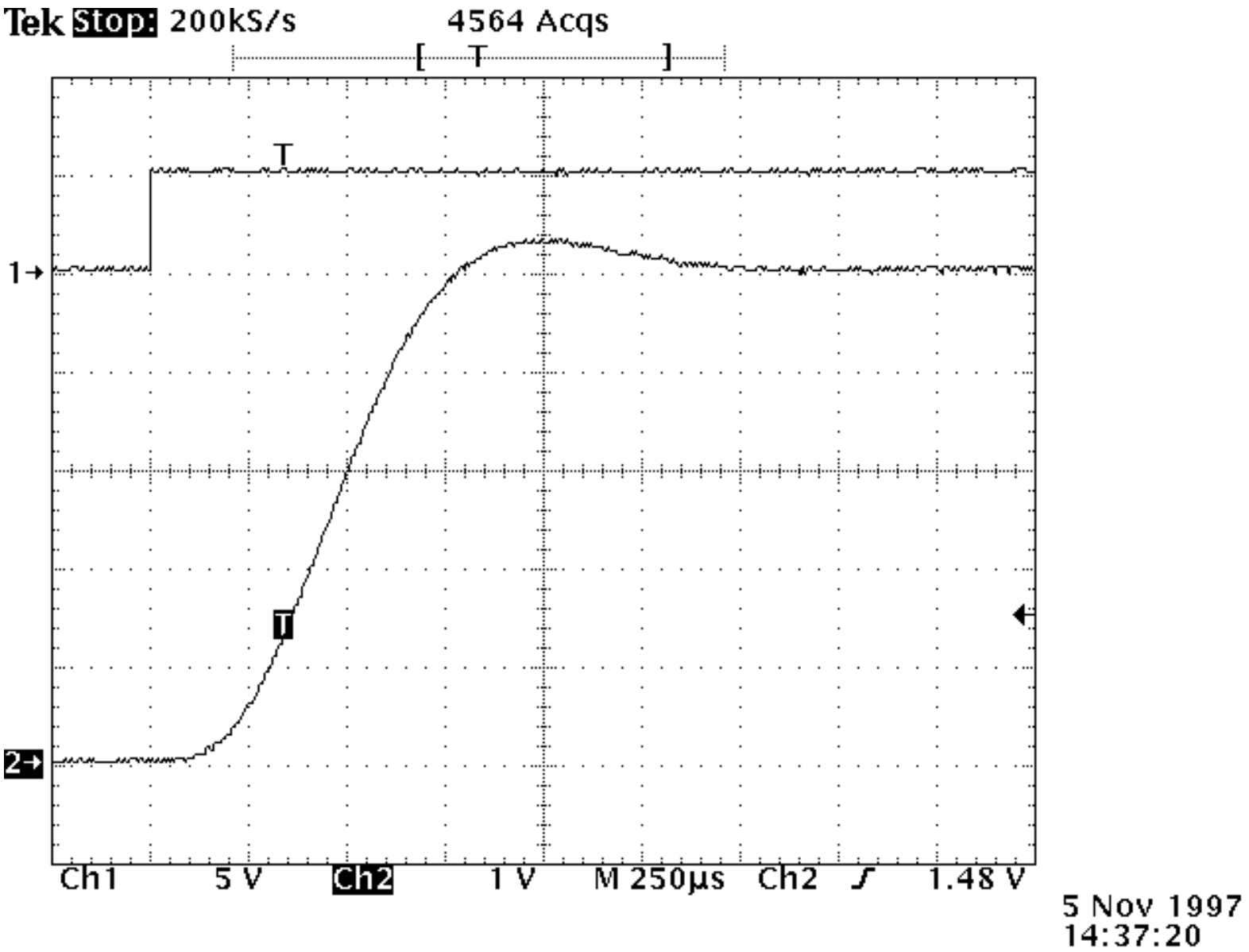
Figure 2-8: Microcap filter response to step input

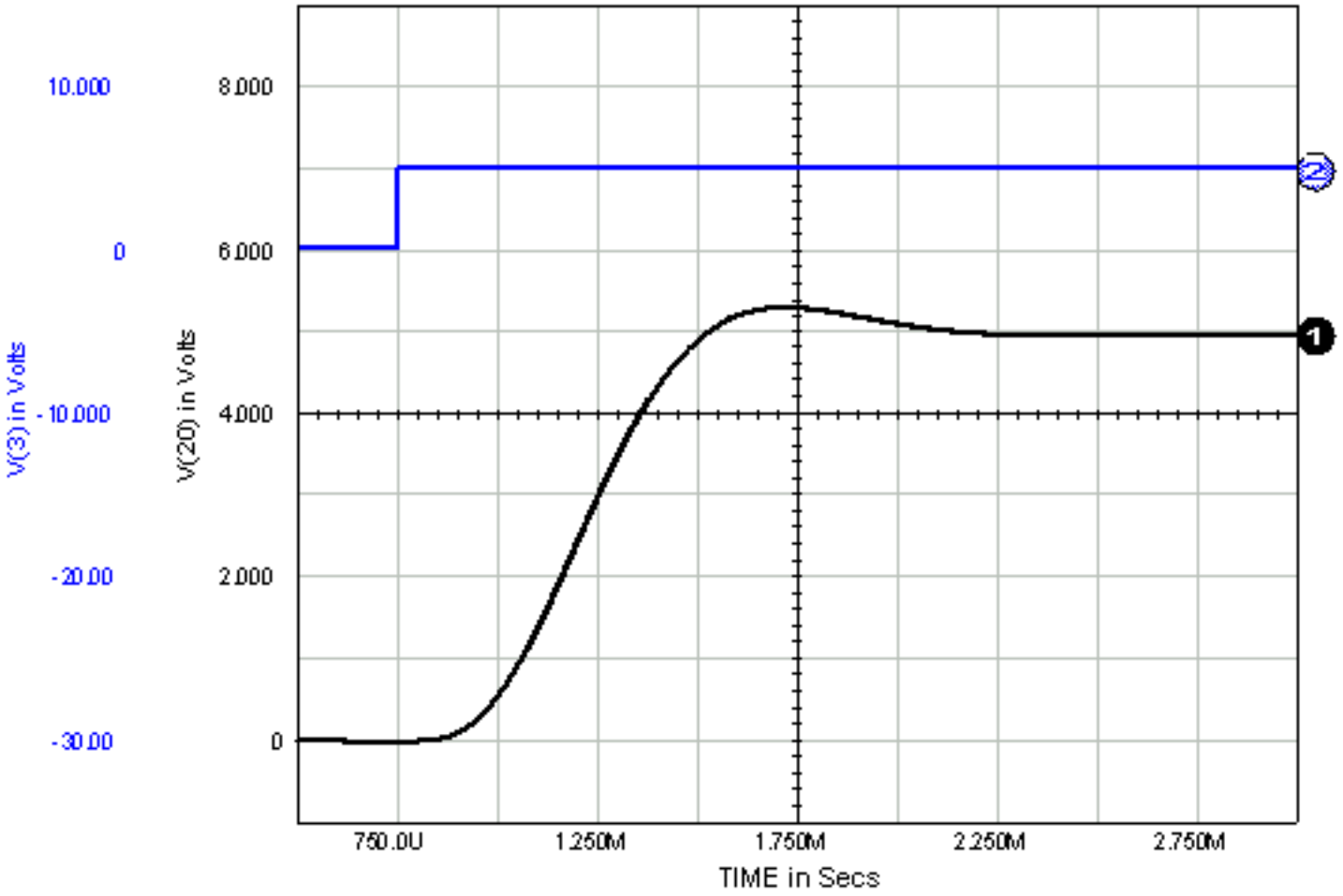
order butterworth high pass filter

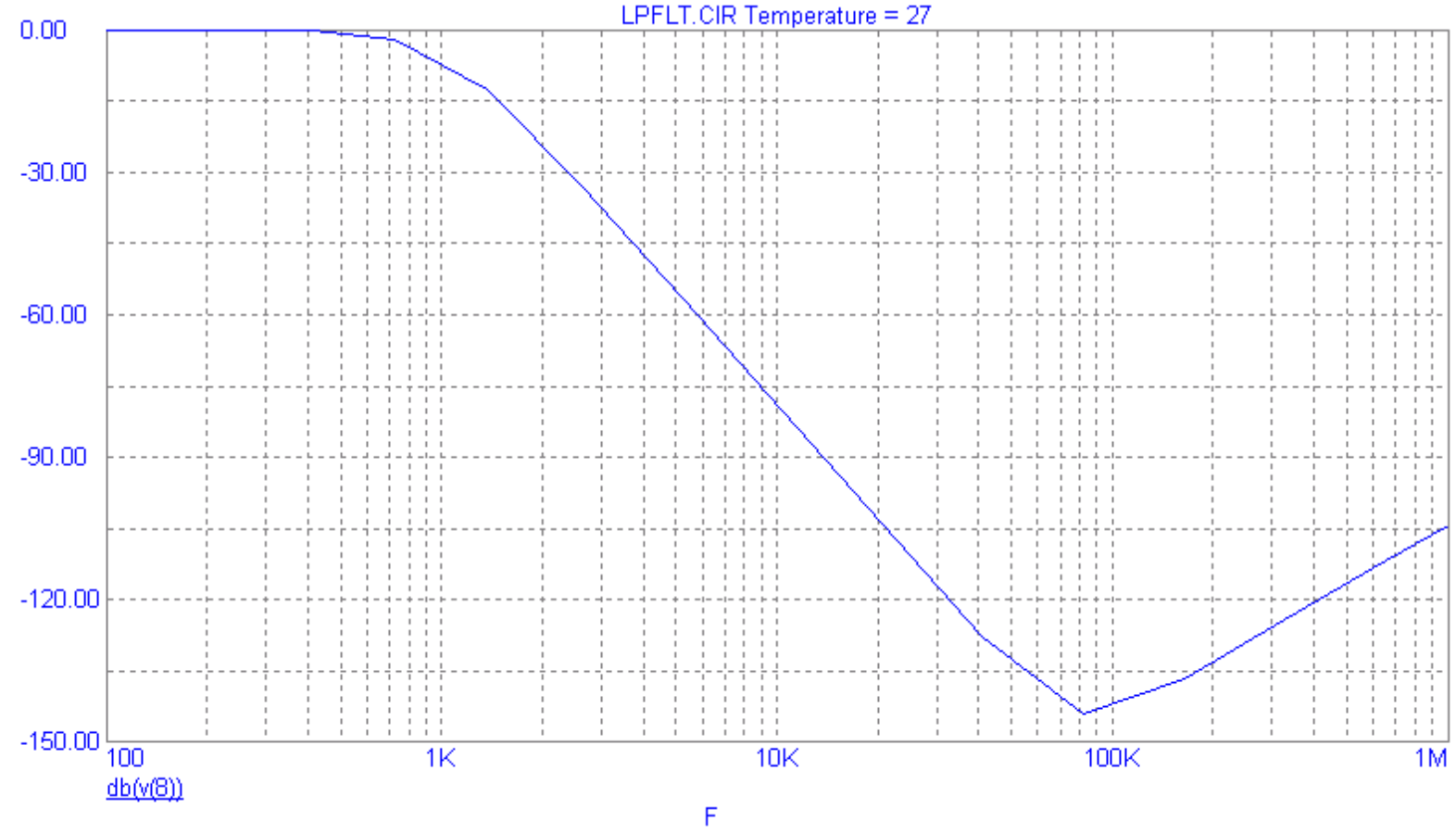
Run Time Summary		
IsSpice v 7.6	PsPice v 6.3	Micro-Cap V v2
21.566 Sec	0.71 Sec	37.76 Sec
Advantages: Moderate parts count, flat response in the pass band		
Disadvantages: Filter Q greater than other filter types		

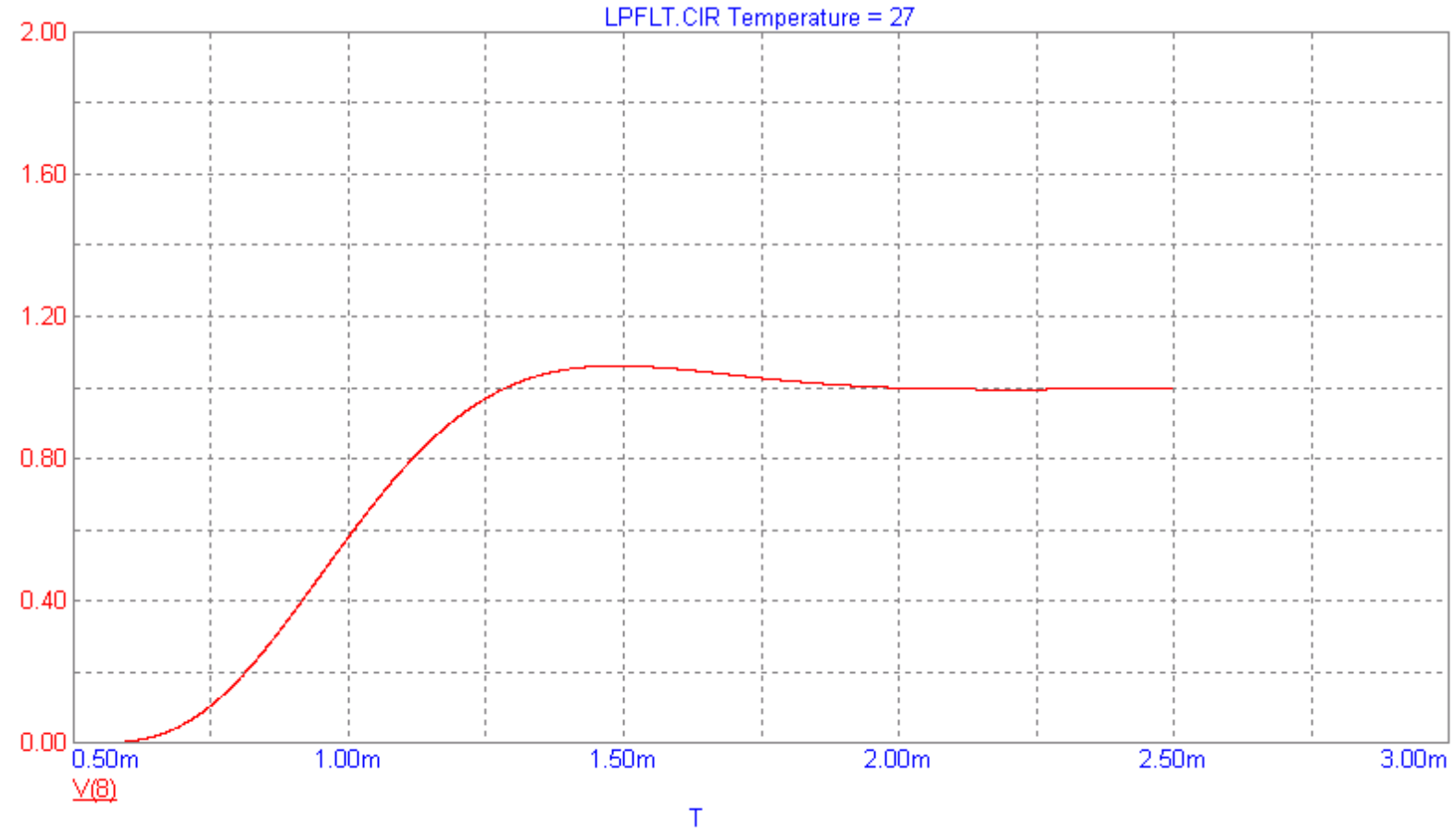
Filenames: hp_fltr (IsSpice) hpflt (Micro-cap) hp_flt (Pspice)

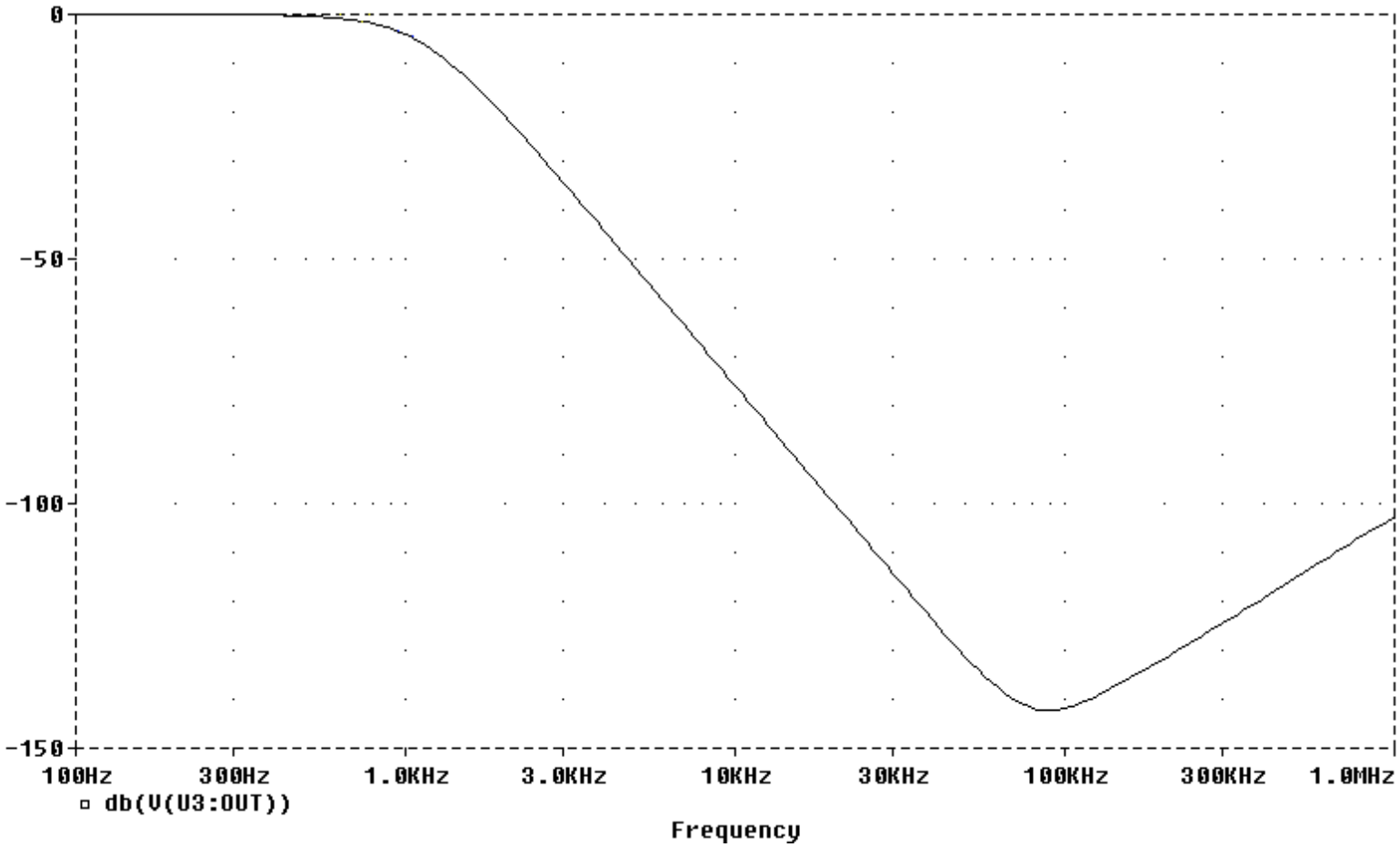

20.00
-20.00
-60.00
-100.00
-140.0
Gain in dB (Volts)
1K
10K
100K
1MEG
FREQUENCY in Hz
1

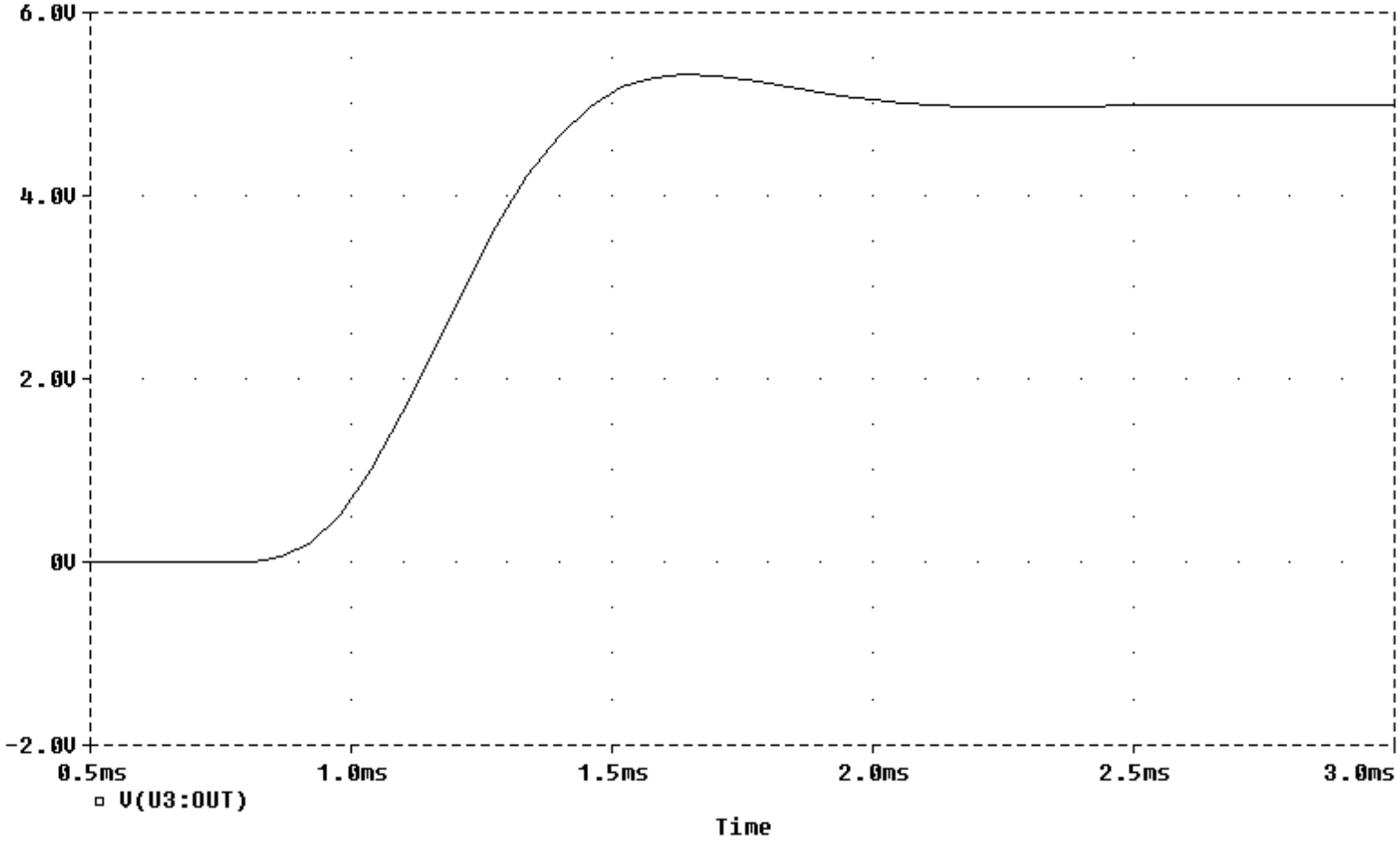

Tek Stop: 200kS/s
4564 Acqs
T
1→
2→
Ch1 5 V
Ch2 1 V
M 250µs Ch2 ∫ 1.48 V
5 Nov 1997
14:37:20


10.000
0
-10.000
-20.00
-30.00
V(3) in Volts
8.000
6.000
4.000
2.000
0
V(20) in Volts
750.0U
1.250M
1.750M
2.250M
2.750M
TIME in Secs
2
1


LPFLT.CIR Temperature = 27
0.00
-30.00
-60.00
-90.00
-120.00
-150.00
100
1K
10K
100K
1M
db(v(8))
F


LPFLT.CIR Temperature = 27
2.00
1.60
1.20
0.80
0.40
0.00
0.50m
1.00m
1.50m
2.00m
2.50m
3.00m
V(8)
T


0
-50
-100
-150
100Hz
300Hz
1.0KHz
3.0KHz
10KHz
30KHz
100KHz
300KHz
1.0MHz
db(V(U3:OUT))
Frequency


6.0V
4.0V
2.0V
0V
-2.0V
0.5ms
1.0ms
1.5ms
2.0ms
2.5ms
3.0ms
V(U3:OUT)
Time

#3: 4th order butterworth band pass filter

The schematic in Figure 3-1 shows the configuration for a butterworth band pass filter. The AC characteristic of the filter is shown in Figure 3-2.

Figure 3-1: Schematic of 4th order Butterworth band pass filter

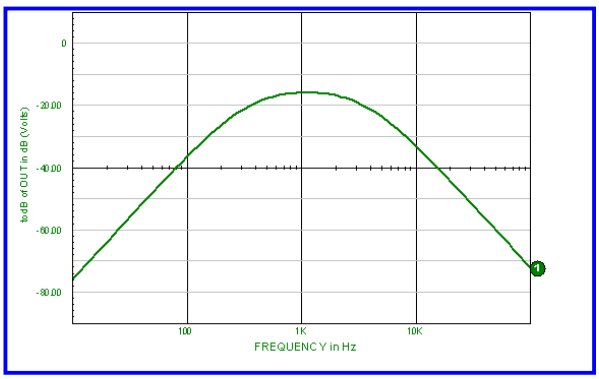


Figure 3-2: AC filter response

The breadboard circuit was pulsed with a 5 volt step. The results of the band pass filter to the input step are shown in Figure 3-3. The top trace is the input step and the bottom trace is the filter response at the output of X5. The IsSpice circuit response to the input step is shown in Figure 3-4.

order butterworth band pass filter

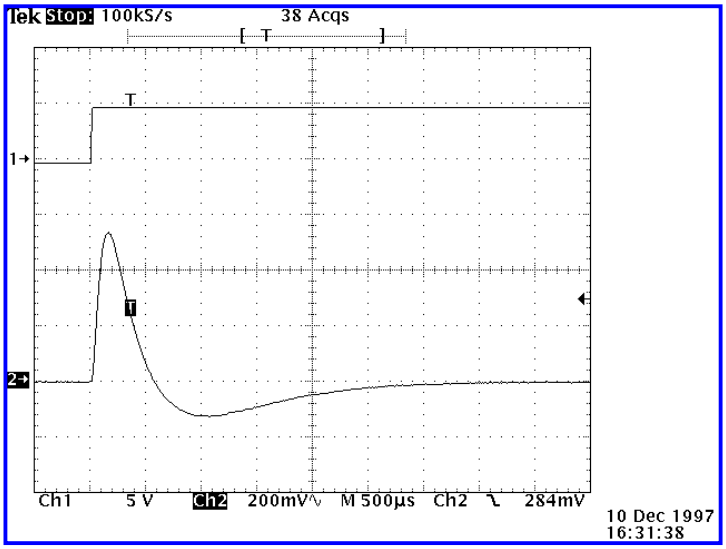


Figure 3-3: Breadboard filter response to step input

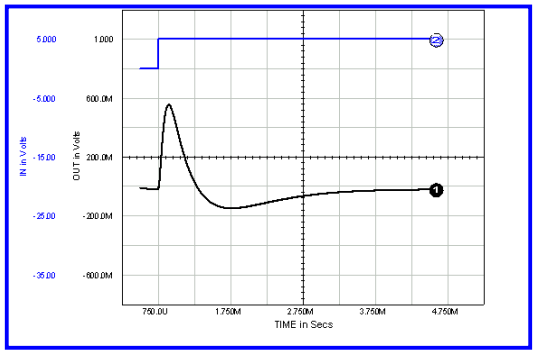


Figure 3-4: IsSpice filter response to step input

This circuit was also simulated using Pspice and Microcap. The results of these simulations are shown below.

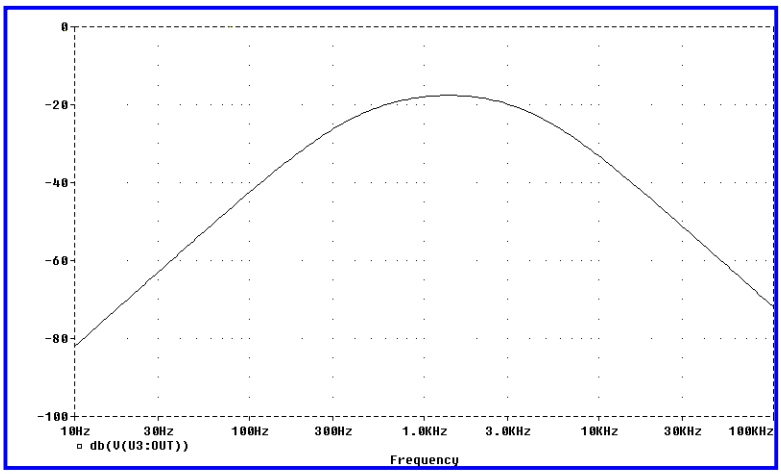


Figure 3-5: Pspice AC filter response

order butterworth band pass filter

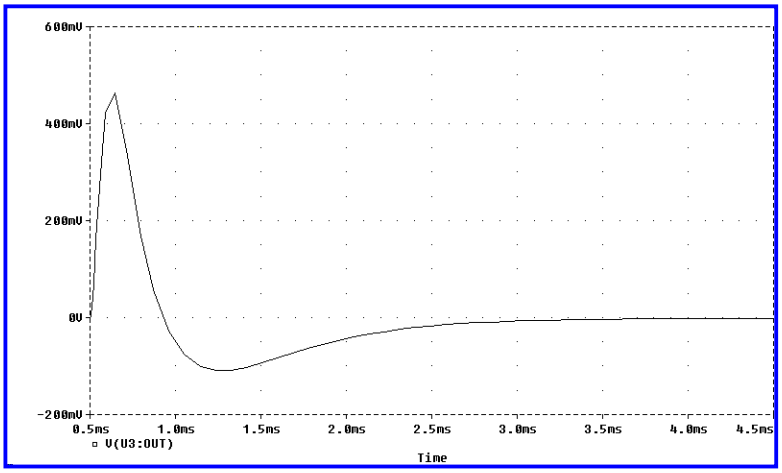


Figure 3-6: Pspice filter response to step input

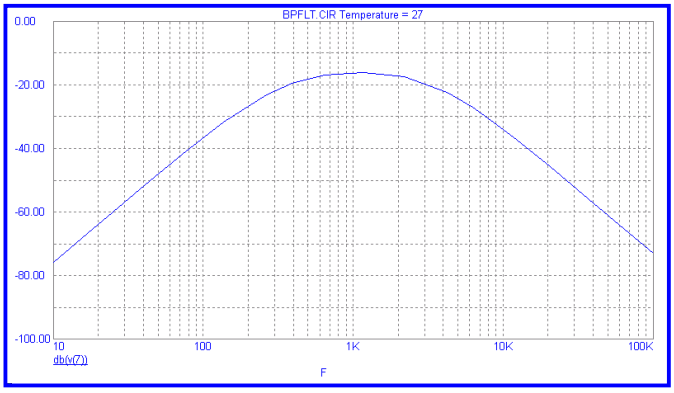


Figure 3-7: Microcap AC filter response

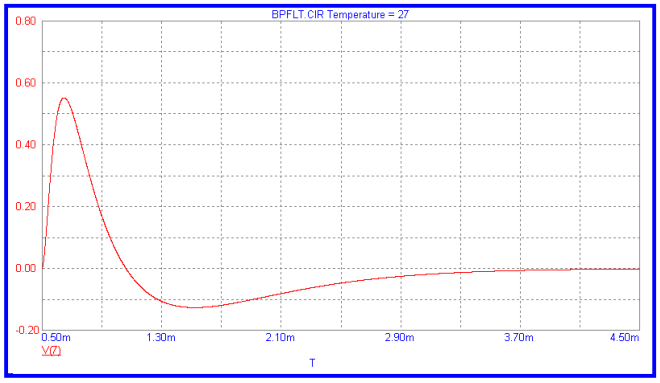


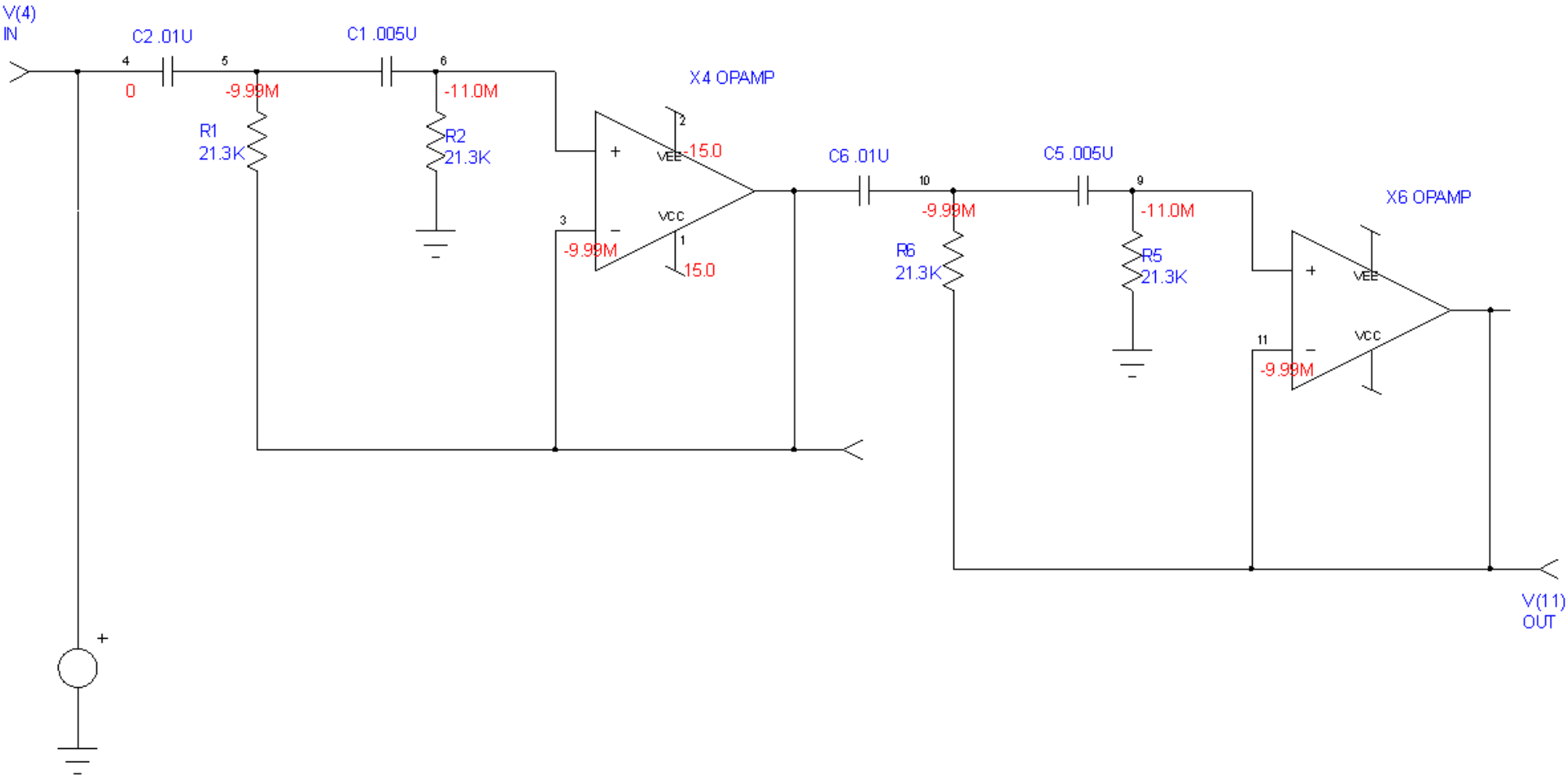
Figure 3-8: Microcap filter response to step input

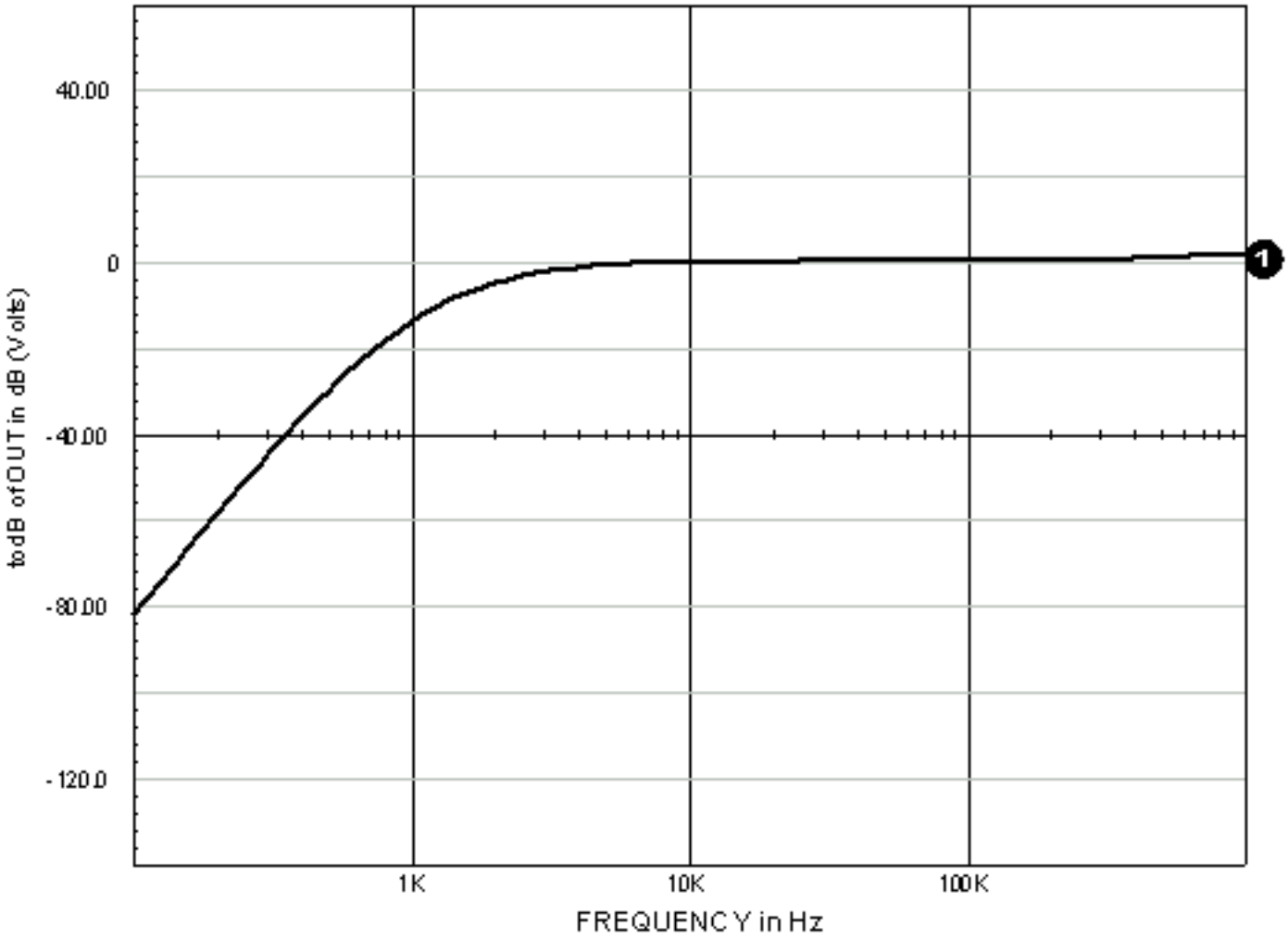
Run Time Summary

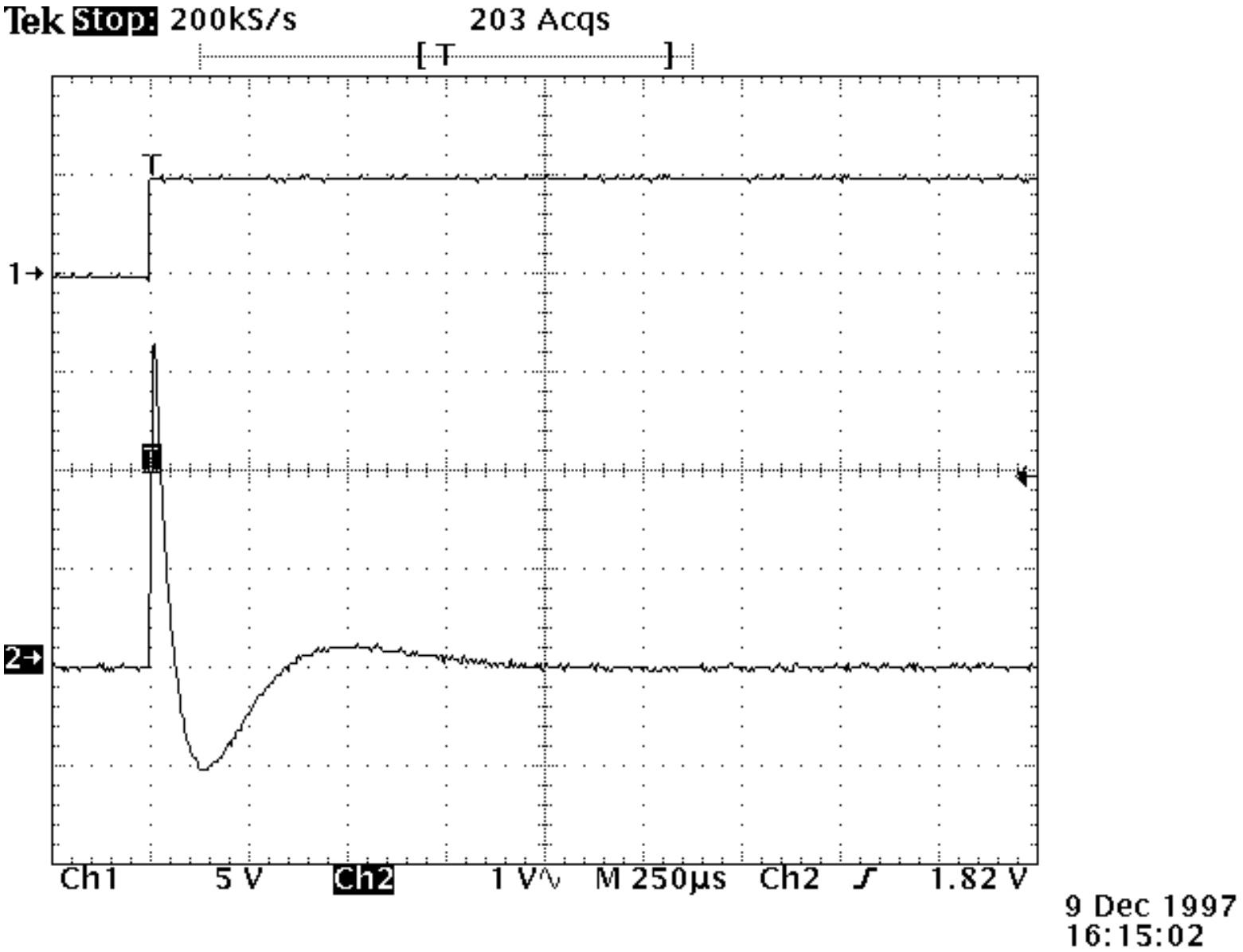
order butterworth band pass filter

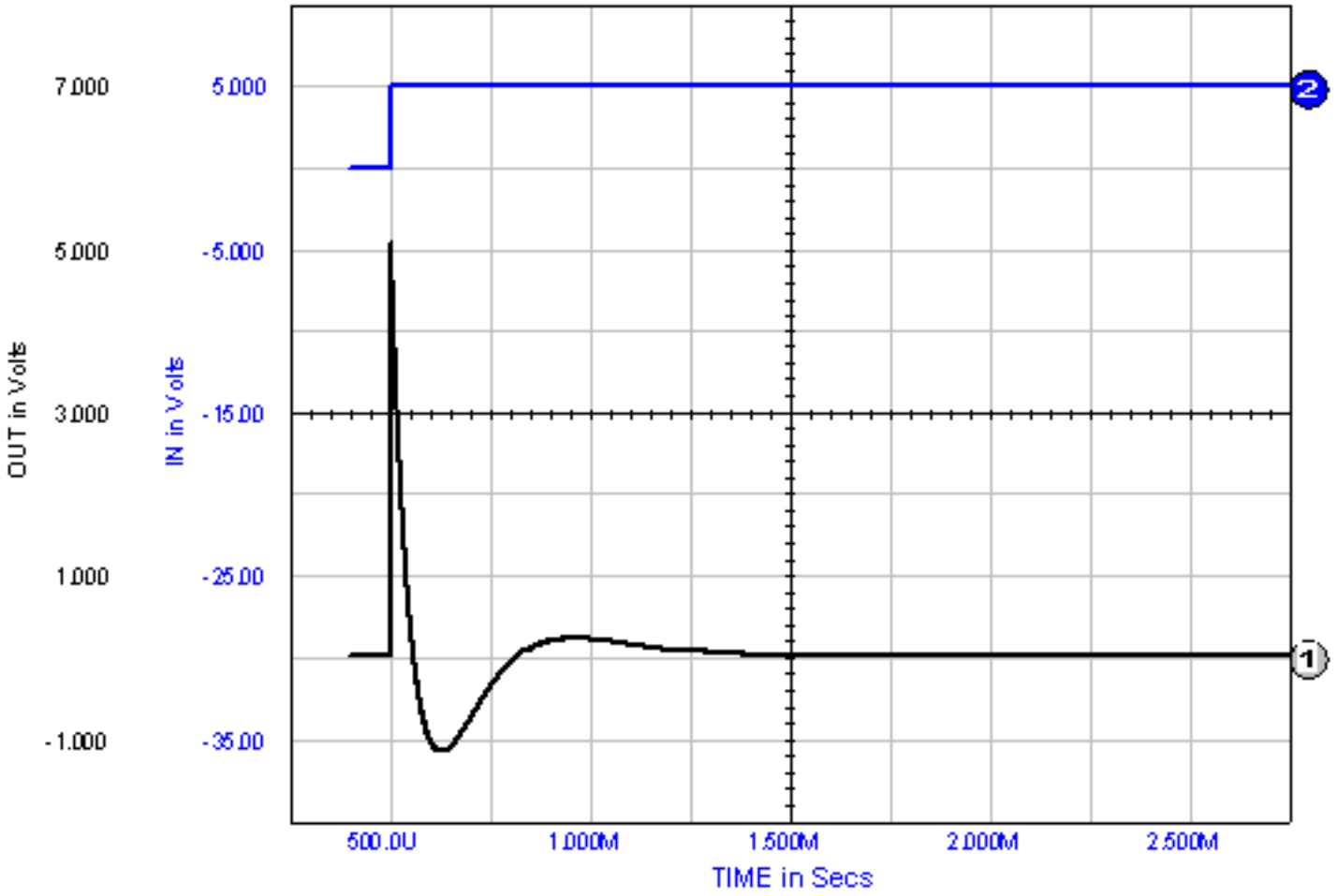
IsSpice v 7.6	PsPice v 6.3	Micro-Cap V v2
28.216 Sec	1.45 Sec	57.98 Sec
Advantages: Moderate parts count		
Disadvantages: Filter Q greater than other filter types		

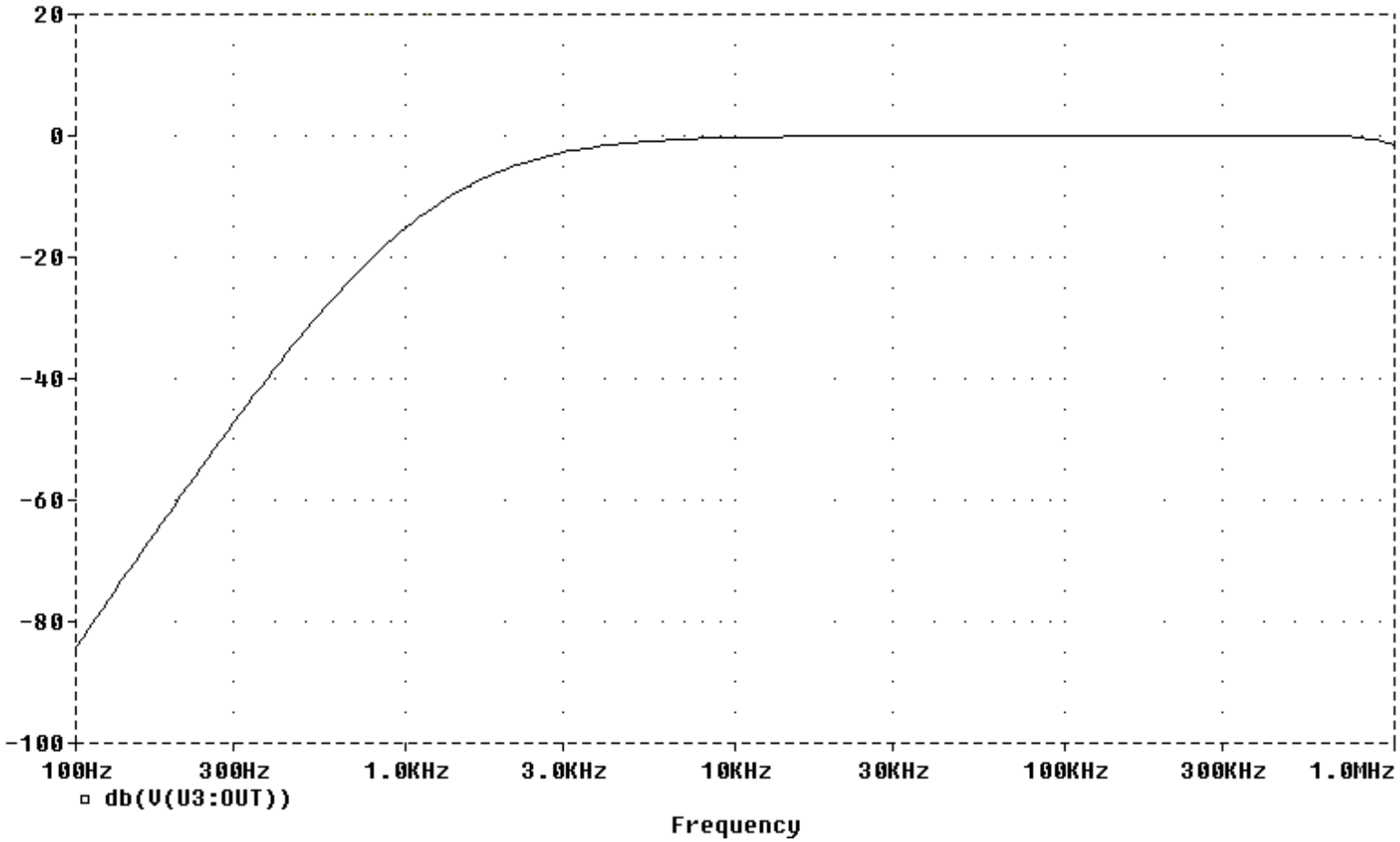
Filenames: bp_flt (IsSpice) bpflt (Micro-cap) bp_flt (Pspice)

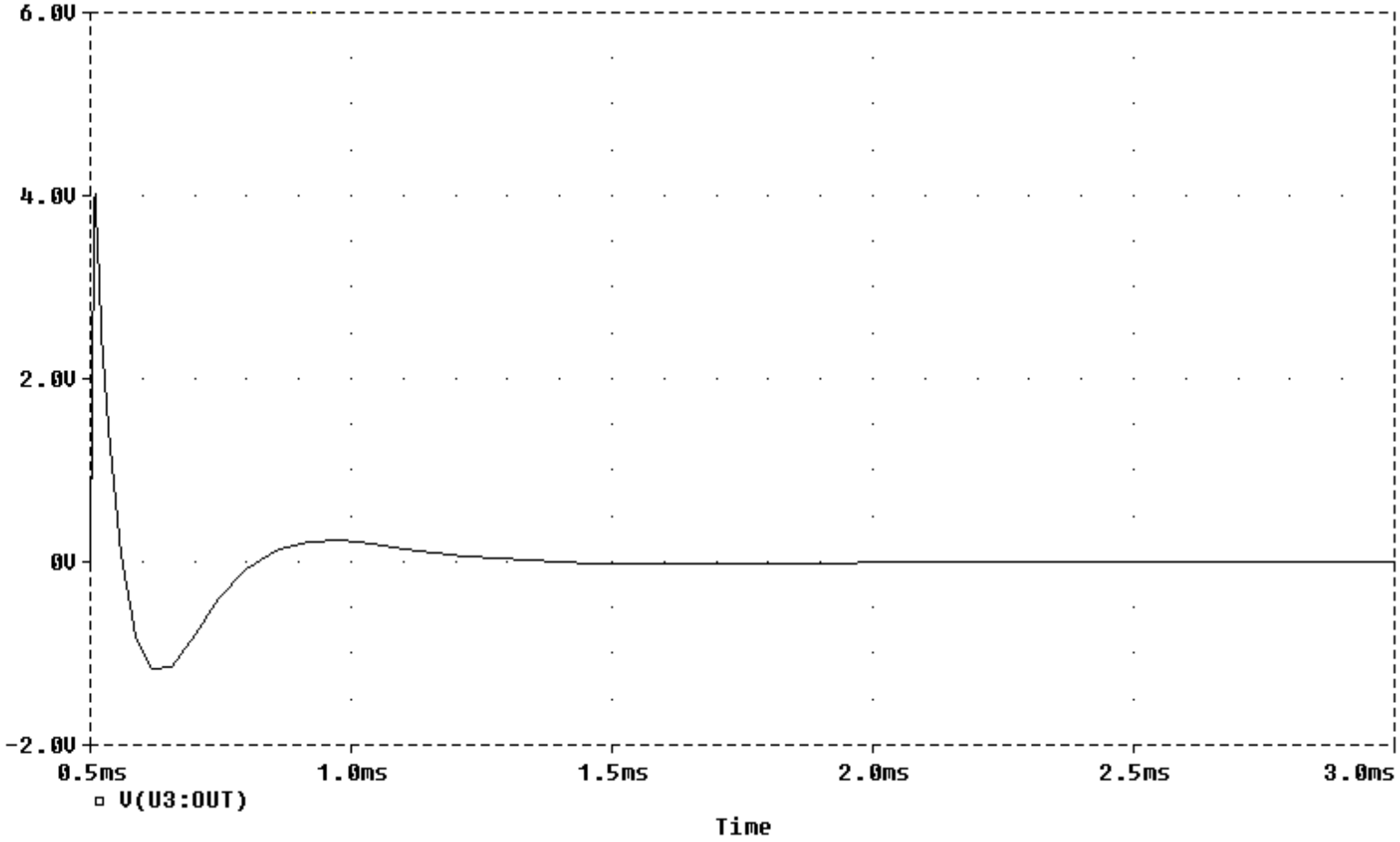

V(4)
IN
C2 .01U
C1 .005U
4
5
6
0
-9.99M
-11.0M
R1
21.3K
R2
21.3K
X4 OPAMP
2
VEE
-15.0
VCC
3
1
-9.99M
15.0
C6 .01U
C5 .005U
10
9
-9.99M
-11.0M
R6
21.3K
R5
21.3K
X6 OPAMP
VEE
VCC
11
-9.99M
V(11)
OUT

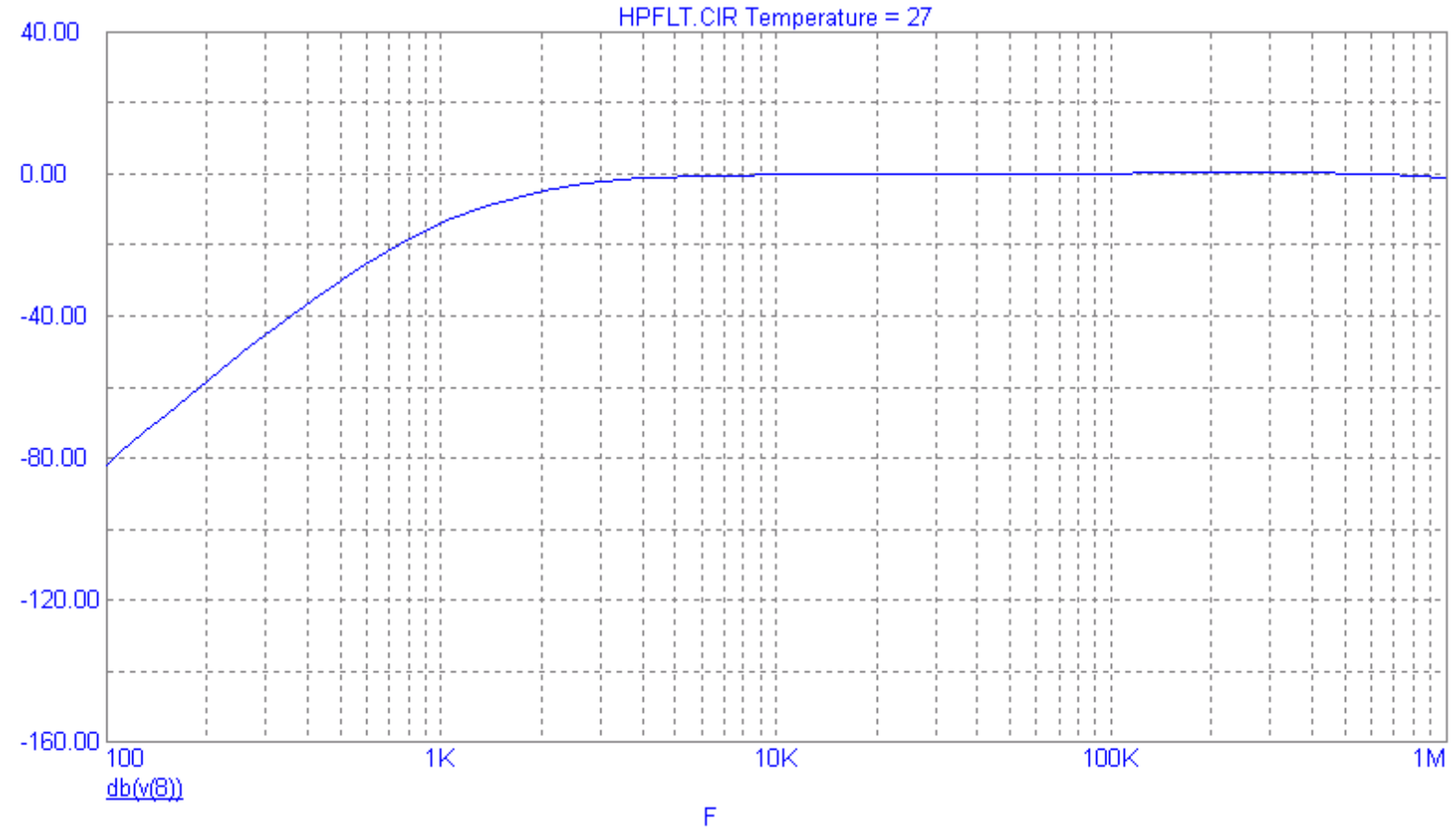

40.00
0
-40.00
-80.00
-120.0
1K
10K
100K
FREQUENCY in Hz
to dB of OUT in dB (Volts)
1

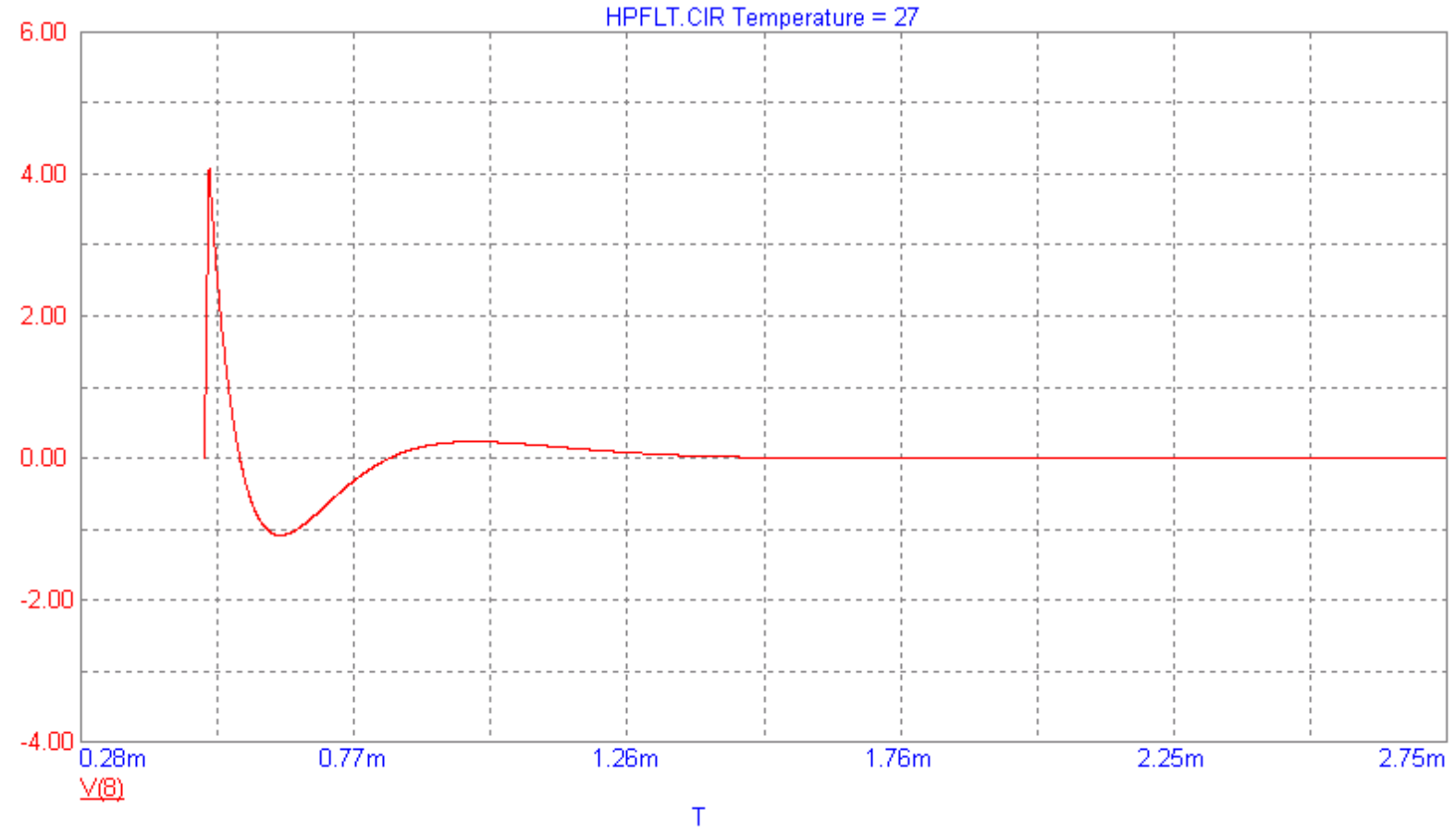

Tek Stop: 200kS/s
203 Acqs
1→
2→
Ch1 5 V
Ch2 1 V
M 250µs Ch2 1.82 V
9 Dec 1997
16:15:02


7.000
5.000
3.000
1.000
-1.000
OUT in Volts
5.000
-5.000
-15.00
-25.00
-35.00
IN in Volts
500.0U
1.000M
1.500M
2.000M
2.500M
TIME in Secs
2
1


20
0
-20
-40
-60
-80
-100
100Hz
300Hz
1.0KHz
3.0KHz
10KHz
30KHz
100KHz
300KHz
1.0MHz
db(V(U3:OUT))
Frequency


6.0V
4.0V
2.0V
0V
-2.0V
0.5ms
1.0ms
1.5ms
2.0ms
2.5ms
3.0ms
V(U3:OUT)
Time


HPFLT.CIR Temperature = 27
40.00
0.00
-40.00
-80.00
-120.00
-160.00
100
1K
10K
100K
1M
db(v(8))
F


HPFLT.CIR Temperature = 27
6.00
4.00
2.00
0.00
-2.00
-4.00
0.28m
0.77m
1.26m
1.76m
2.25m
2.75m
V(8)
T

#4: Bessel-Thompson Delay low pass filter

The primary purpose of this filter is to add a delay to a pulse or data sequence. The use of the RC time constant allows this delay to be added to both the rising and falling edge of the pulse. The ideal response of the filter is a perfect reproduction of the input delayed by a specified time constant. The time delay of the Bessel-Thompson is measured by the time the pulse occurs until the time the response is 50% of the input step height.

A Bessel-Thompson filter was designed to close to 500 us of delay. The design procedure followed gave exact values for all of the capacitors and resistors. These values are rounded to the nearest value of capacitor available. The three spice packages are used to determine what the implemented delay will be. Measured values of all the components used in the hardware are used. The schematic and the breadboard results are shown as figure 4-1and figure 4-2 respectively.

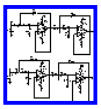


Figure 4-1: Bessel-Thompson Delay filter

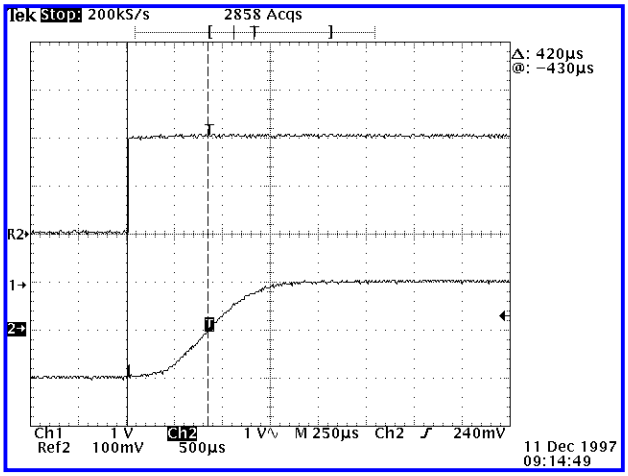


Figure 4-2: Breadboard filter response to step input

IsSpice had a built in LM124 model. The simulation response to a step input is

shown in figure 4-3, the AC simulation results are shown in figure 4-4.

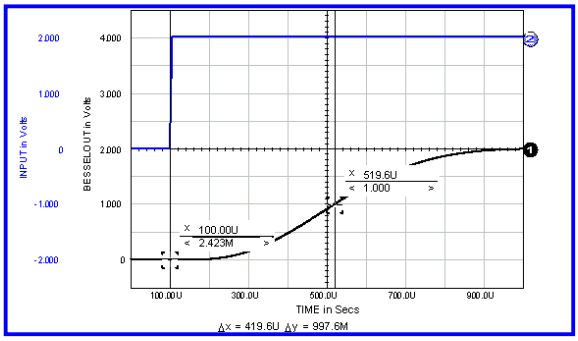


Figure 4-3: IsSpice filter response to step input

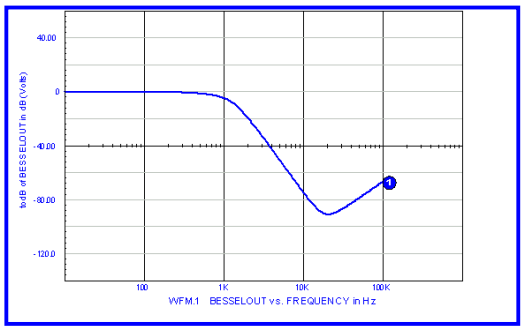


Figure 4-4: IsSpice AC filter response

The evaluation version of Pspice has a model for the LM324, but the default model had an error in it. The UA741 opamp model was used in its place. The operation amplifier does not play a critical role in this circuit because of the slow response of the circuit. The limiting parameter of the delay time is the RC time constant and not the slew rate or drive capability of the operational amplifier. The Pspice model response to a step input is shown in figure 4-5, and the AC results are shown in figure 4-6.

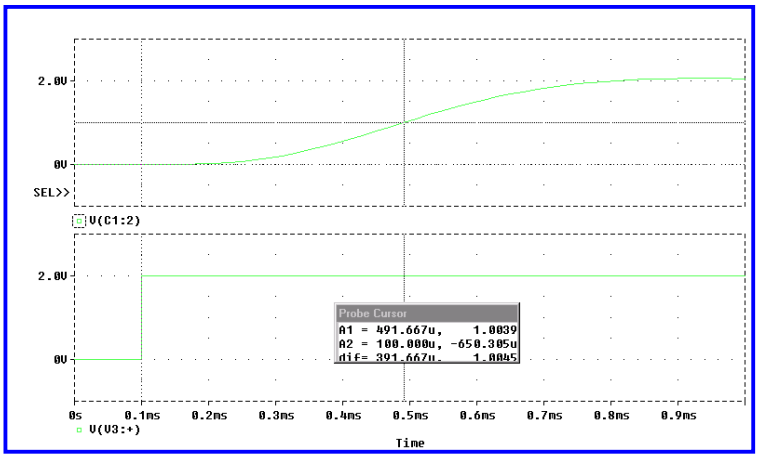


Figure 4-5: Pspice filter response to step input

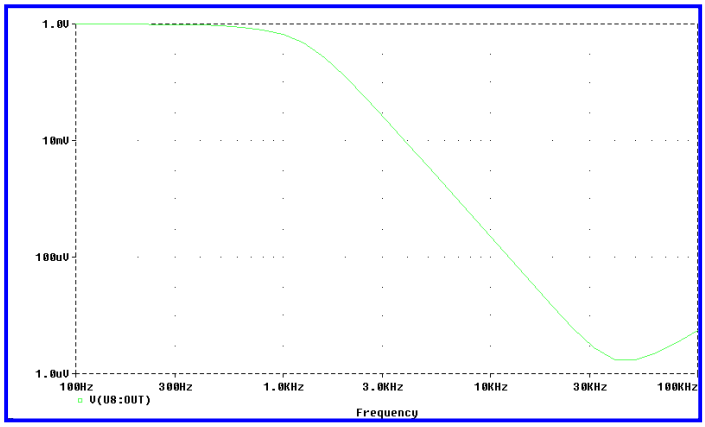


Figure 4-6: Pspice AC filter response

Micro-cap V also had an LM124 model. The model response to a step input is shown as figure 4-7, and the AC results are shown as figure 4-8.

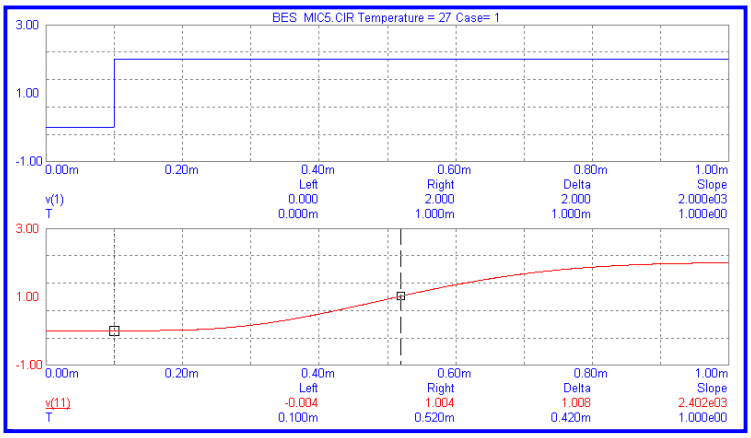


Figure 4-7: Microcap filter response to step input

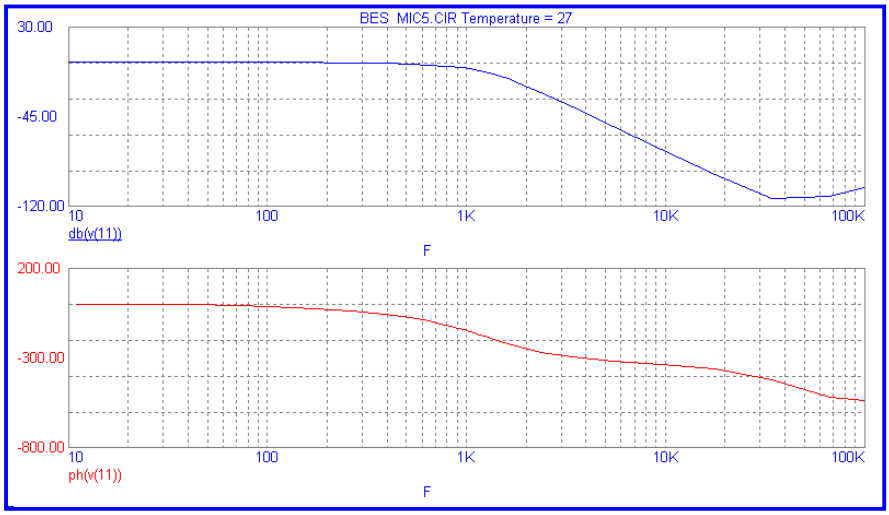
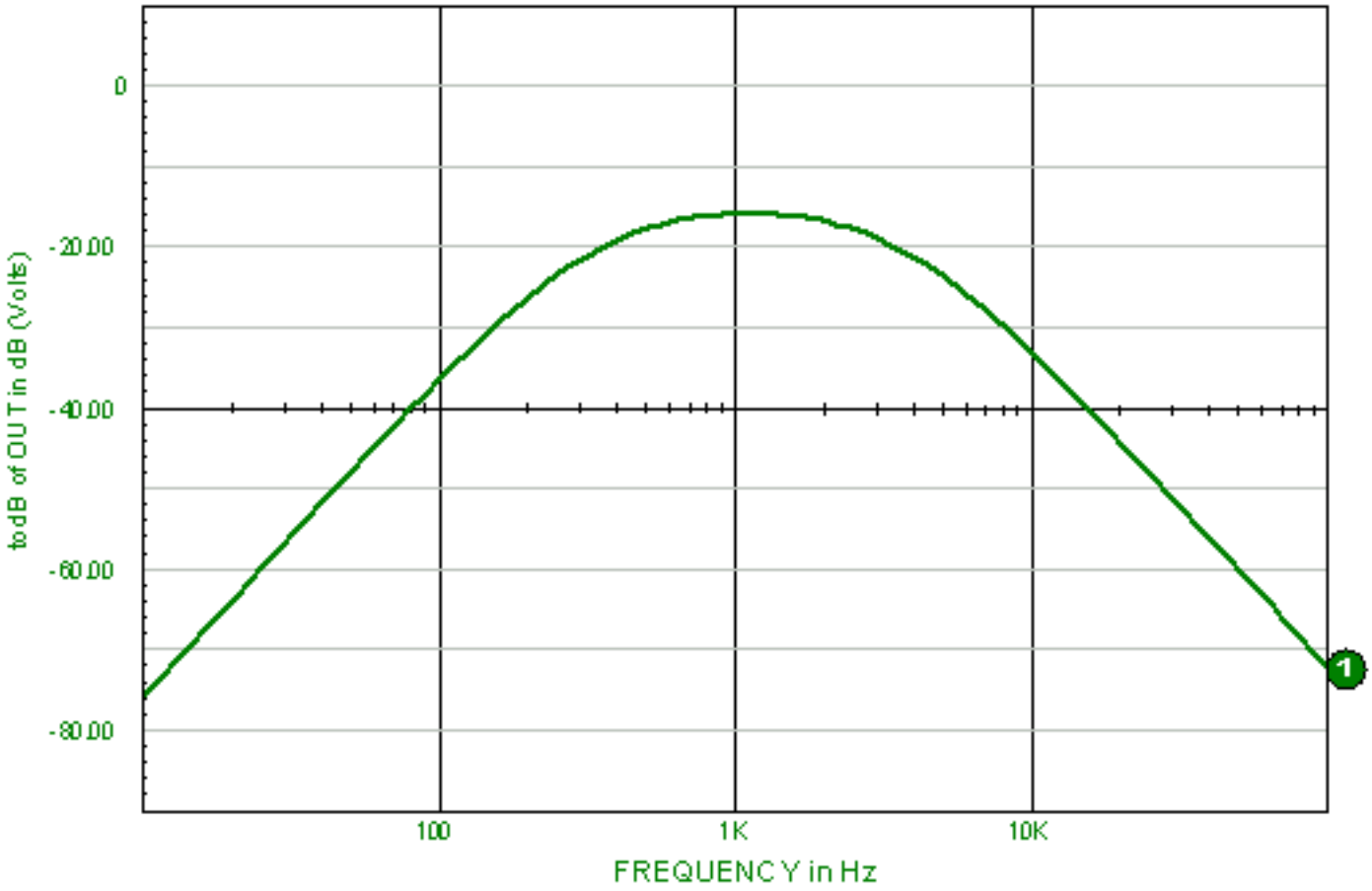


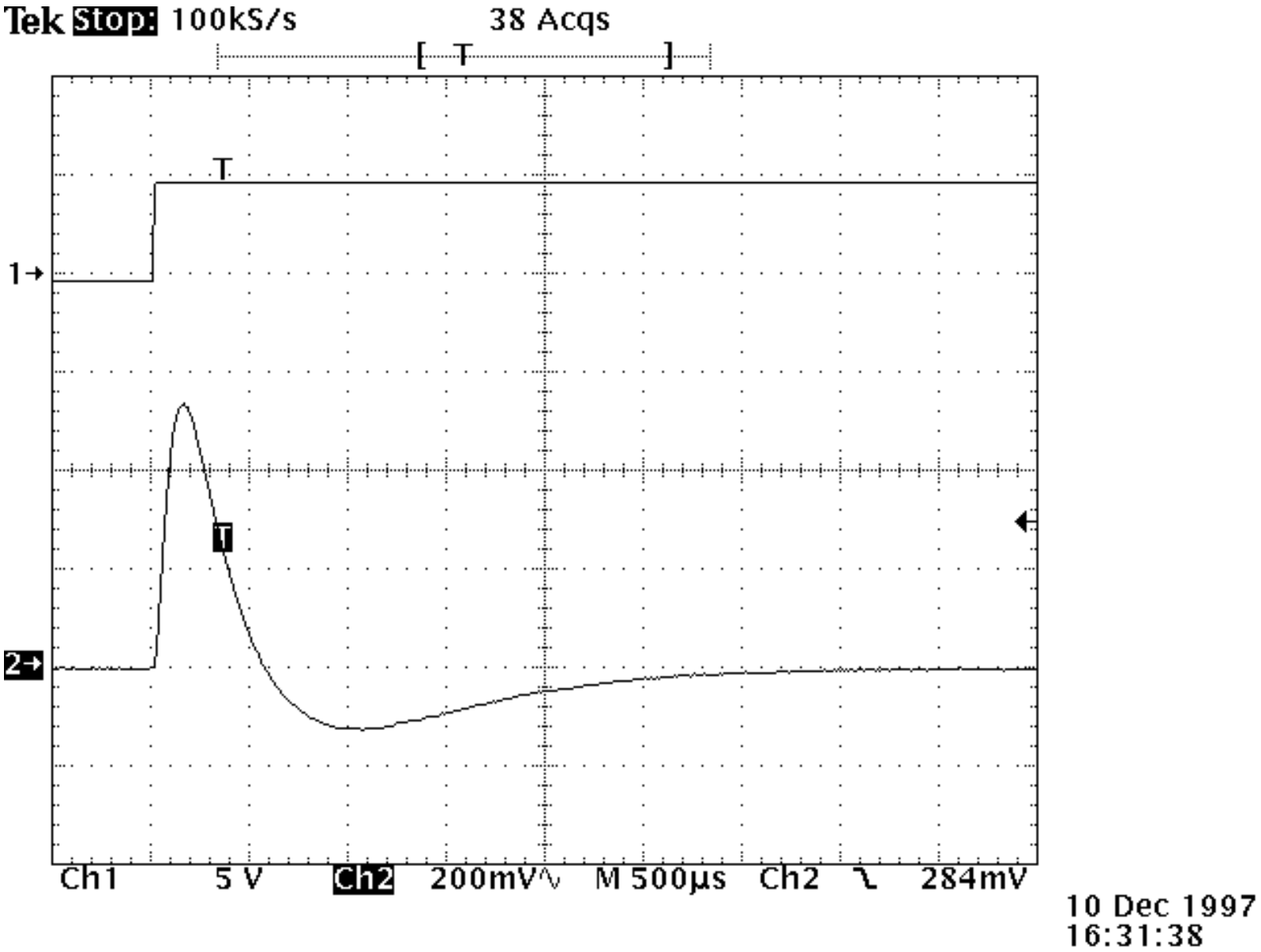
Figure 4-8: Microcap AC filter response

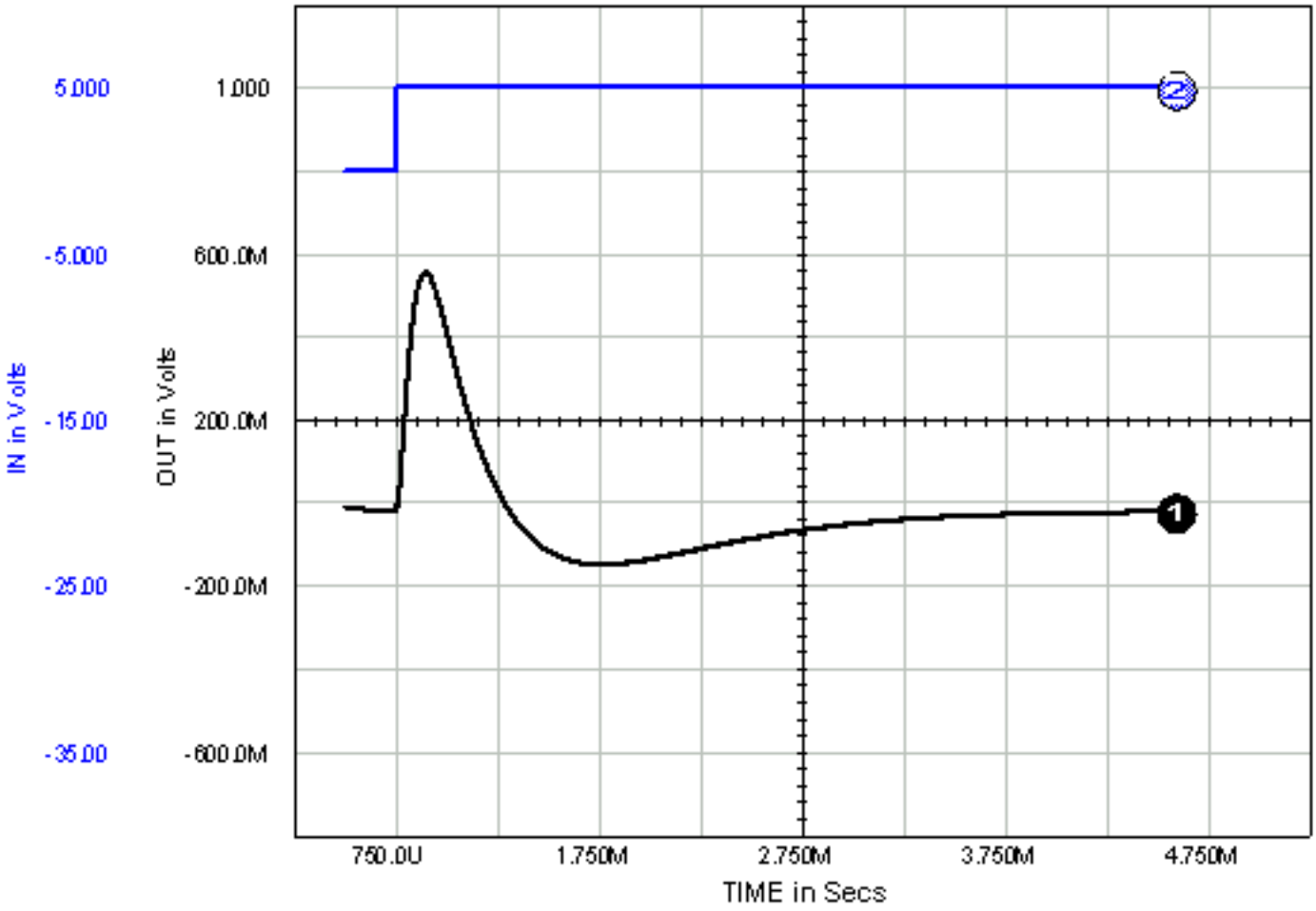
Bessel-Thompson Delay low pass filter

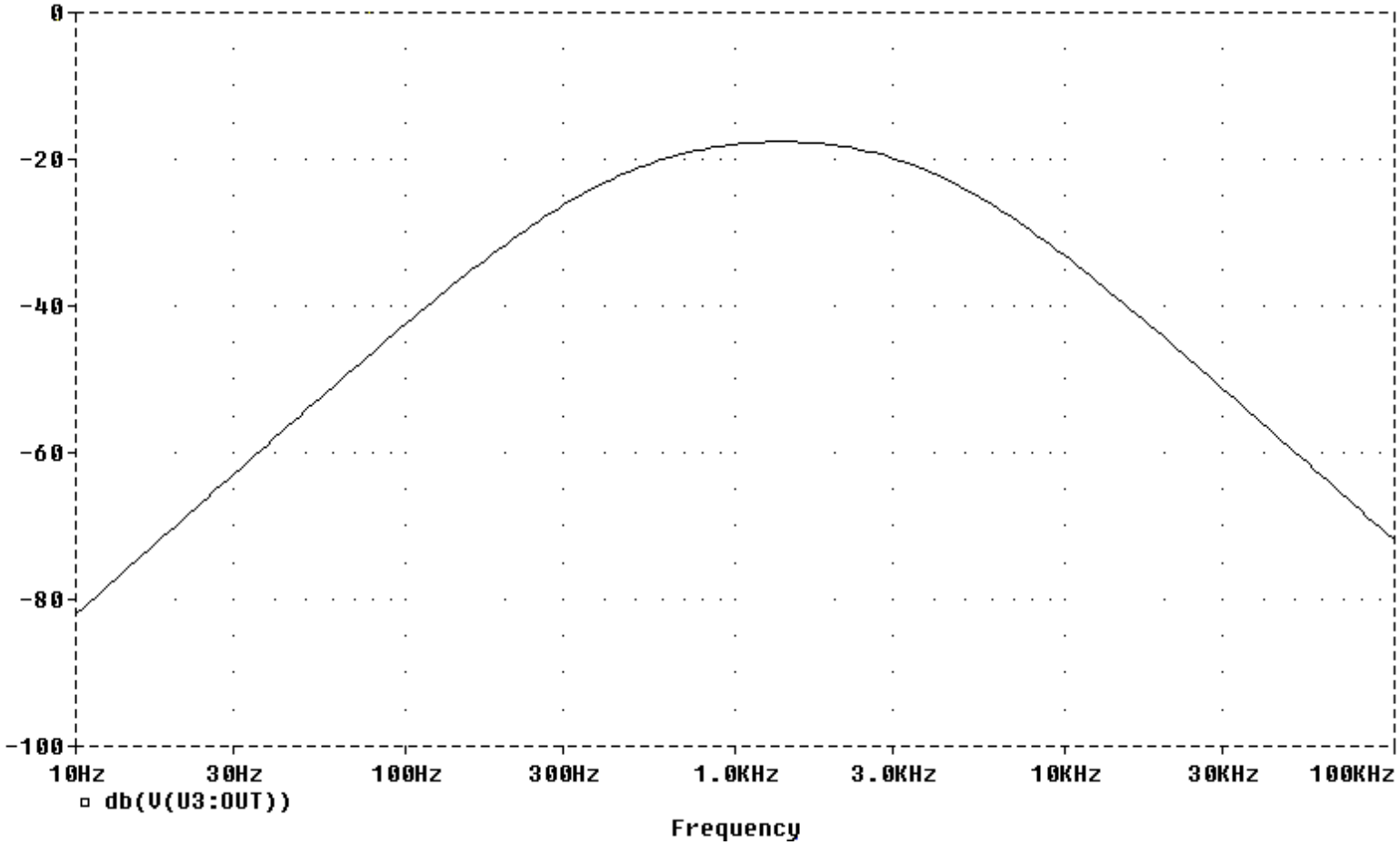
Run Time Summary		
IsSpice v 7.6	PsPice v 6.3	Micro-Cap V v2
5.6 Sec	2.37 Sec	16.5 Sec
Advantages: Adds controlled delay to a given signal with moderate parts count.		
Disadvantages: Rounds off signal and places importance on detection device.		

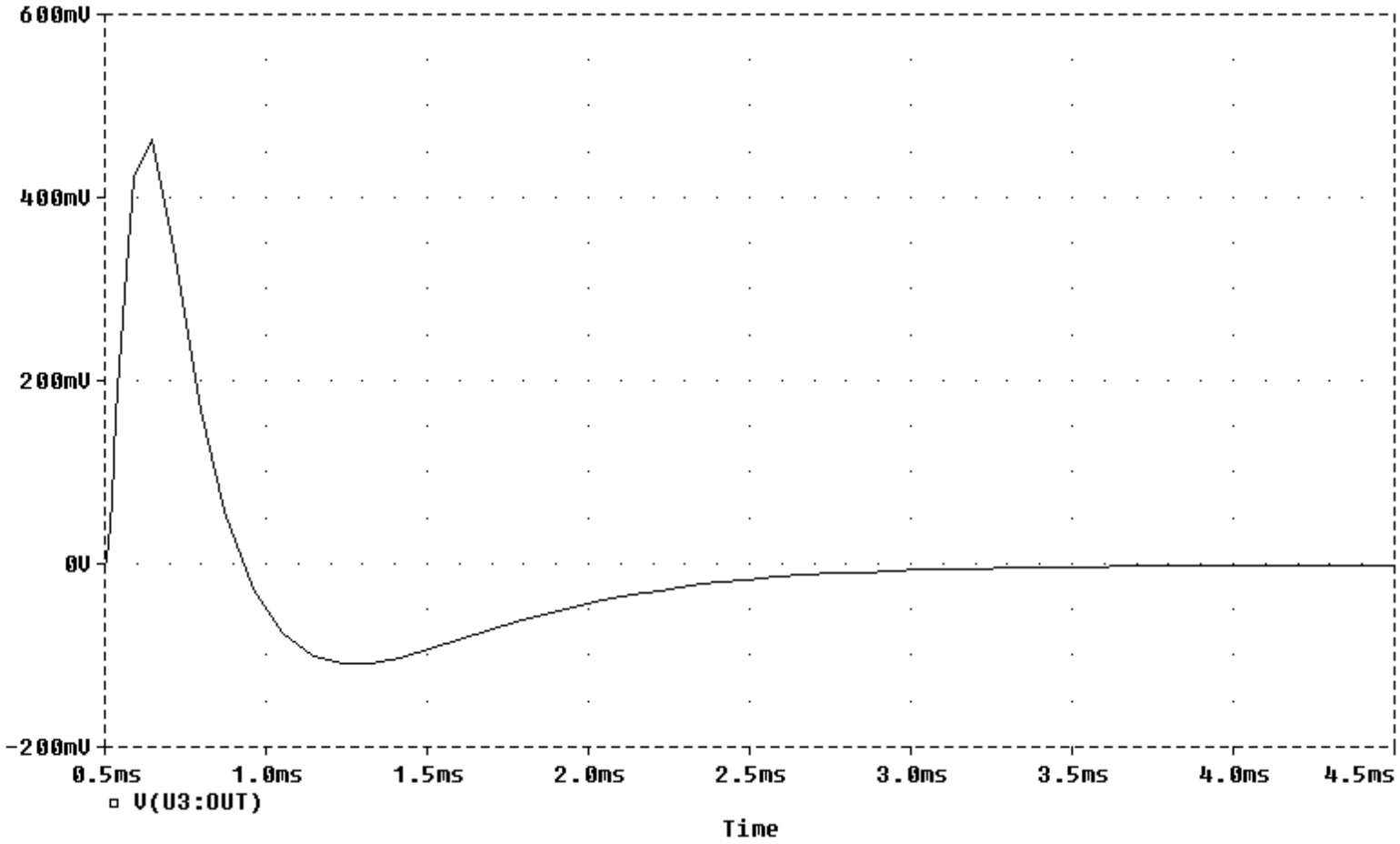
Filenames: bessel (IsSpice) besmc5 (Micro-cap) bes_ps (Pspice)

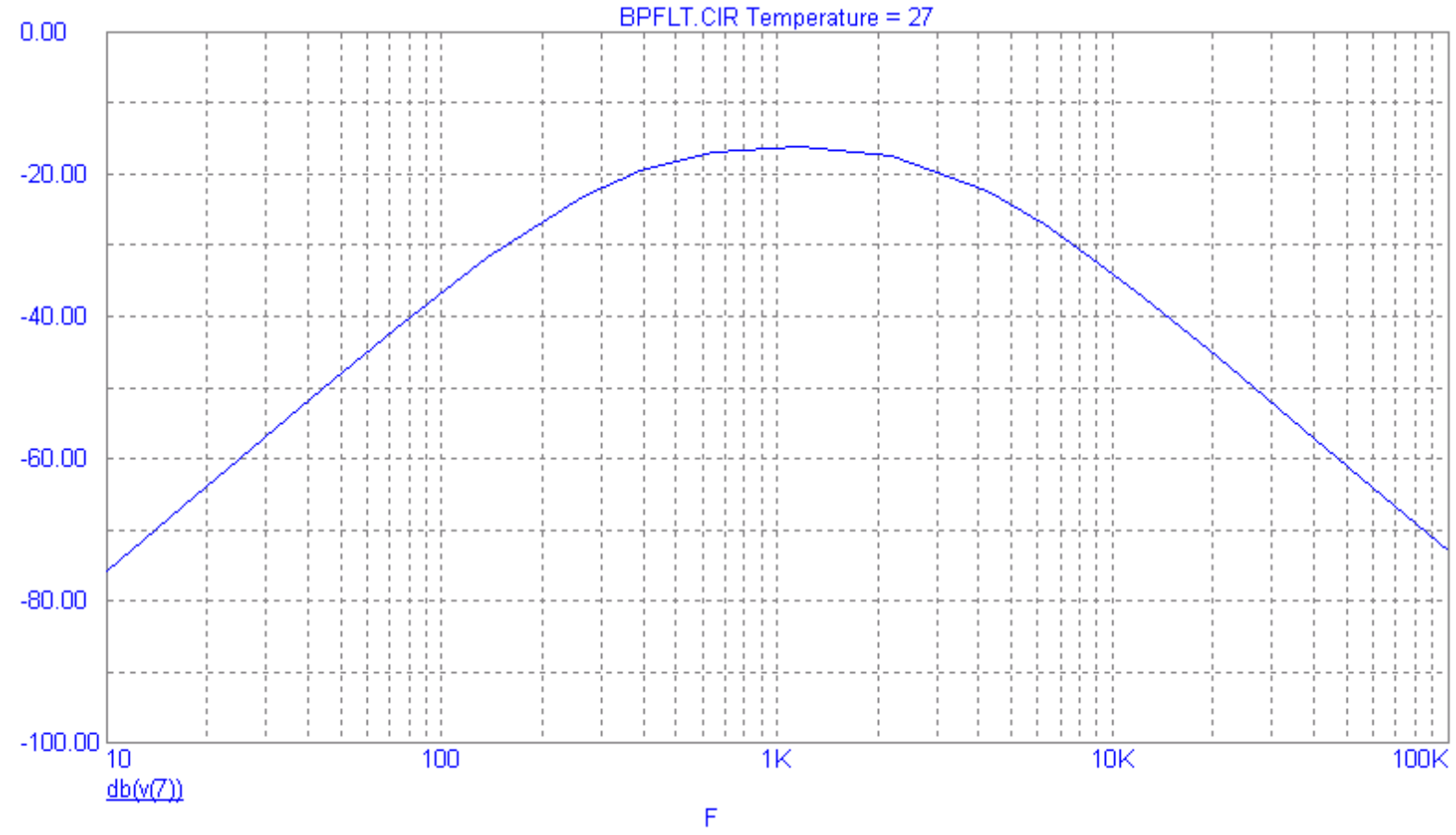

0
-20.00
-40.00
-60.00
-80.00
toDB of OUT in dB (Volts)
100
1K
10K
FREQUENCY in Hz
1

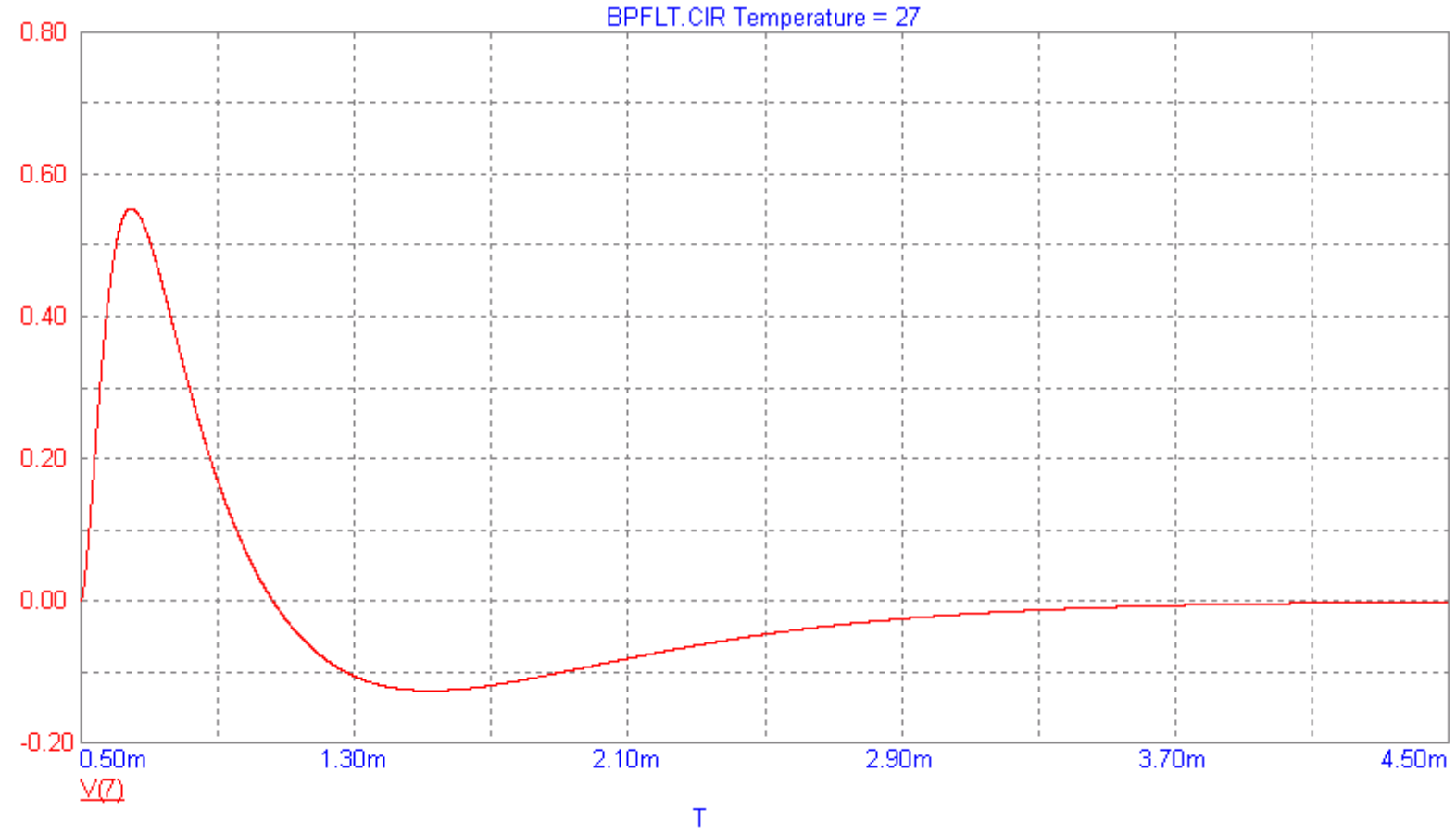

Tek Stop: 100kS/s
38 Acqs
[T]
T
1→
T
2→
Ch1 5 V
Ch2 200mV
M 500µs
Ch2 284mV
10 Dec 1997
16:31:38


5.000
-5.000
-15.00
-25.00
-35.00
IN in Volts
1.000
600.0M
200.0M
-200.0M
-600.0M
OUT in Volts
750.0U
1.750M
2.750M
3.750M
4.750M
TIME in Secs
2
1


0
-20
-40
-60
-80
-100
10Hz
30Hz
100Hz
300Hz
1.0KHz
3.0KHz
10KHz
30KHz
100KHz
db(V(U3:OUT))
Frequency


600mV
400mV
200mV
0V
-200mV
0.5ms
1.0ms
1.5ms
2.0ms
2.5ms
3.0ms
3.5ms
4.0ms
4.5ms
V(U3:OUT)
Time


BPFLT.CIR Temperature = 27
0.00
-20.00
-40.00
-60.00
-80.00
-100.00
10
100
1K
10K
100K
db(v(7))
F


BPFLT.CIR Temperature = 27
0.80
0.60
0.40
0.20
0.00
-0.20
0.50m
1.30m
2.10m
2.90m
3.70m
4.50m
V(7)
T

#5: Bessel-Thompson Delay low pass filter with pulse shaper

A simple pulse shaping modification can be added to the Bessel-Thompson delay filter using an additional operational amplifier. Using resistors to divide down the supply voltage to half the output voltage of the delay filter, then comparing it to the delay filters response results in a time delayed square wave. The schematic of this circuit is shown in figure 5-1. This simulation also allows us to compare the operational amplifier models that came with each software package. The response of this circuit is driven from rail to rail providing the saturation voltages of the models. Also the slew rate of the output should be consistent with the measured and published data. Keep in mind that these parameters may not be consistent between brands and between lots, and they should be consistent with the average data from the manufacturer designed after.

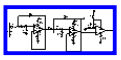


Figure 5-1: Bessel-Thompson delay filter with shape reformation

The parameters that will be measured in each of the software packages and the hardware are the minimum and maximum voltages, the rise and fall time of the output, and the effective pulse width. The results of the IsSpice model is shown as figure 5-2. Micro-cap V results are shown as figure 5-3. The Pspice results are displayed as figure 5-4, and the hardware measurements are shown as figure 5-5.

Bessel-Thompson Delay low pass filter with pulse shaper

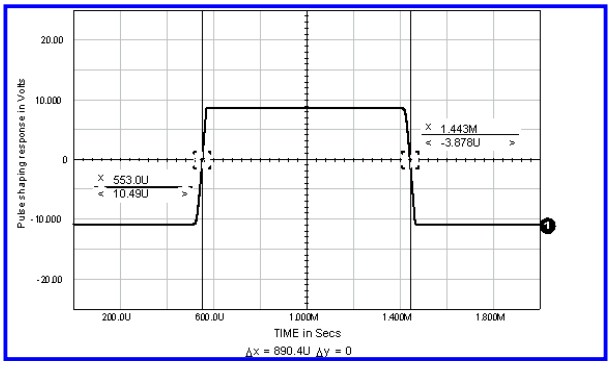


Figure 5-2: IsSpice simulation results

Note:Outmax=8.4, Outmin=-10.7, Rise time=53.3u, fall time=53.3u, pulse width=890u

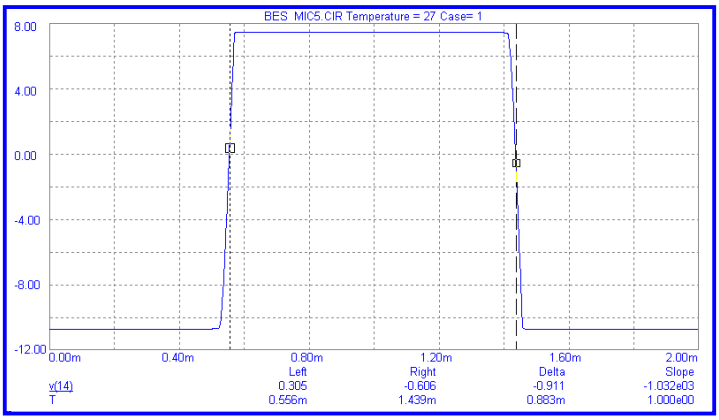


Figure 5-3: Microcap simulation results

Note: Outmax=7.4, Outmin=-10.7, Rise time=49u, fall time=52u, pulse width=833u:

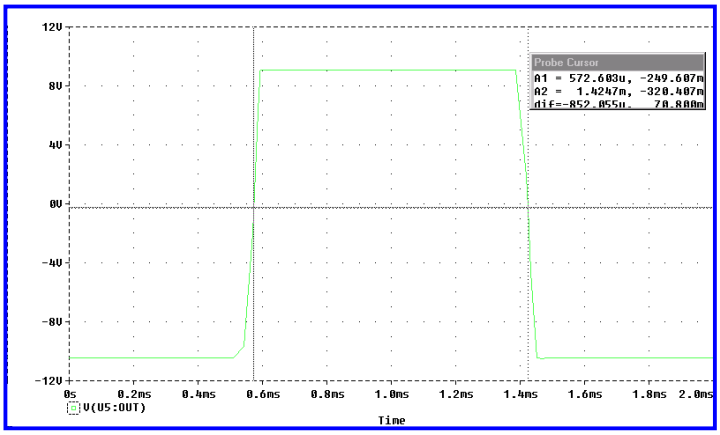


Figure 5-4: Pspice simulation results

Note: Outmax=9.08, Outmin=-10.47, Rise time=84u, fall time=71u, pulse width=851u:

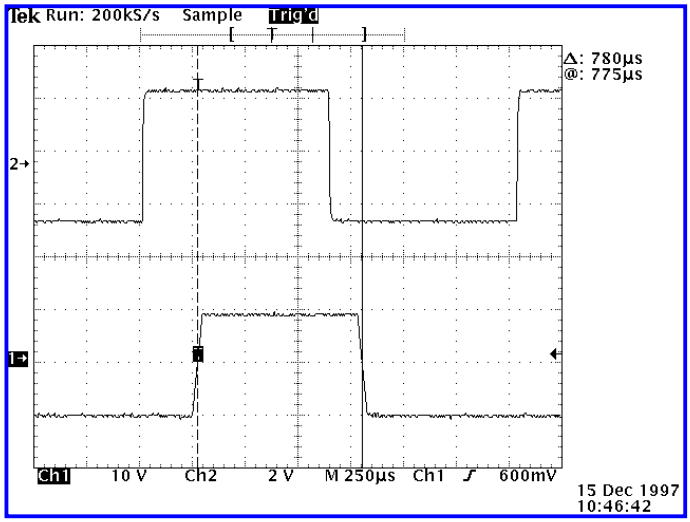
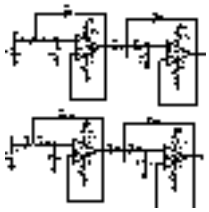


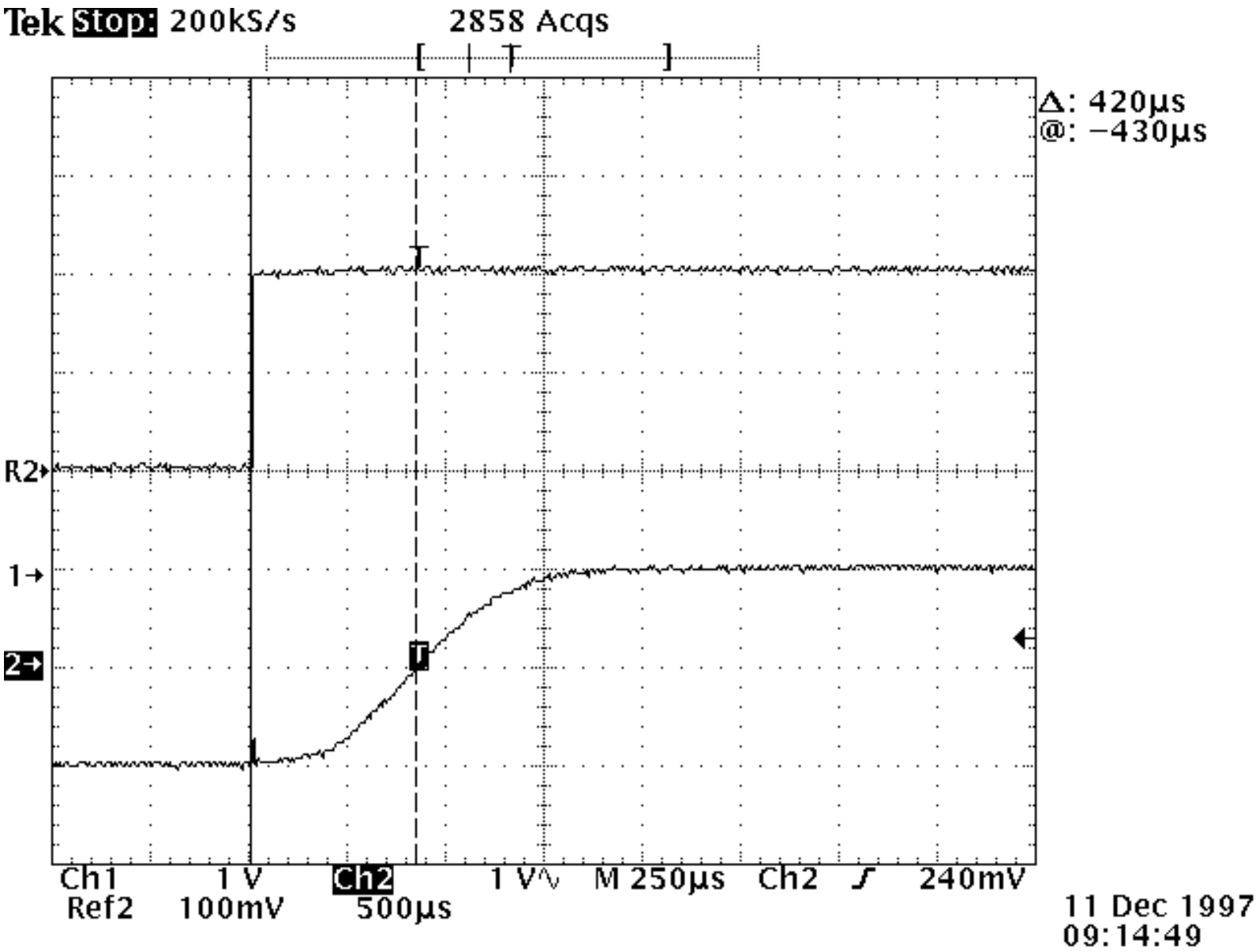
Figure 5-5: Breadboard data

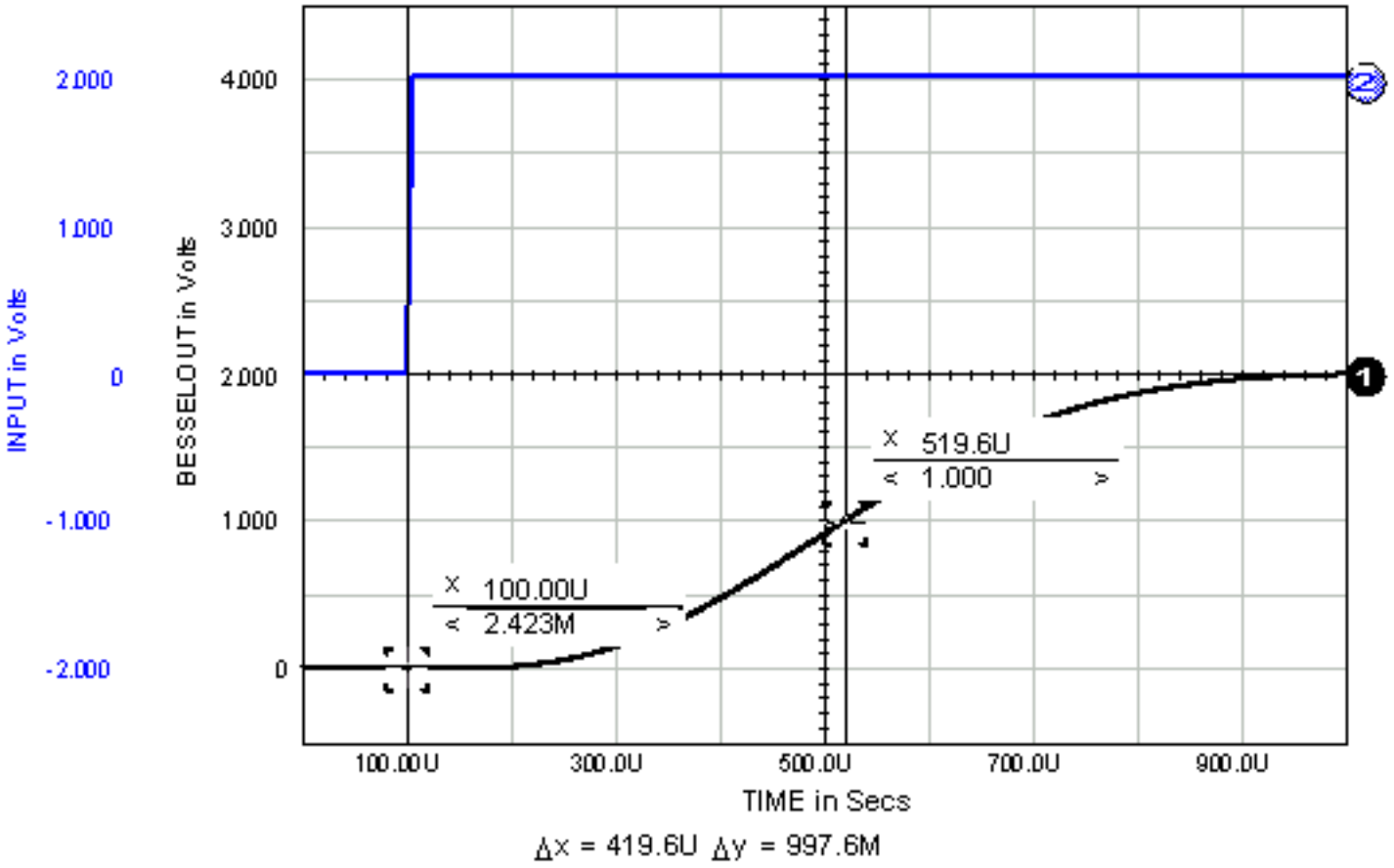
Note: Outmax=9.1, Outmin=-10, Rise time=49u, fall time=50u, pulse width=780u:

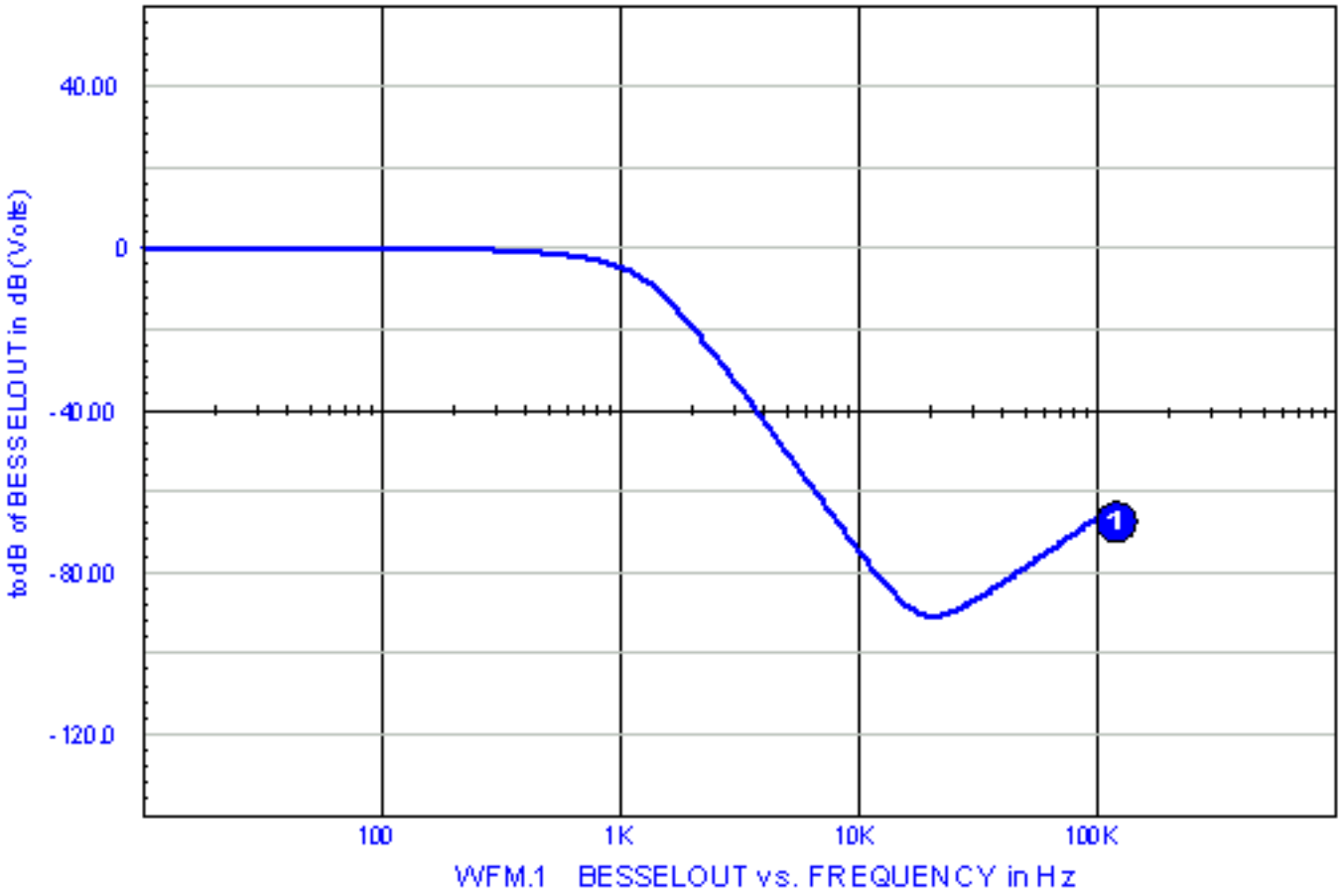
Run Time Summary		
IsSpice v 7.6	PsPice v 6.3	Micro-Cap V v2
38.6 Sec	2.05 Sec	67.4 Sec
Advantages: Moderate part count pulse delay and reshaper		
Disadvantages: May require additional voltage source and opamp package to reshape voltage to a specification.		

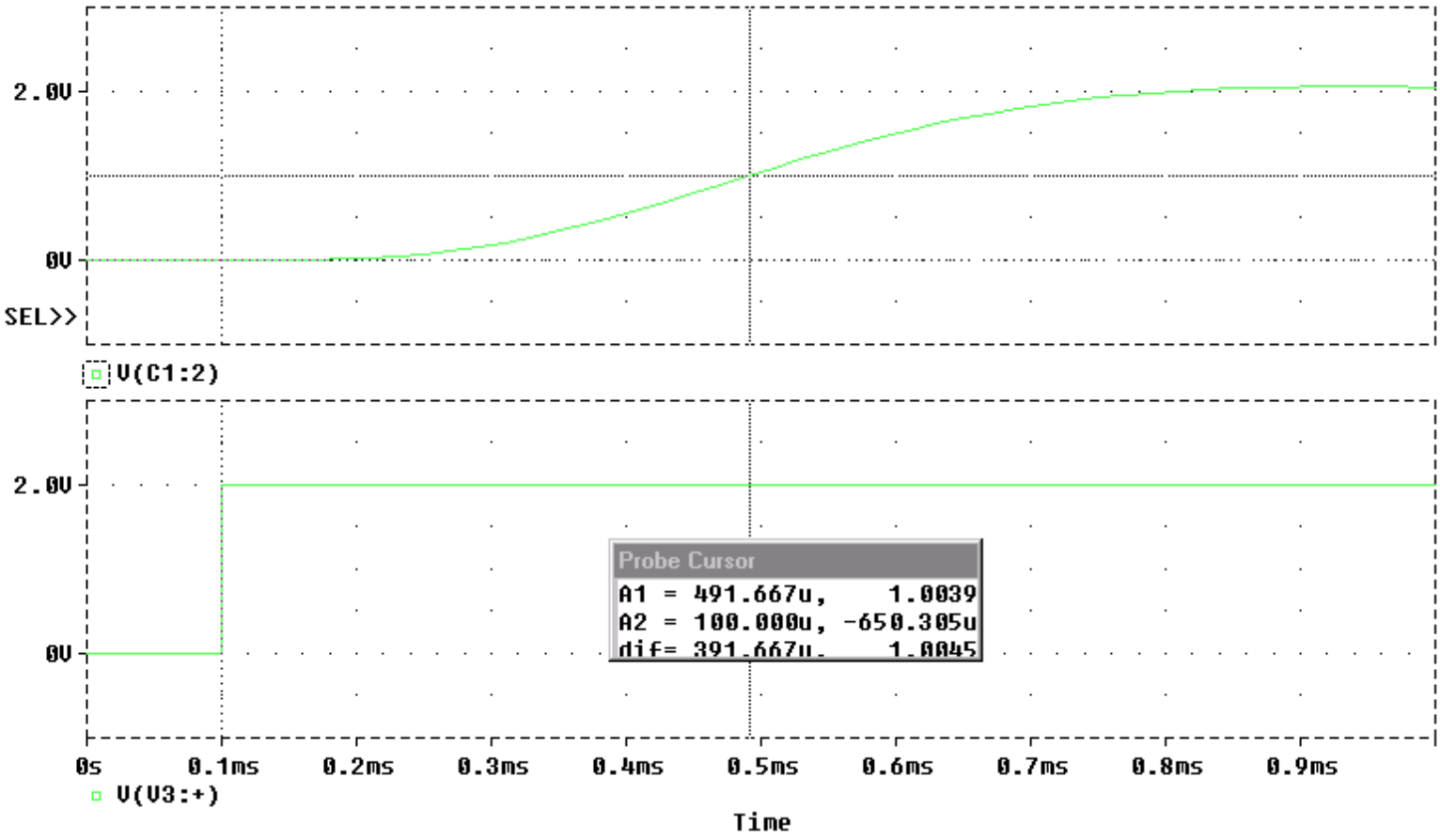
Filenames: bessel (IsSpice) bes_mic5 (Micro-cap) bes_ps (Pspice)

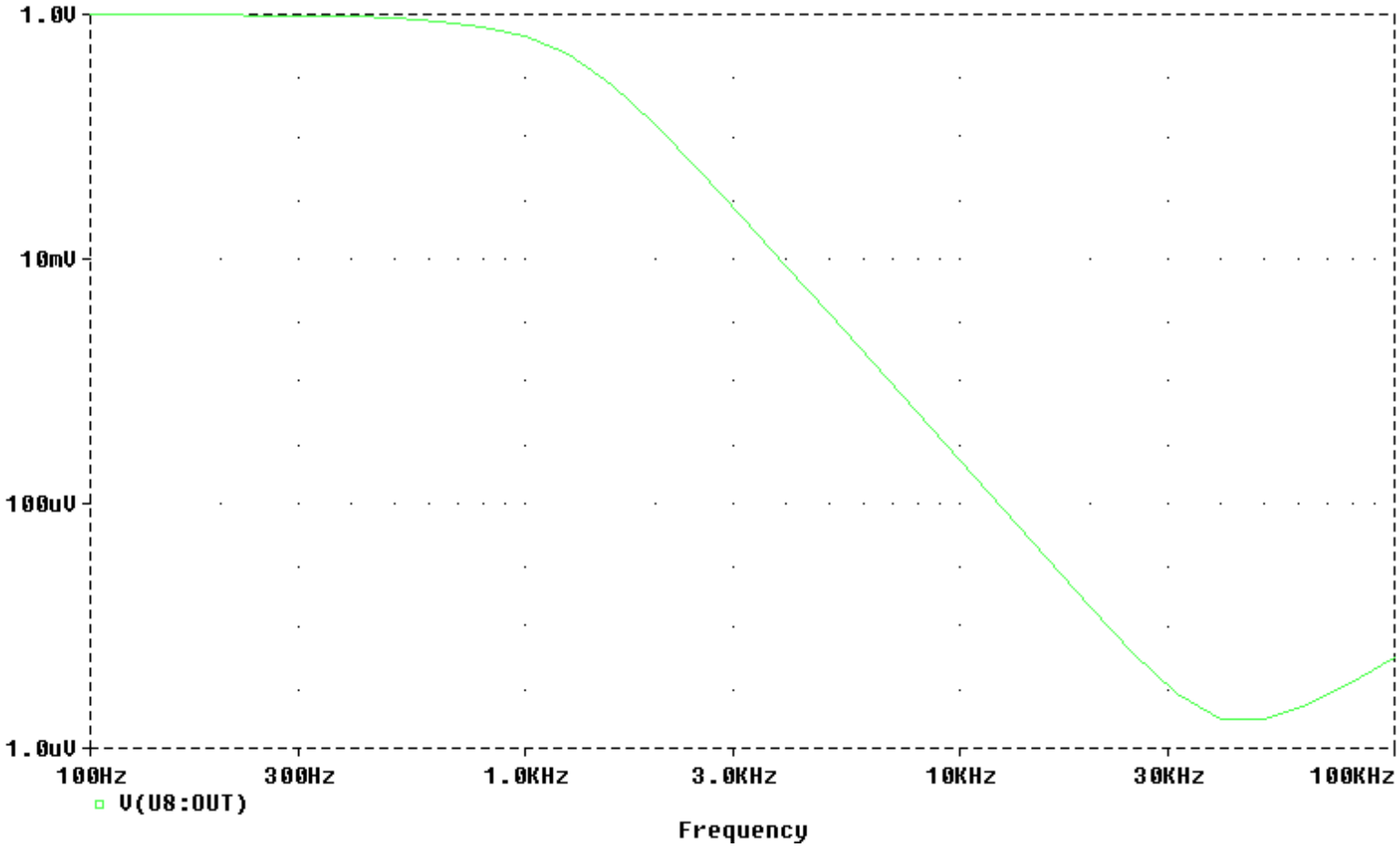


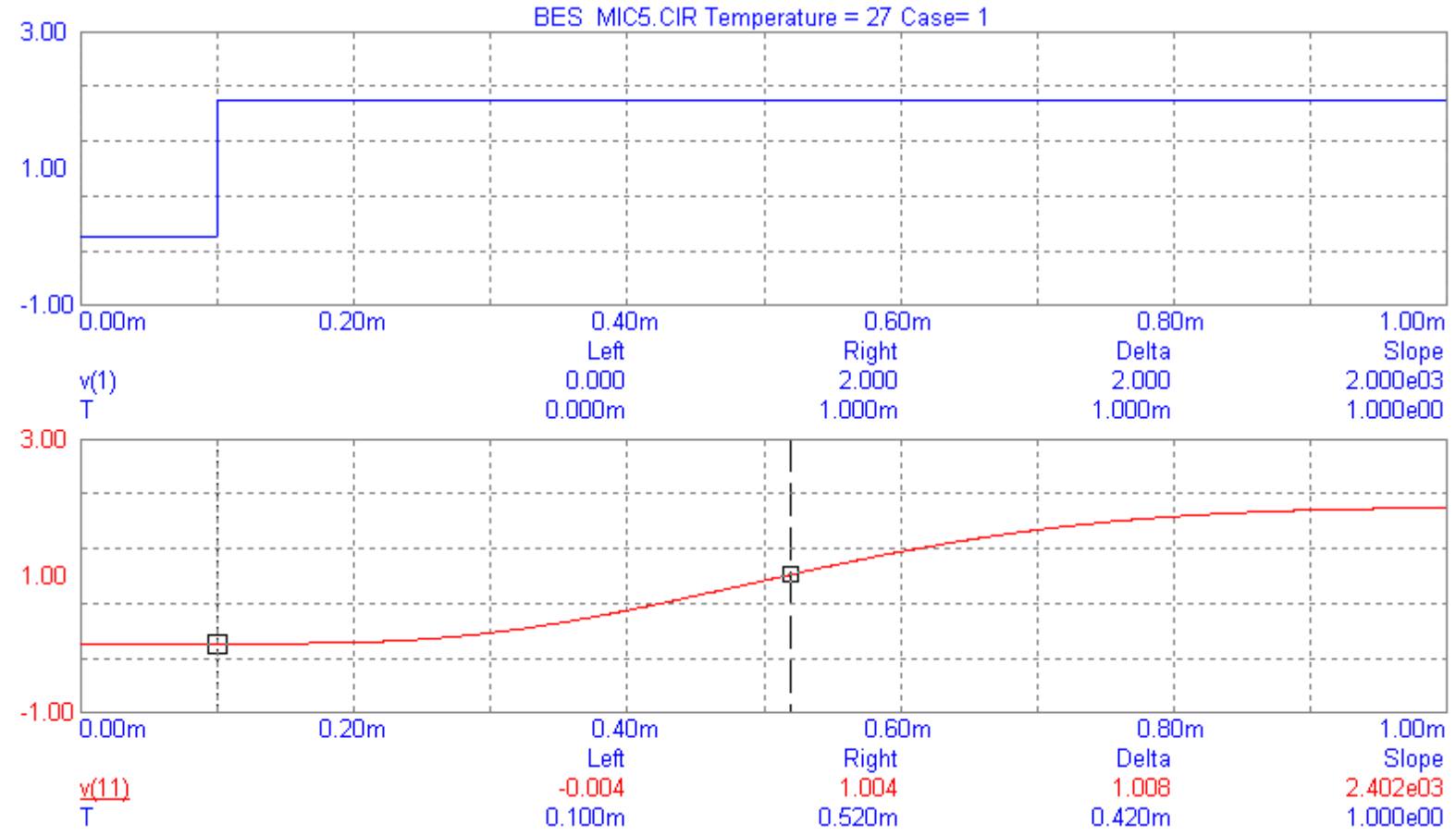

Tek Stop: 200kS/s
2858 Acqs
Δ: 420µs
@: −430µs
R2
1
2
Ch1 1 V
Ch2
1 V
M 250µs Ch2 240mV
Ref2 100mV
500µs
11 Dec 1997
09:14:49

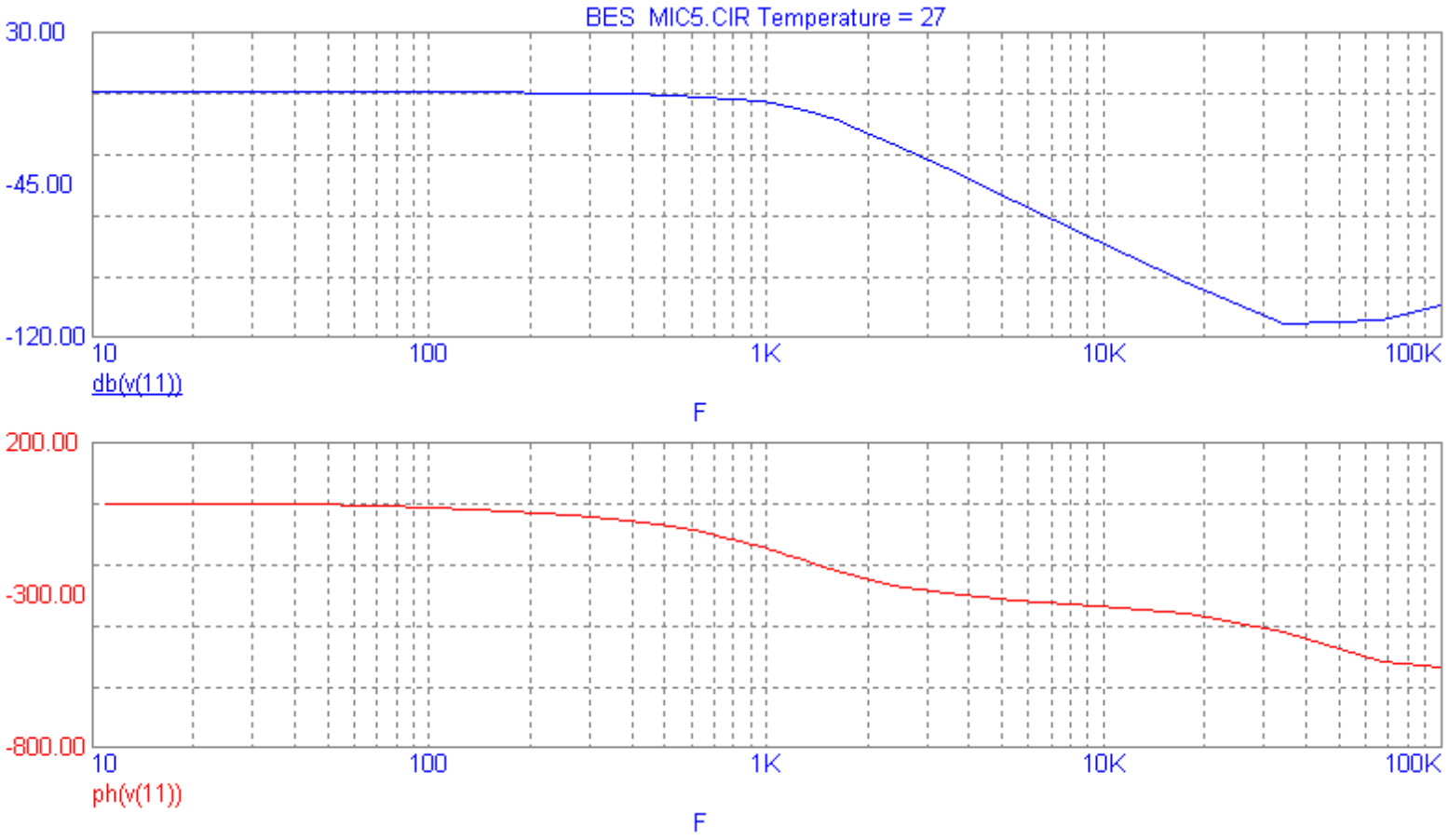

2.000
1.000
0
-1.000
-2.000
INPUT in Volts
4.000
3.000
2.000
1.000
0
BESSELOUT in Volts
X 519.6U
< 1.000 >
X 100.00U
< 2.423M >
100.00U
300.0U
500.0U
700.0U
900.0U
TIME in Secs
Δx = 419.6U Δy = 997.6M


40.00
0
-40.00
-80.00
-120.0
100
1K
10K
100K
1
to dB of BESSELOUT in dB (Volts)
WFM.1 BESSELOUT vs. FREQUENCY in Hz


2.0V
0V
SEL>>
V(C1:2)
2.0V
0V
Probe Cursor
A1 = 491.667u, 1.0039
A2 = 100.000u, -650.305u
dif= 391.667u, 1.0045
0s
0.1ms
0.2ms
0.3ms
0.4ms
0.5ms
0.6ms
0.7ms
0.8ms
0.9ms
V(V3:+)
Time


1.0V
10mV
100uV
1.0uV
100Hz
300Hz
1.0KHz
3.0KHz
10KHz
30KHz
100KHz
V(U8:OUT)
Frequency


BES MIC5.CIR Temperature = 27 Case= 1
3.00
1.00
-1.00
0.00m
0.20m
0.40m
0.60m
0.80m
1.00m
Left
Right
Delta
Slope
v(1)
0.000
2.000
2.000
2.000e03
T
0.000m
1.000m
1.000m
1.000e00
3.00
1.00
-1.00
0.00m
0.20m
0.40m
0.60m
0.80m
1.00m
Left
Right
Delta
Slope
v(11)
-0.004
1.004
1.008
2.402e03
T
0.100m
0.520m
0.420m
1.000e00


BES MIC5.CIR Temperature = 27
30.00
-45.00
-120.00
10
100
1K
10K
100K
db(v(11))
F
200.00
-300.00
-800.00
10
100
1K
10K
100K
ph(v(11))
F

#6: Inverted Bessel-Thompson Delay High pass filter

A quick modification to the Bessel-Thompson filter leaves us with a high pass filter. This filter does not have the built in delay like the low pass version, but it does provide an interesting response. The schematic and the breadboard results are shown in figure 6-1 and figure 6-2 respectively. The measurements that will be made for comparison purposes are the step response height and the time until the second cross of the zero axis.

Figure 6-1: High pass filter inverse Bessel-Thompson

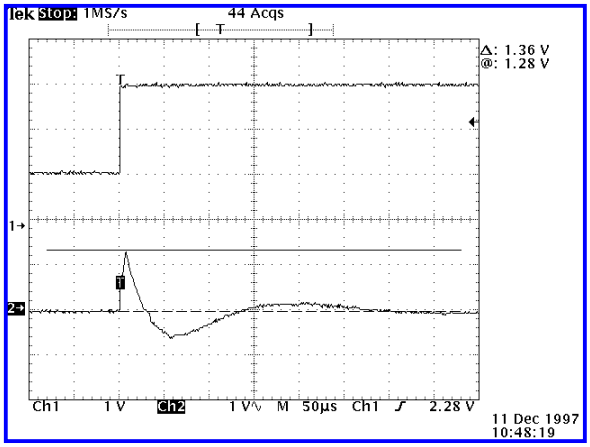


Figure 6-2: Breadboard results of step response

For each filter an AC analysis was run for comparison between the different software packages. These results are displayed along with the step response from each of the filters for comparison between the software packages. The results of the IsSpice model are displayed as figure 6-3 and figure 6-4. The Pspice results are shown as figure 6-5 and figure 6-6. The results from the Microcap model are shown as figure 6-7 and figure 6-8.

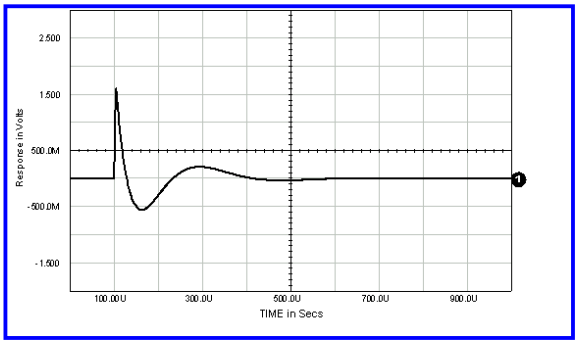


Figure 6-3: IsSpice results of step response

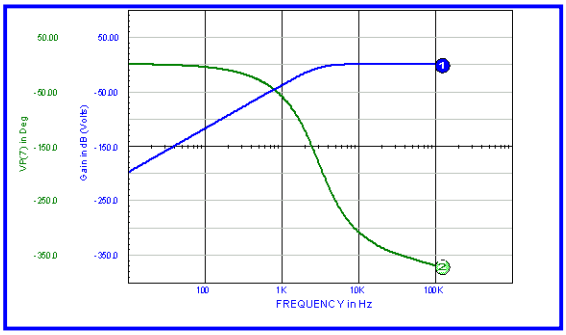


Figure 6-4: IsSpice AC filter response

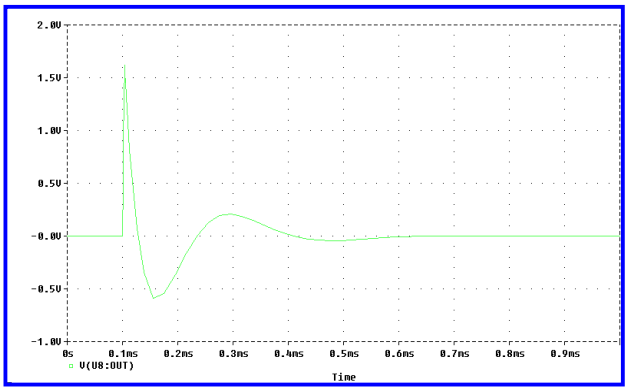


Figure 6-5: Pspice results of step response

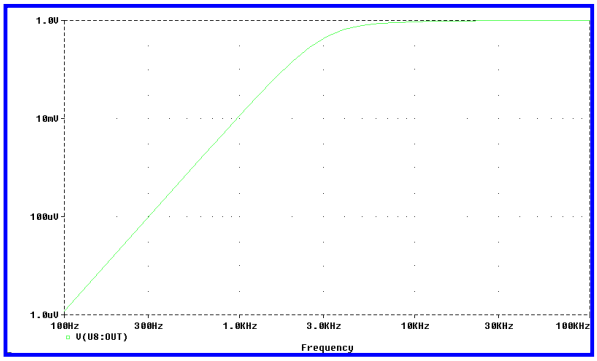


Figure 6-6: Pspice AC filter response

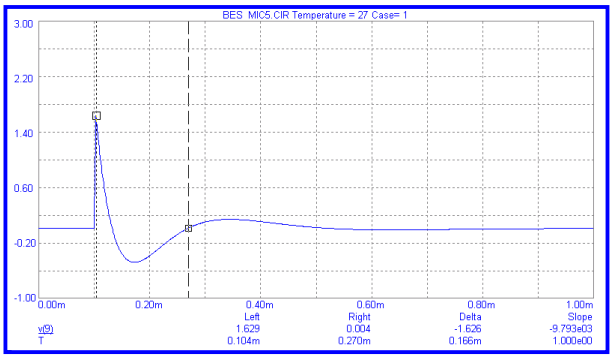


Figure 6-7: Microcap results of step response

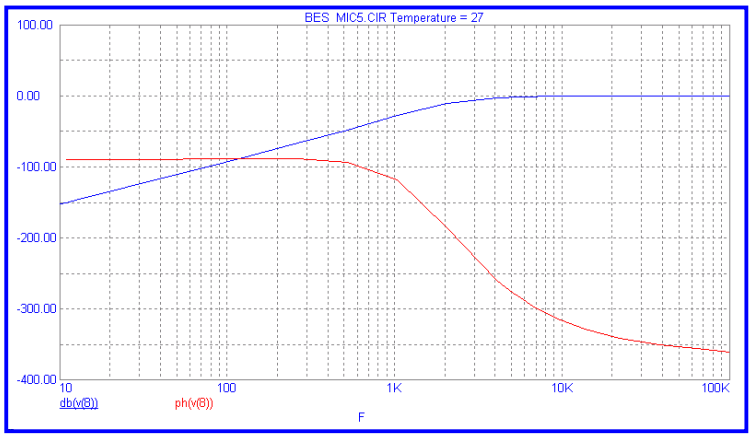


Figure 6-8: Microcap AC filter response

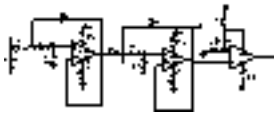
Run Time Summary		
IsSpice v 7.6	PsPice v 6.3	Micro-Cap V v2
2.25 Sec	1.01 Sec	18.8 Sec
Advantages: Moderate parts count		
Disadvantages: Under damped response.		

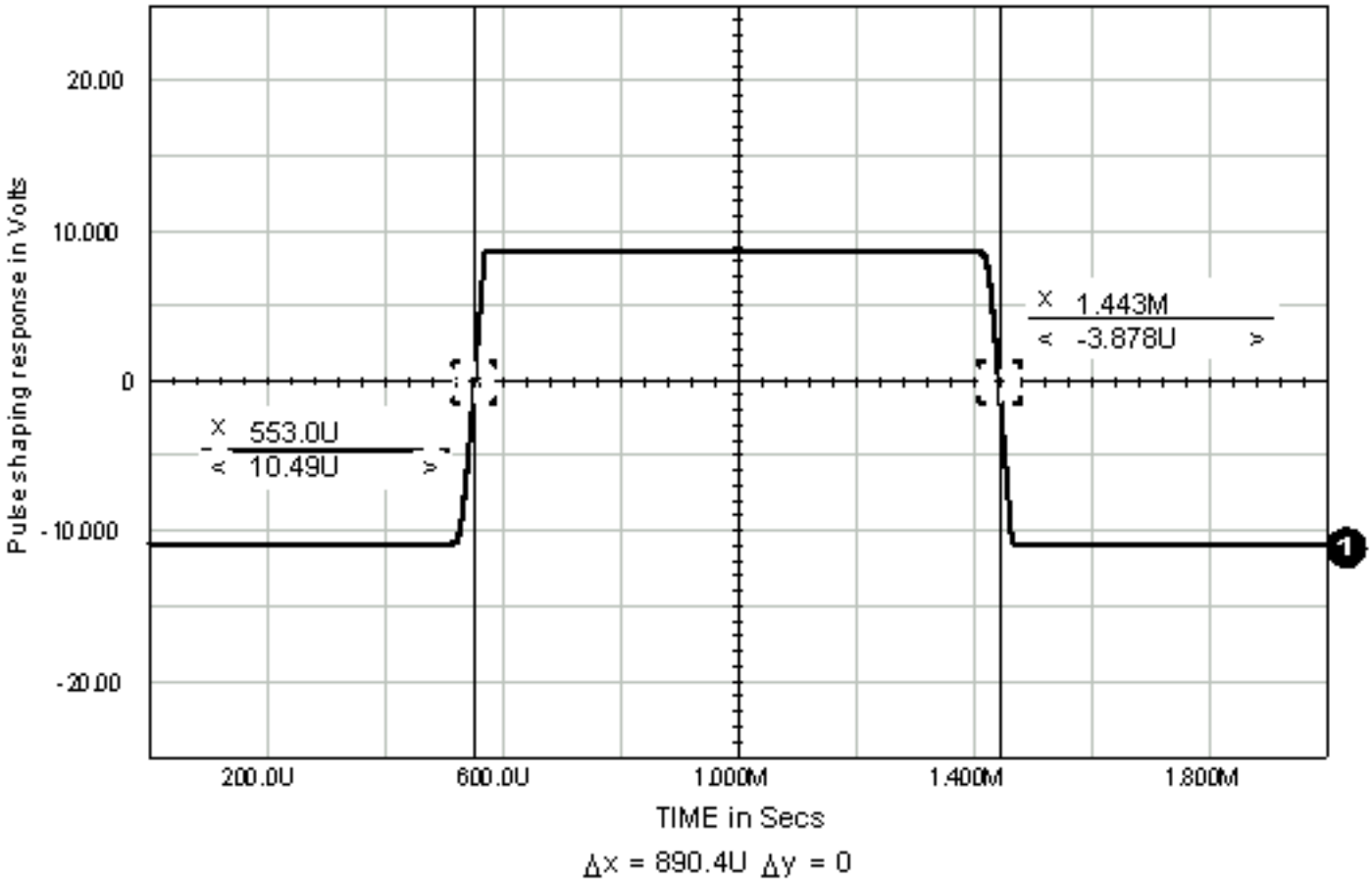
Filenames: hpbessel (IsSpice) bes_mic5 (Micro-cap) bes_ps (Pspice)

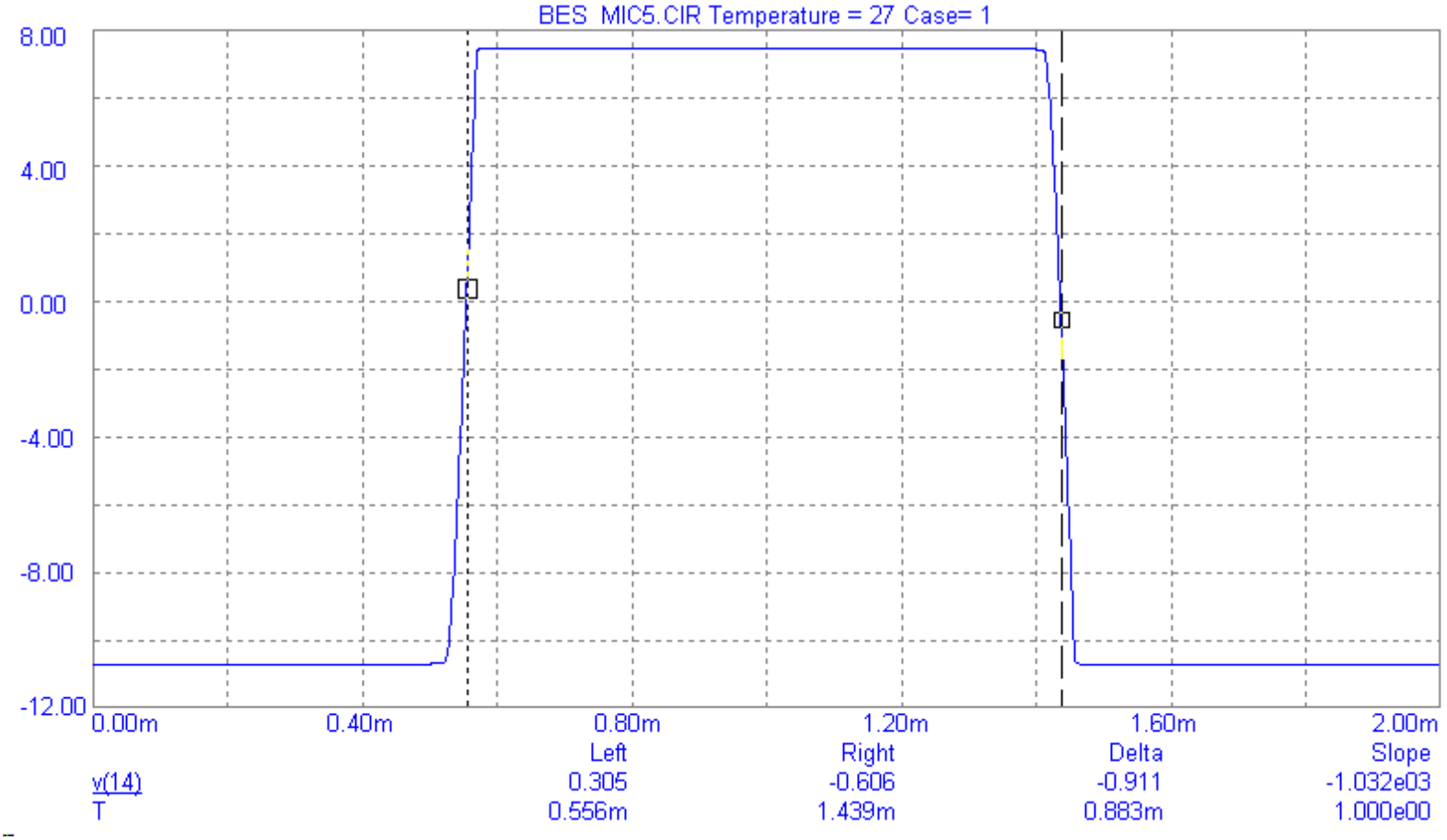
References

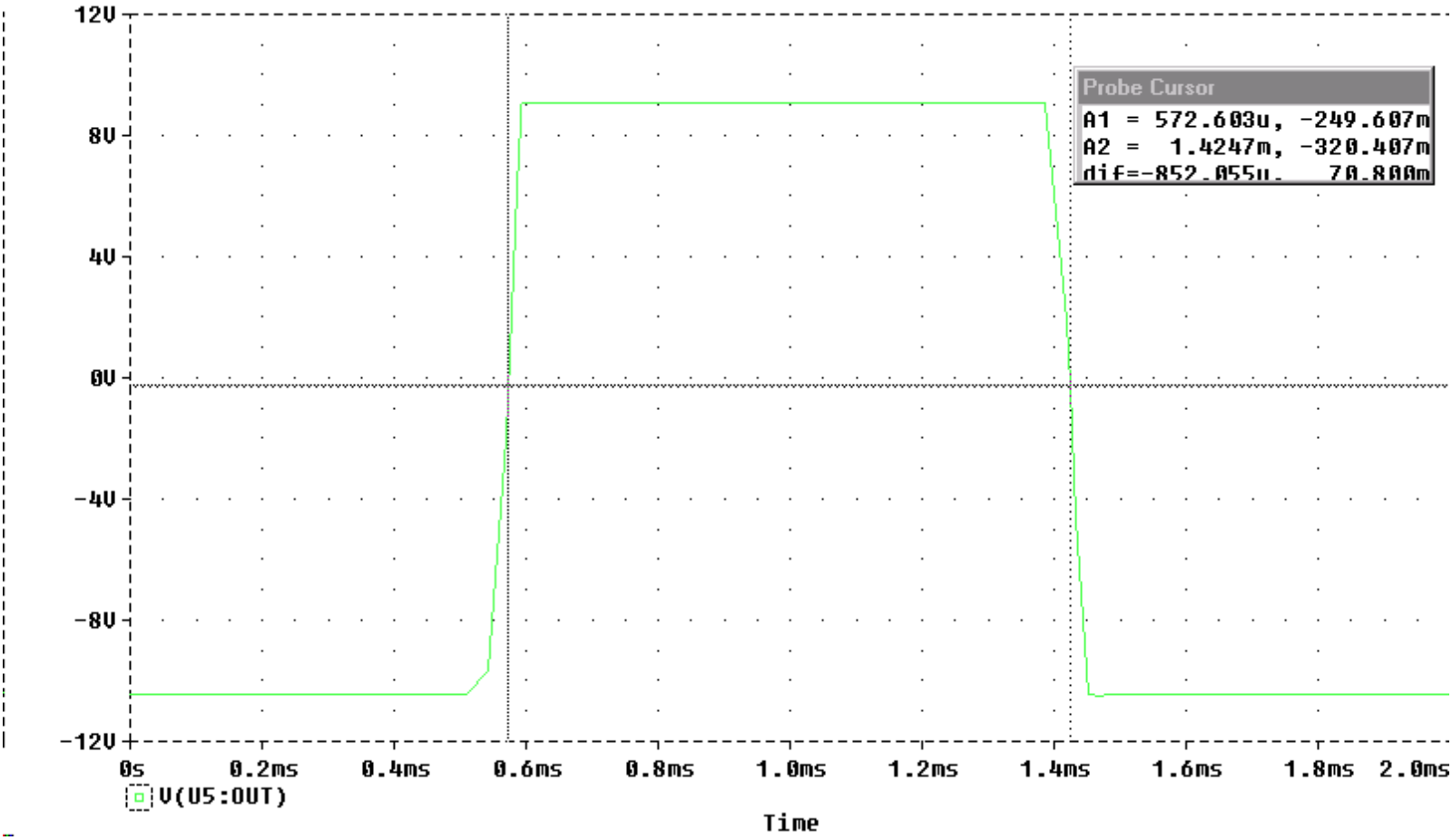
Parker, Sybil, ed. 1984. Concise Encyclopedia of Science and Technology. New York: McGraw Hill

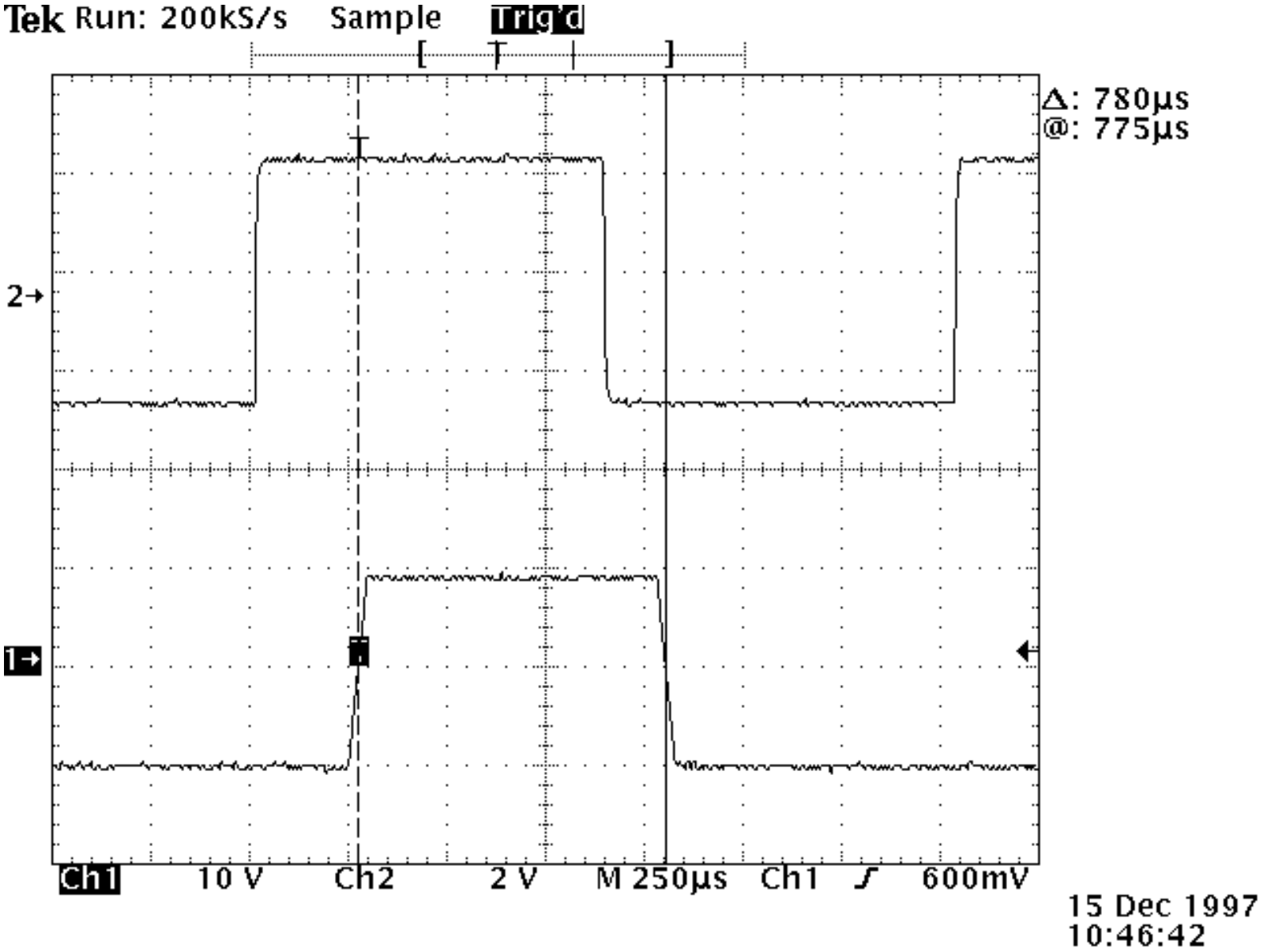
Van Valkenburg, M.E. 1982. Analog Filter Design. New York: Harcort Brace Jovanovich College Publishers.




20.00
10.000
0
-10.000
-20.00
Pulse shaping response in Volts
X 553.0U
< 10.49U >
X 1.443M
< -3.878U >
1
200.0U
600.0U
1.000M
1.400M
1.800M
TIME in Secs
Δx = 890.4U Δy = 0


BES MIC5.CIR Temperature = 27 Case= 1
8.00
4.00
0.00
-4.00
-8.00
-12.00
0.00m
0.40m
0.80m
1.20m
1.60m
2.00m
Left
Right
Delta
Slope
v(14)
0.305
-0.606
-0.911
-1.032e03
T
0.556m
1.439m
0.883m
1.000e00


12V
8V
4V
0V
-4V
-8V
-12V
0s
0.2ms
0.4ms
0.6ms
0.8ms
1.0ms
1.2ms
1.4ms
1.6ms
1.8ms
2.0ms
V(U5:OUT)
Time
Probe Cursor
A1 = 572.603u, -249.607m
A2 = 1.4247m, -320.407m
dif=-852.855u, 70.800m


Tek Run: 200kS/s Sample Trig'd
Δ: 780µs
@: 775µs
2→
1→
Ch1 10 V Ch2 2 V M 250µs Ch1 ƒ 600mV
15 Dec 1997
10:46:42

#7: Chebyshev Bandpass Filter

The Chebyshev filter response offers higher attenuation and a steeper roll-off near the cutoff frequency, than the Butterworth filter response. There is a tradeoff to achieve the higher attenuation. The cost of utilizing a Chebyshev filter is higher values of Q, which leads to difficulties in hardware realization, and nonlinear phase characteristics, which can result in difficulties in predicting circuit performance. The following Mathcad file was used to design a Chebyshev bandpass filter with unity gain in the passband. A friend circuit was used in each stage of the filter.

Design specifications in rad/sec, where rad/sec=2π*Hz:

$\omega_2 := 29502 \cdot \pi$

$\omega_4 := 35002 \cdot \pi$

$\alpha_{max} := .5$

$\omega_1 := 20502 \cdot \pi$

$\omega_3 := 15002 \cdot \pi$

$\alpha_{min} := 22$

$\omega_0^2 = \omega_1 \omega_2$

$\omega_0 := \sqrt{\omega_1 \cdot \omega_2}$

$\omega_{0freq} := \frac{\omega_0}{2 \cdot \pi}$

$bw := \omega_2 - \omega_1$

$$q_c = \frac{\omega_0}{bw}$$

$$q_c := \frac{\omega_0}{\omega_2 - \omega_1}$$

$$\Omega_s := \frac{\omega_4 - \omega_3}{\omega_2 - \omega_1}$$

$$\Omega_p := -\left[\frac{-\left(\omega_2^2\right) + \omega_0^2}{\omega_2 \cdot \left(\omega_2 - \omega_1\right)}\right]$$

$$\alpha_{max} := 10 \frac{\ln\left[\frac{\left[\cosh\left(n \cdot \operatorname{acosh}\left(\frac{\Omega_s}{\Omega_p}\right)\right)\right]^2 + 10^{\left(\frac{1}{10} \cdot \alpha_{min}\right)} - 1}{\cosh\left(n \cdot \operatorname{acosh}\left(\frac{\Omega_s}{\Omega_p}\right)\right)^2}\right]}{\ln(10)}$$

$$\alpha_{max} = 0.5$$

$$\alpha_{min} := 10 \frac{\ln\left[\cosh\left(n \cdot \operatorname{acosh}\left(\frac{\Omega_s}{\Omega_p}\right)\right)^2 \cdot 10^{\left(\frac{1}{10} \cdot \alpha_{max}\right)} + 1 - \cosh\left(n \cdot \operatorname{acosh}\left(\frac{\Omega_s}{\Omega_p}\right)\right)^2\right]}{\ln(10)}$$

$$\alpha_{min} = 22$$

$$n := \frac{\operatorname{acosh}\left[\left[\frac{10^{\frac{\alpha_{min}}{10}} - 1}{10^{\frac{\alpha_{max}}{10}} - 1}\right]^{\frac{1}{2}}\right]}{\operatorname{acosh}\left(\frac{\Omega_s}{\Omega_p}\right)}$$

$$n = 2.975$$

Round up to an interger.

$$\text{ceil}(n) = 3$$

$$n := \text{ceil}(n)$$

$$\psi := \begin{cases} \frac{180}{2 \cdot n} & \text{if } \frac{n}{2} = \text{floor}\left(\frac{n}{2}\right) \\ \frac{180}{n} & \text{otherwise} \end{cases}$$

$$\psi = 60$$

$$\psi := \psi \cdot \frac{\pi}{180}$$

$$\psi = 1.0$$

$$\varepsilon := \left(10^{\frac{\alpha_{max}}{10}} - 1\right)^{\frac{1}{2}}$$

The pole locations are now determined:

$$q_c = 2.732$$

$$a := \frac{1}{n} \cdot \text{asinh}\left(\frac{1}{\varepsilon}\right)$$

Real Poles:

For $\psi = 0$; n odd

$$\sigma_s := |\sinh(a)|$$

Complex Poles:

For $\psi = (\psi, +/-2\psi, +/-3\psi....)$

$$\sigma_k := |-\sinh(a) \cdot \cos(\psi)|$$

$$\omega_k := |\cosh(a) \cdot \sin(\psi)|$$

The half power (3-dB) frequency is determined by:

$$\Omega_{hp} := \cosh\left(\frac{1}{\text{ceil}(n)} \cdot \text{acosh}\left(\frac{1}{\varepsilon}\right)\right)$$

$$\Sigma := |\sigma_k|$$

$$\Omega := |\omega_k|$$

$$C := \Sigma^2 + \Omega^2$$

$$D := \frac{2 \cdot \Sigma}{q_c}$$

$$E := 4 + \frac{C}{q_c^2}$$

$$G := \sqrt{E^2 - 4 \cdot D^2}$$

$$Q := \frac{1}{D} \cdot \sqrt{\frac{1}{2} \cdot (E + G)}$$

$$K := \frac{\Sigma \cdot Q}{q_c}$$

$$W := K + \sqrt{K^2 - 1}$$

$$\omega_{02} := W \cdot \omega_0$$

$$Q_o := \frac{q_c}{\sigma_s}$$

$$\omega_{01} := \frac{1}{W} \cdot \omega_0$$

Set all values of capacitors to be equal

$$C := 10^{-7}$$

$$K_{m1} := \frac{1}{2 \cdot Q \cdot C \cdot \omega_{01}}$$

$$K_{m2} := \frac{1}{2 \cdot Q_o \cdot C \cdot \omega_0}$$

$$K_{m3} := \frac{1}{2 \cdot Q \cdot C \cdot \omega_{02}}$$

Stage one:

$$R_1 := \left(T_1\right) \cdot K_{m1}$$

$$R_2 := \frac{1}{1 - \frac{1}{T_1}} \cdot K_{m1}$$

$$R_3 := 4 \cdot Q^2 \cdot K_{m1}$$

Stage 2:

$$R_4 := T_2 \cdot K_{m2}$$

$$R_5 := \frac{1}{1 - \frac{1}{T_2}} \cdot K_{m2}$$

$$R_6 := 4 \cdot Q_o{}^2 \cdot K_{m2}$$

Stage 3:

$$R_7 := \left(T_3\right) \cdot K_{m3}$$

$$R_8 := \frac{1}{1 - \frac{1}{T_3}} \cdot K_{m3}$$

$$R_9 := 4 \cdot Q^2 \cdot K_{m3}$$

The schematic in Figure 7-1 of the Chebyshev bandpass filter utilized the predicted values from the mathcad file, where lab resources allowed. Close approximations were used, which the circuit performance was extremely sensitive to. Any deviations from the values predicted in the mathcad file resulted in gain in the passband. Using SPICE to test possible circuit realizations greatly reduces the time to implement hardware. SPICE will predict if a given circuit realization will perform as desired with available parts, before actual hardware measurements are made. This is helpful because Chebyshev circuit realization can be difficult, small changes in the circuit elements can result in undesired performance. The simulated AC results from Ispice, Pspice, and Micro-Cap V are shown in Figure 7-2 through Figure 7-4 respectively. The measured breadboard AC response of the filter is shown in Figure 7-5, and the measured transient response in shown Figure 7-6. The simulated transient response is shown in Figure 7-7 through Figure 7-8. All of the simulators correlated well to the hardware.

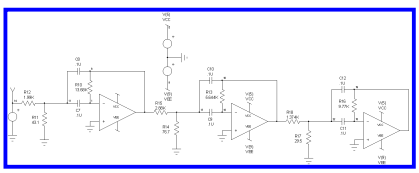


Figure 7-1: Chebyshev Bandpass Filter

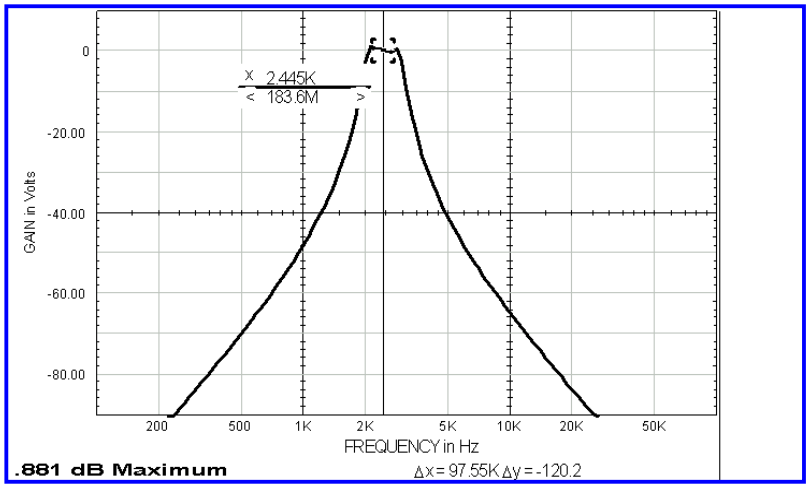


Figure 7-2: Ispice Simulated Chebyshev Bandpass Filter Response

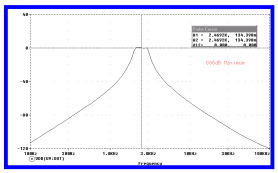


Figure 7-3: Pspice Simulated Chebyshev Bandpass Response

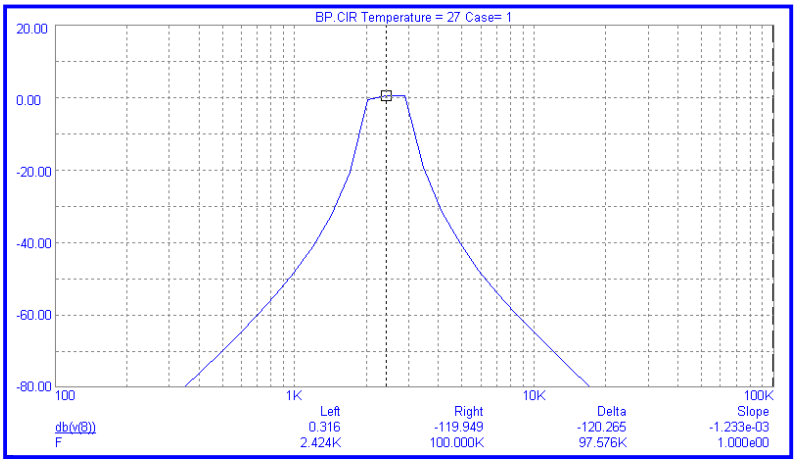


Figure 7-4: Micro-CapV Simulated Chebyshev Bandpass Response

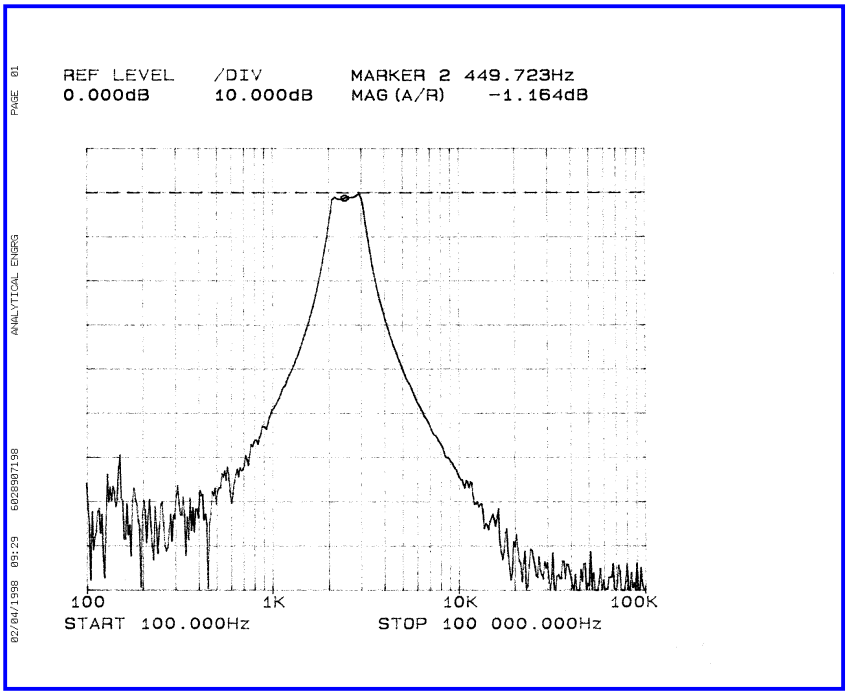


Figure 7-5: Measured Cebyshev Bandpass Filter Response

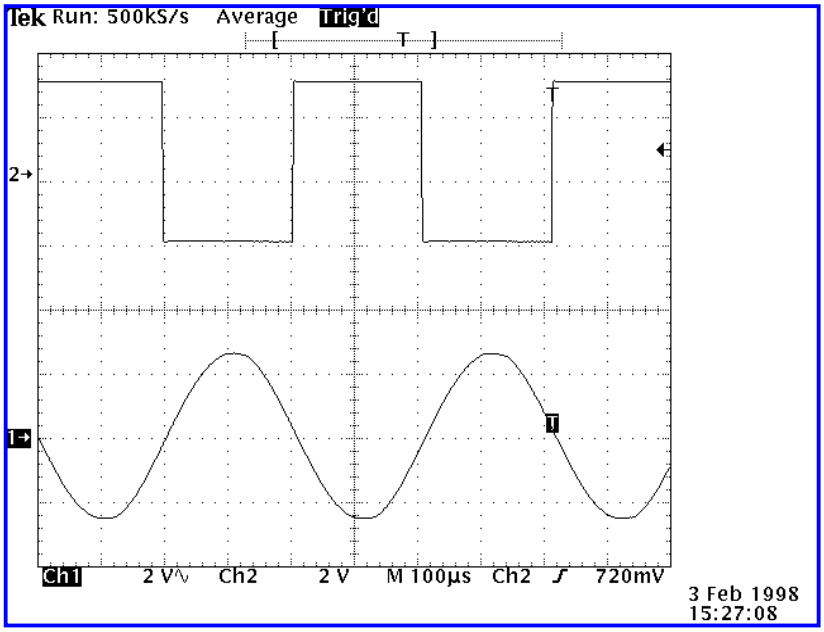


Figure 7-6: 2500Hz Square Wave Input, and Sine Wave Output

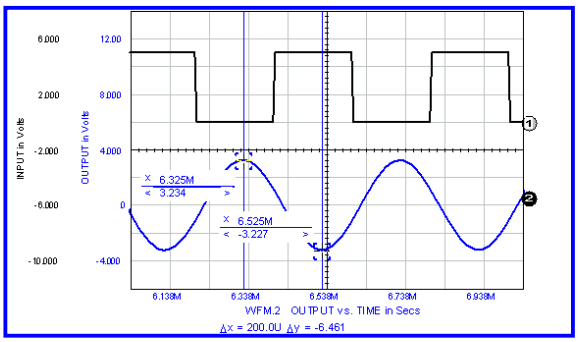


Figure 7-7: Ispice 2500Hz Square Wave Input, and Sine Wave Output

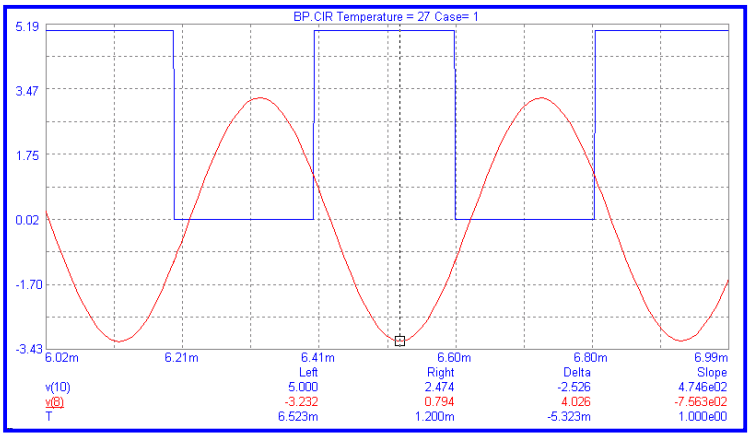


Figure 7-8: Micro-Cap 5 2500Hz Square Wave Input, and Sine Wave Output

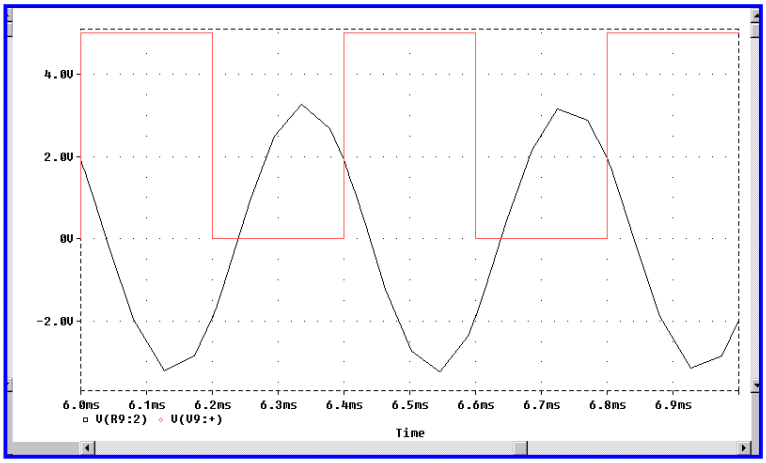


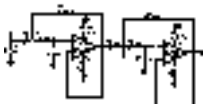
Figure 7-9: Pspice 2500Hz Square Wave Input, and Sine Wave Output

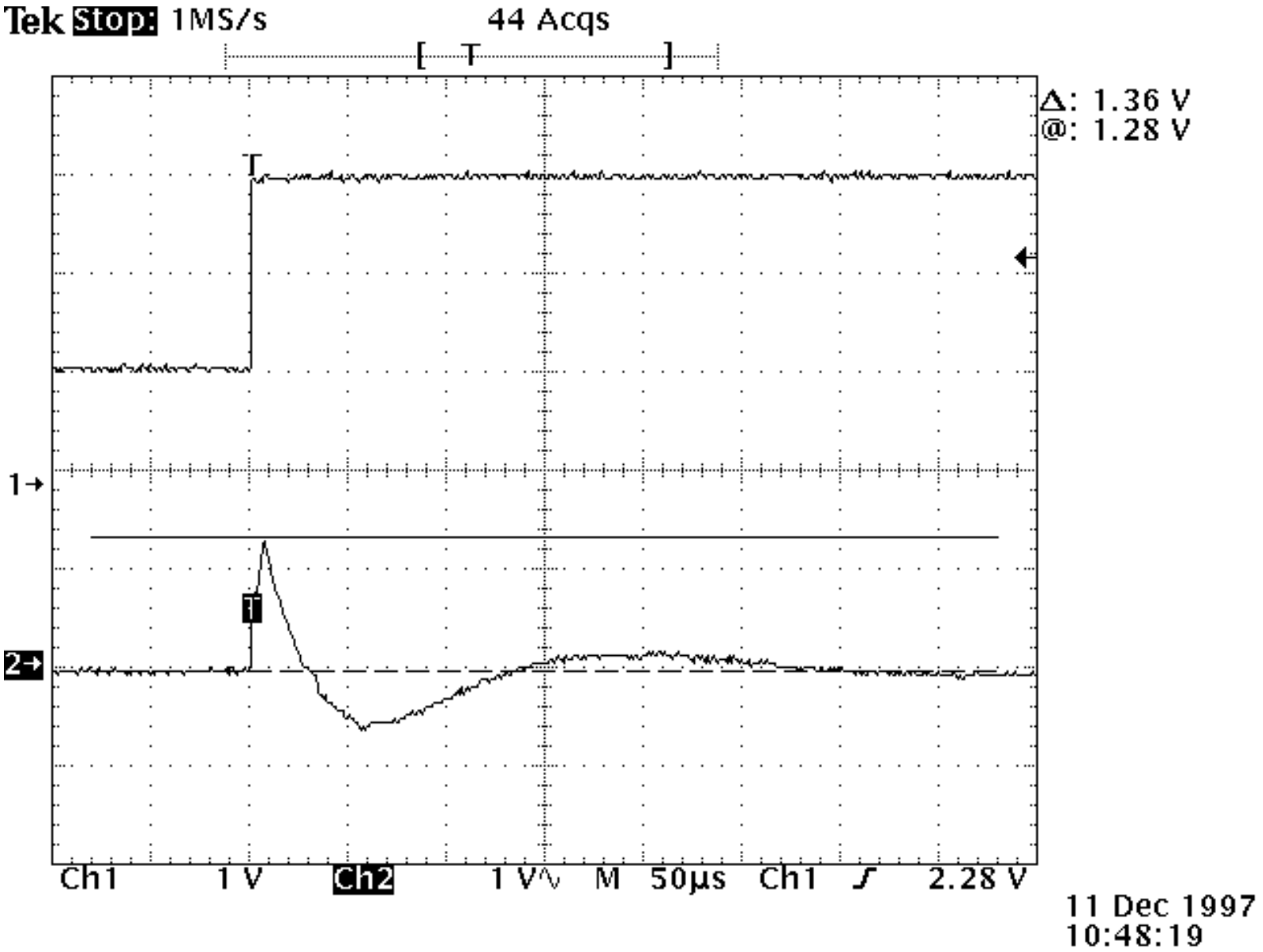
Table 7-1: Summary of Results

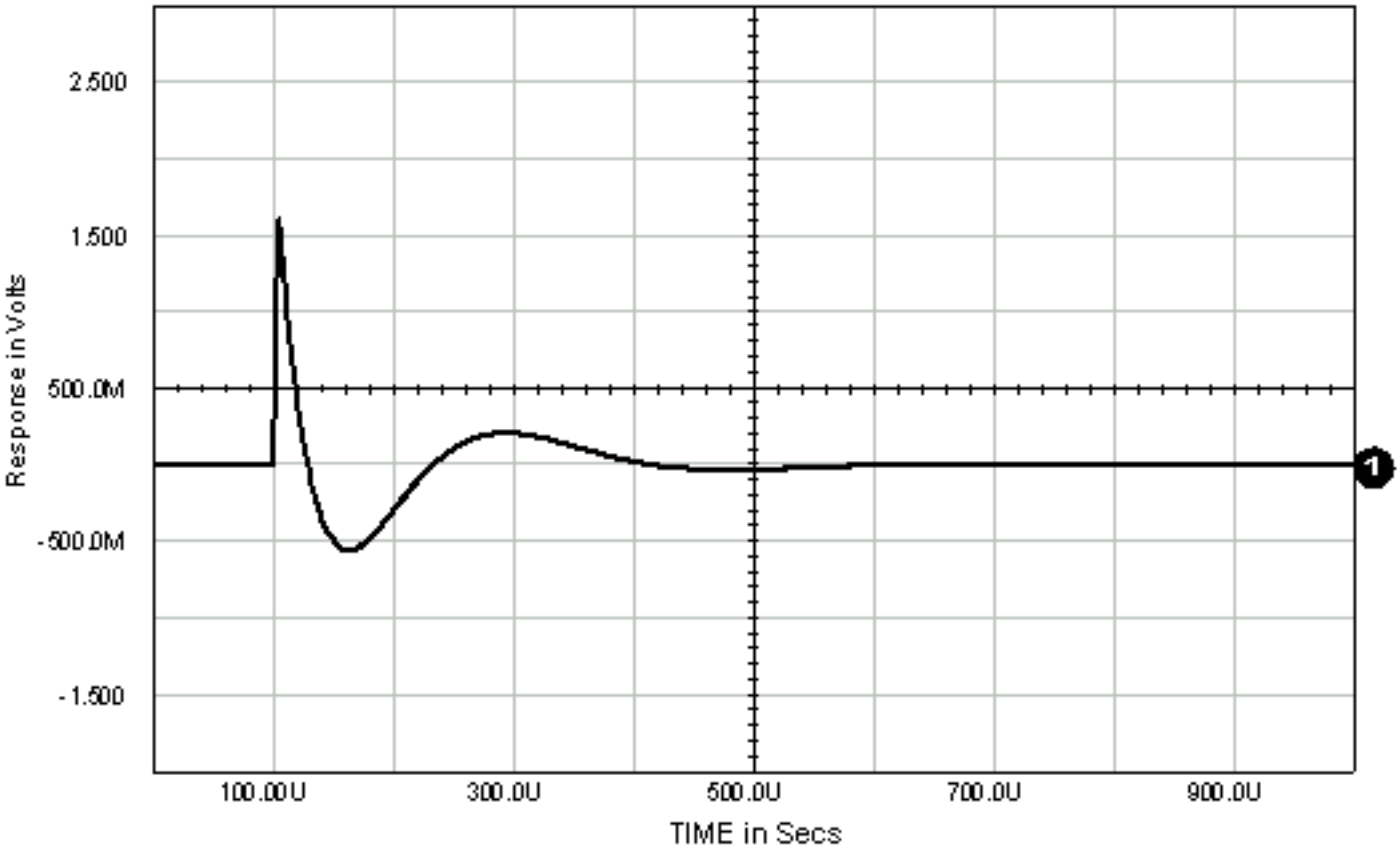
Condition	Hardware	Micro-Cap V	Ispice	Pspice
Center Frequency	2.45 KHz	2.42KHz	2.4 KHz	2.44 KHz
Maximum Attenuation	0 dB	0.316 dB	0.44 dB	0.886 dB
File Name	NA	BP	Cheby1	BP_n2

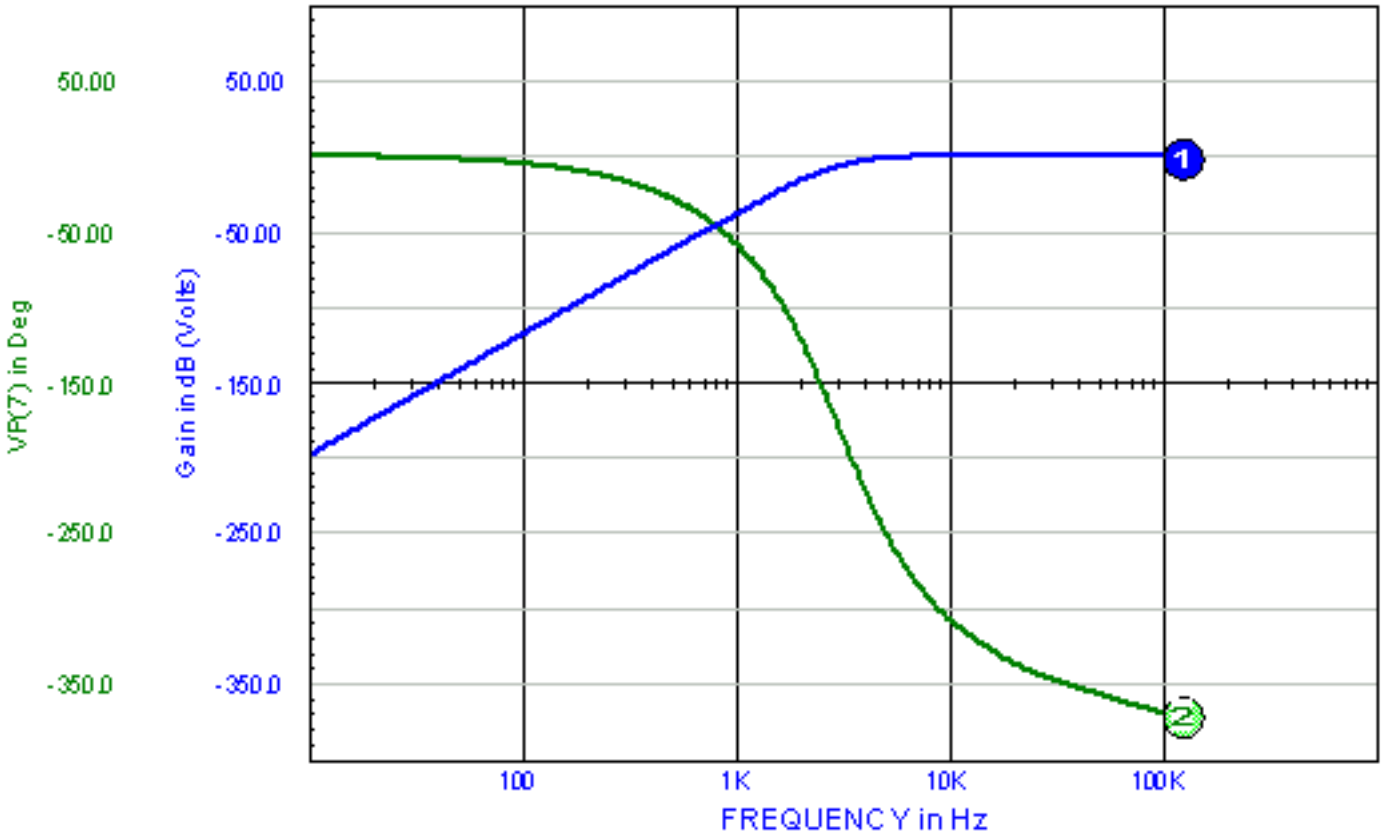
Run Time AC Analysis	NA	2.816 Sec	0.65 Sec	0.84 Sec

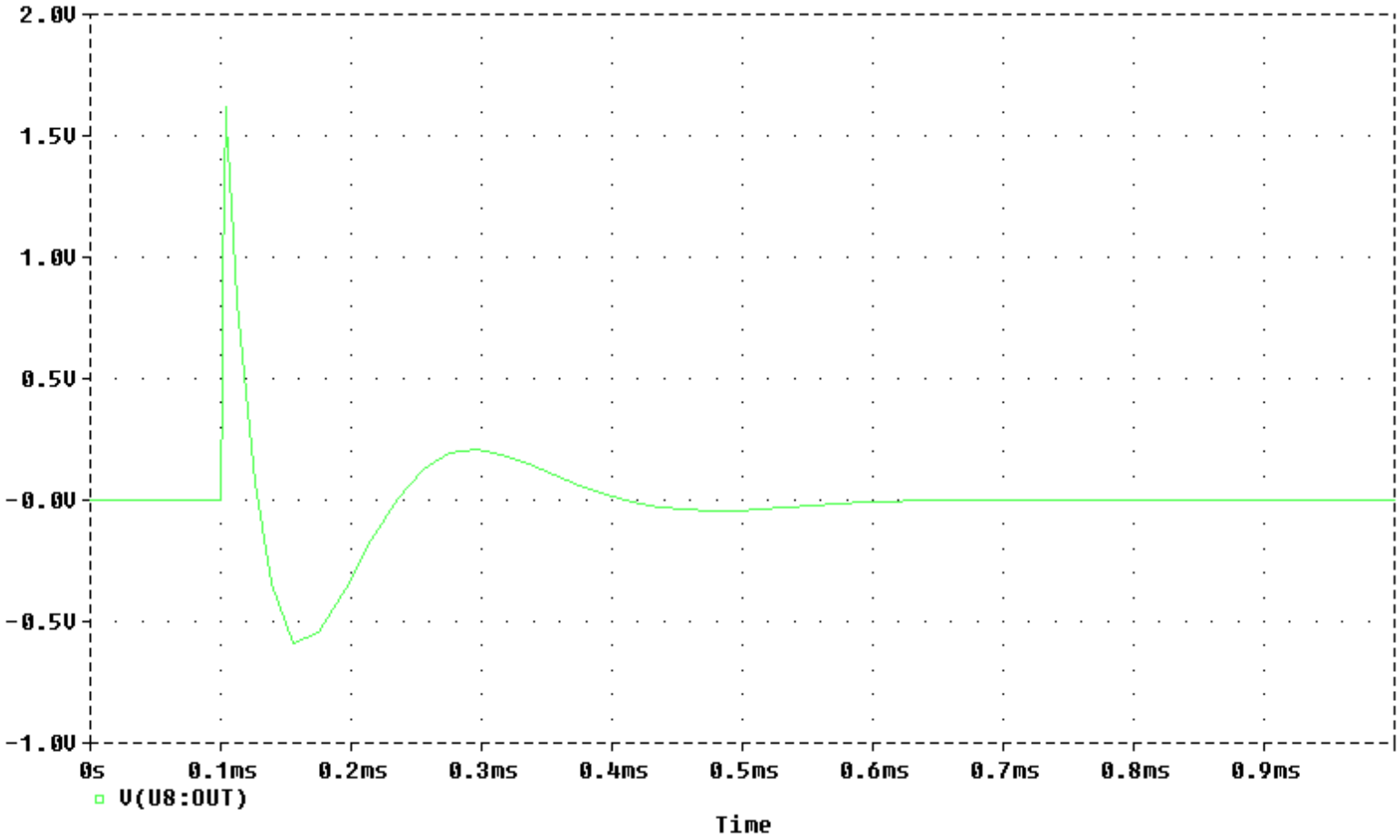
For more accuracy increase the number of points per division.

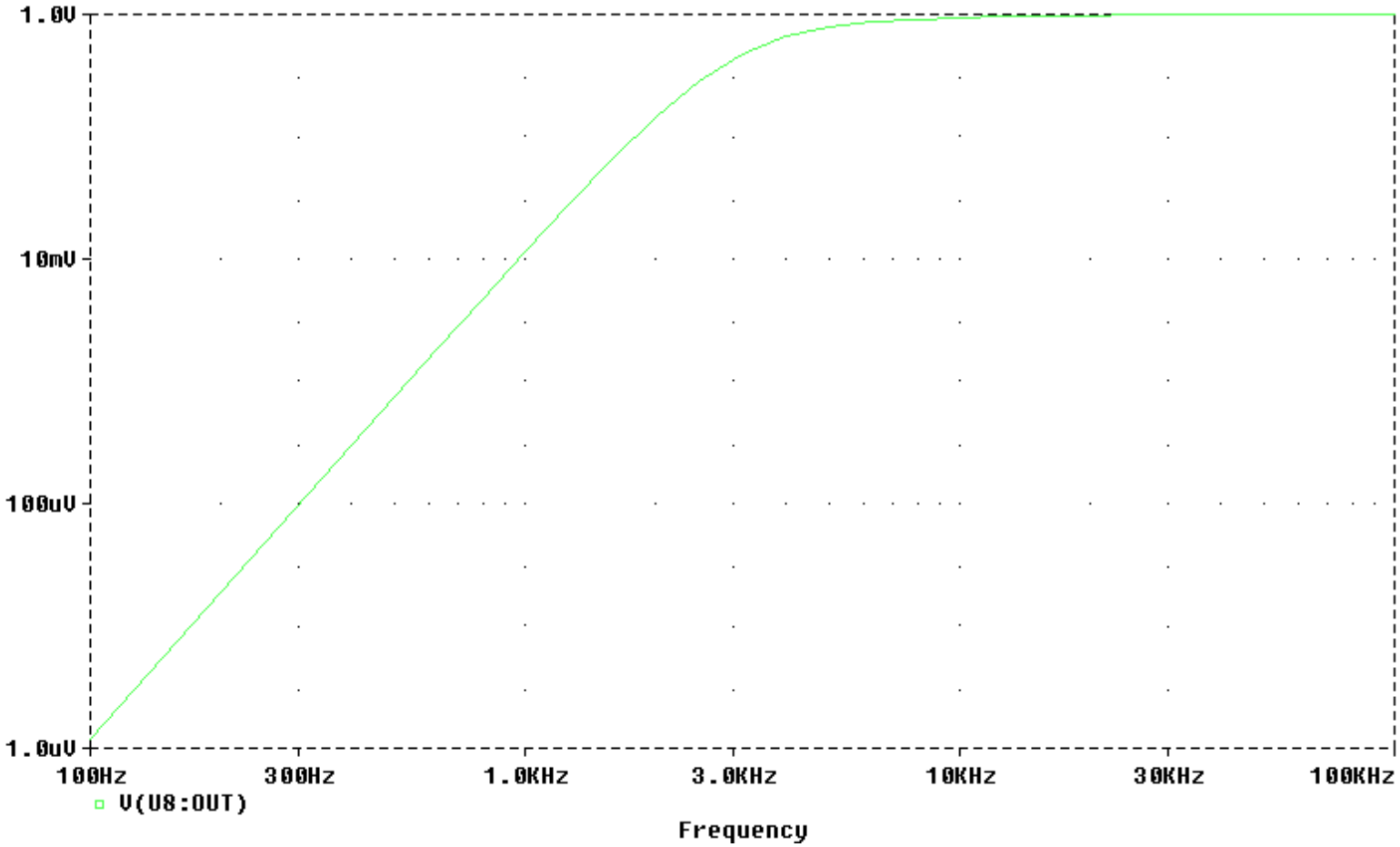


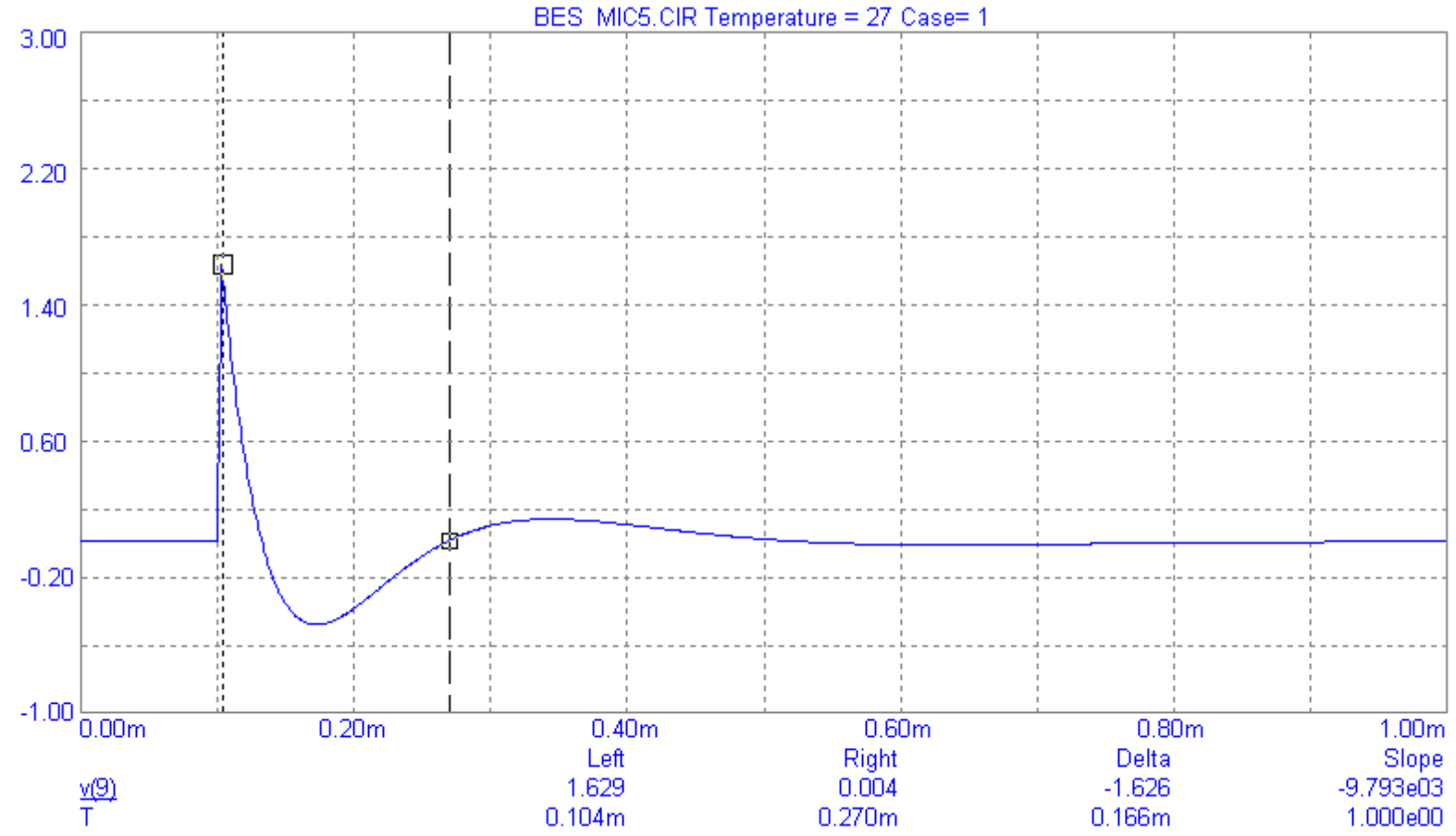

Tek Stop: 1MS/s
44 Acqs
Δ: 1.36 V
@: 1.28 V
1→
2→
Ch1 1 V
Ch2 1 V
M 50µs Ch1 2.28 V
11 Dec 1997
10:48:19

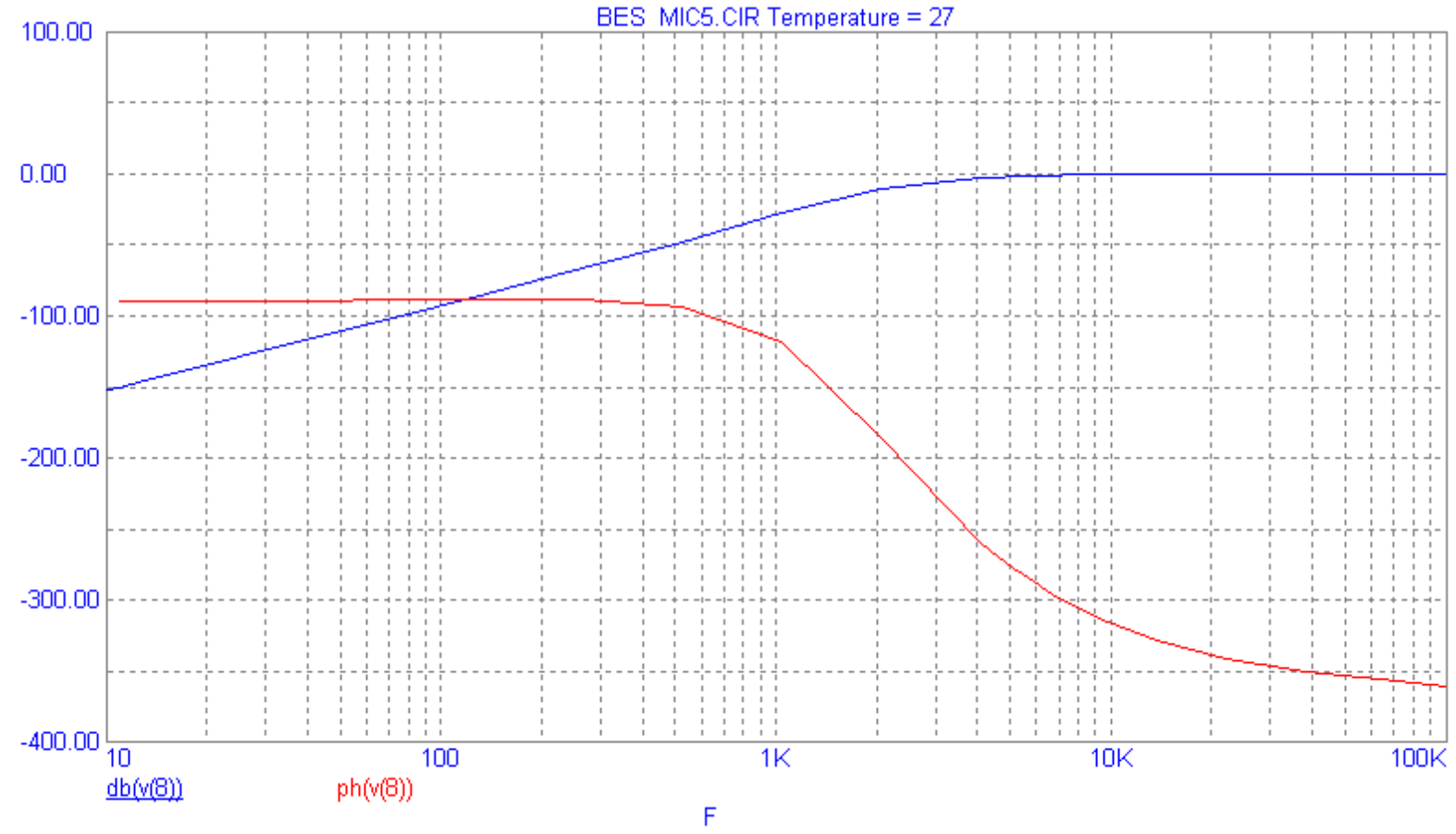

2.500
1.500
500.0M
-500.0M
-1.500
Response in Volts
100.00U
300.0U
500.0U
700.0U
900.0U
TIME in Secs
1


50.00
-50.00
-150.0
-250.0
-350.0
VP(7) in Deg
50.00
-50.00
-150.0
-250.0
-350.0
Gain in dB (Volts)
100
1K
10K
100K
FREQUENCY in Hz
1
2


2.0V
1.5V
1.0V
0.5V
-0.0V
-0.5V
-1.0V
0s
0.1ms
0.2ms
0.3ms
0.4ms
0.5ms
0.6ms
0.7ms
0.8ms
0.9ms
V(U8:OUT)
Time


1.0V
10mV
100uV
1.0uV
100Hz
300Hz
1.0KHz
3.0KHz
10KHz
30KHz
100KHz
V(U8:OUT)
Frequency


BES MIC5.CIR Temperature = 27 Case= 1
3.00
2.20
1.40
0.60
-0.20
-1.00
0.00m
0.20m
0.40m
0.60m
0.80m
1.00m
Left
Right
Delta
Slope
v(9)
1.629
0.004
-1.626
-9.793e03
T
0.104m
0.270m
0.166m
1.000e00


BES MIC5.CIR Temperature = 27
100.00
0.00
-100.00
-200.00
-300.00
-400.00
10
100
1K
10K
100K
db(v(8))
ph(v(8))
F

#8: Chebyshev Lowpass Filter

The Chebyshev lowpass filter shown in Figure 2 was constructed in all three simulators as well as in hardware. The circuit values in Figure were used in all cases. A Mathcad file that was utilized to design the Chebyshev lowpass filter is located in the Chebyshev directory of the CD which accompanies this book. This file can easily be modified to accommodate designs which utilize a Sallen-Key circuit for the stages in the filter. The Sallen-Key Circuit used for each stage of the filter is shown in Figure 8-1. The schematic of the circuit that was used in each simulator is shown in Figure 8-2. The measured breadboard results are shown in Figure 8-3, and the simulated results are shown in Figure 8-4 through Figure 8-6.

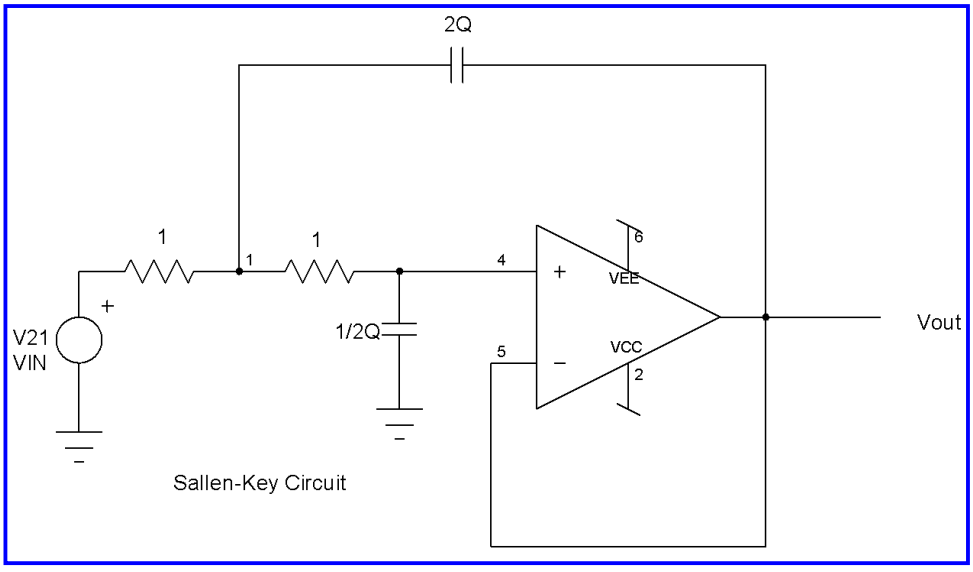


Figure 8-1: Sallen-Key Circuit

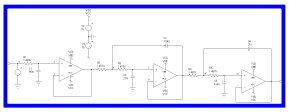


Figure 8-2: Chebyshev Lowpass Filter

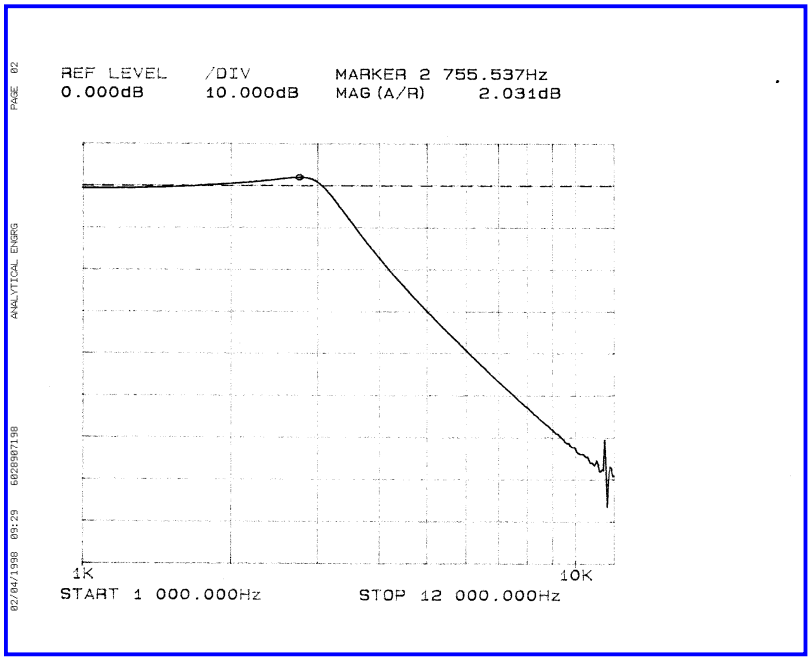


Figure 8-3: Chebyshev Lowpass Filter, Measured Data

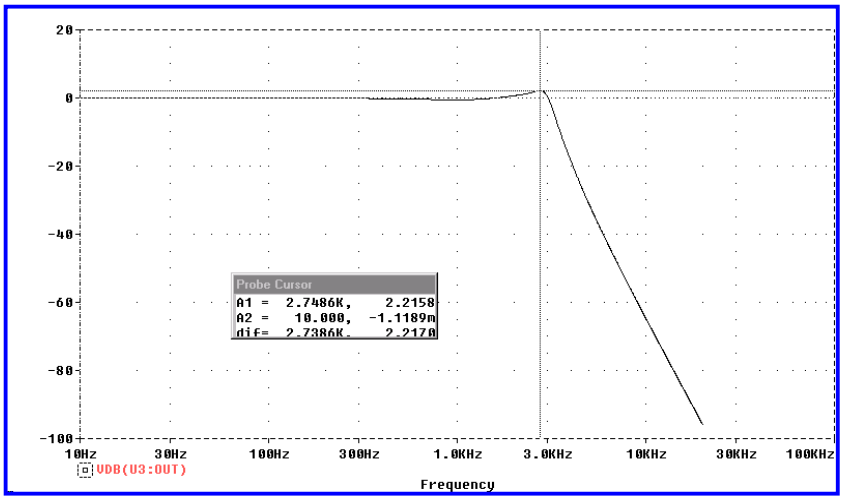


Figure 8-4 Pspice Chebyshev Lowpass Filter Results

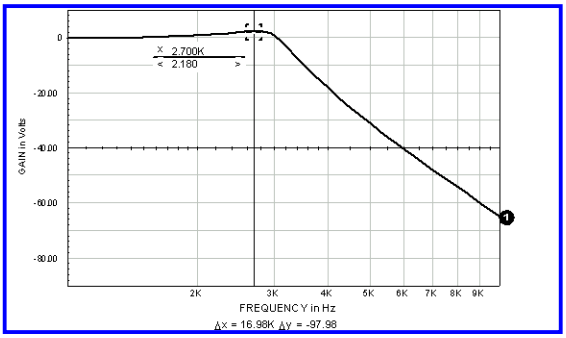


Figure 8-5: Ispice Chebyshev Lowpass Filter Results

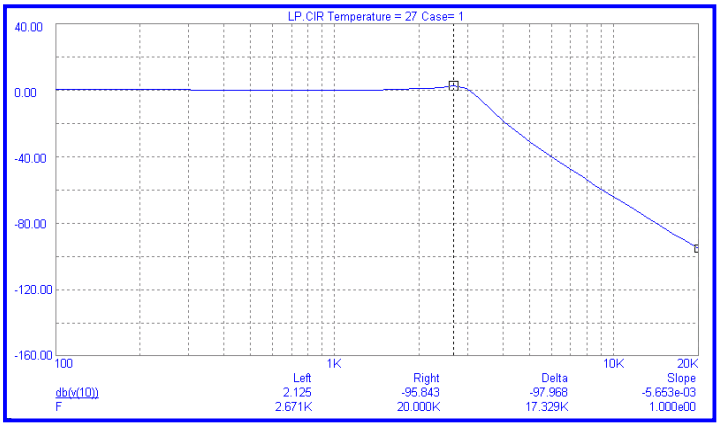


Figure 8-6: Micro-Cap V Chebyshev Lowpass Filter Results

Table 8-1: Spice Statistics

Simulator	File Name	Maximum Attenuation	Run Time
Hardware	NA	2.03dB at 2.76KHz	NA
Pspice	Lp_2	2.22dB at 2.75KHz	1.05sec
Micro-Cap V	Lp	2.13dB at 2.67KHz	3.2sec
Ispice	Lp_n5	2.18dB at 2.70Khz	1.133sec

$$\omega_2 := 29502 \cdot \pi$$

$$\omega_4 := 35002 \cdot \pi$$

$$\alpha_{max} := .5$$

$$\omega_1 := 20502 \cdot \pi$$

$$\omega_3 := 15002 \cdot \pi$$

$$\alpha_{min} := 22$$

$$\omega_0^2 = \omega_1 \omega_2$$

$$\omega_0 := \sqrt{\omega_1 \cdot \omega_2}$$

$$\omega_{0freq} := \frac{\omega_0}{2 \cdot \pi}$$

$$bw := \omega_2 - \omega_1$$

$$q_c = \frac{\omega_0}{bw}$$

$$q_c := \frac{\omega_0}{\omega_2 - \omega_1}$$

$$\Omega_s := \frac{\omega_4 - \omega_3}{\omega_2 - \omega_1}$$

$$\Omega_p := -\left[\frac{-\left(\omega_2^2\right) + \omega_0^2}{\omega_2 \cdot \left(\omega_2 - \omega_1\right)}\right]$$

$$\alpha_{max} := 10 \frac{\ln\left[\frac{\left[\cosh\left(n \cdot \operatorname{acosh}\left(\frac{\Omega_s}{\Omega_p}\right)\right)\right]^2 + 10^{\left(\frac{1}{10} \cdot \alpha_{min}\right)} - 1}{\left[\cosh\left(n \cdot \operatorname{acosh}\left(\frac{\Omega_s}{\Omega_p}\right)\right)\right]^2}\right]}{\ln(10)}$$

$$\alpha_{max} = 0.5$$

$$\alpha_{min} := 10 \frac{\ln\left[\cosh\left(n \cdot \operatorname{acosh}\left(\frac{\Omega_s}{\Omega_p}\right)\right)^2 \cdot 10^{\left(\frac{1}{10} \cdot \alpha_{max}\right)} + 1 - \cosh\left(n \cdot \operatorname{acosh}\left(\frac{\Omega_s}{\Omega_p}\right)\right)^2\right]}{\ln(10)}$$

$$\alpha_{min} = 22$$

$$n := \frac{\operatorname{acosh}\left[\left[\frac{10^{\frac{\alpha_{min}}{10}} - 1}{10^{\frac{\alpha_{max}}{10}} - 1}\right]^{\frac{1}{2}}\right]}{\operatorname{acosh}\left(\frac{\Omega_s}{\Omega_p}\right)}$$

$$n = 2.975$$

ceil(n) = 3

$$n := ceil(n)$$

$$\psi := \begin{cases} \frac{180}{2 \cdot n} & \text{if } \frac{n}{2} = \text{floor}\left(\frac{n}{2}\right) \\ \frac{180}{n} & \text{otherwise} \end{cases}$$

$\psi = 60$

$$\psi := \psi \cdot \frac{\pi}{180}$$

$\psi = 1.0$

$$\varepsilon := \left(10^{\frac{\alpha_{max}}{10}} - 1 \right)^{\frac{1}{2}}$$

$$q_c = 2.732$$

$$a := \frac{1}{n} \cdot \operatorname{asinh}\left(\frac{1}{\varepsilon}\right)$$

$$\sigma_s := |\sinh(a)|$$

$$\sigma_k := \left| -\sinh(a) \cdot \cos(\psi) \right|$$

$$\omega_k := \left|\cosh(a)\cdot\sin(\psi)\right|$$

$$\Omega_{hp} := \cosh\left(\frac{1}{\mathrm{ceil}(n)} \cdot \mathrm{acosh}\left(\frac{1}{\varepsilon}\right)\right)$$

$$\Sigma := \left|\sigma_k\right|$$

$$\Omega := \left|\omega_k\right|$$

$$C := \Sigma^2 + \Omega^2$$

$$D := \frac{2 \cdot \Sigma}{q_c}$$

$$E := 4 + \frac{C}{q_c^2}$$

$$G := \sqrt{E^2 - 4 \cdot D^2}$$

$$Q := \frac{1}{D} \cdot \sqrt{\frac{1}{2} \cdot (E + G)}$$

$$K := \frac{\Sigma \cdot Q}{q_c}$$

$$W := K + \sqrt{K^2 - 1}$$

$$\omega_{02} := W \cdot \omega_0$$

$$Q_o := \frac{q_c}{\sigma_s}$$

$$\omega_{01} := \frac{1}{W} \cdot \omega_0$$

$$C := 10^{-7}$$

$$K_{m1} := \frac{1}{2 \cdot Q \cdot C \cdot \omega_{01}}$$

$$K_{m2} := \frac{1}{2 \cdot Q_o \cdot C \cdot \omega_0}$$

$$K_{m3} := \frac{1}{2 \cdot Q \cdot C \cdot \omega_{02}}$$

$$R_1 := \left(T_1\right) \cdot K_{m1}$$

$$R_2 := \frac{1}{1 - \frac{1}{T_1}} \cdot K_{m1}$$

$$R_3 := 4 \cdot Q^2 \cdot K_{m1}$$

$$R_4 := T_2 \cdot K_{m2}$$

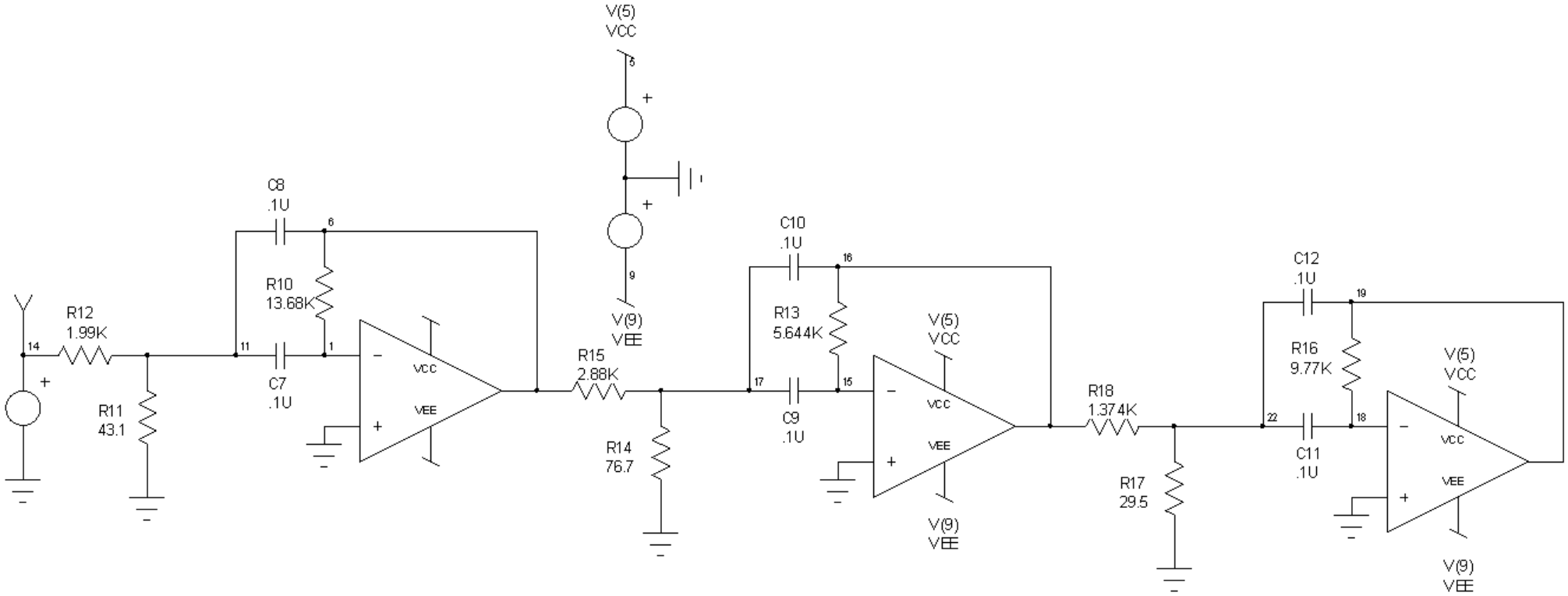
$$R_5 := \frac{1}{1 - \frac{1}{T_2}} \cdot K_{m2}$$

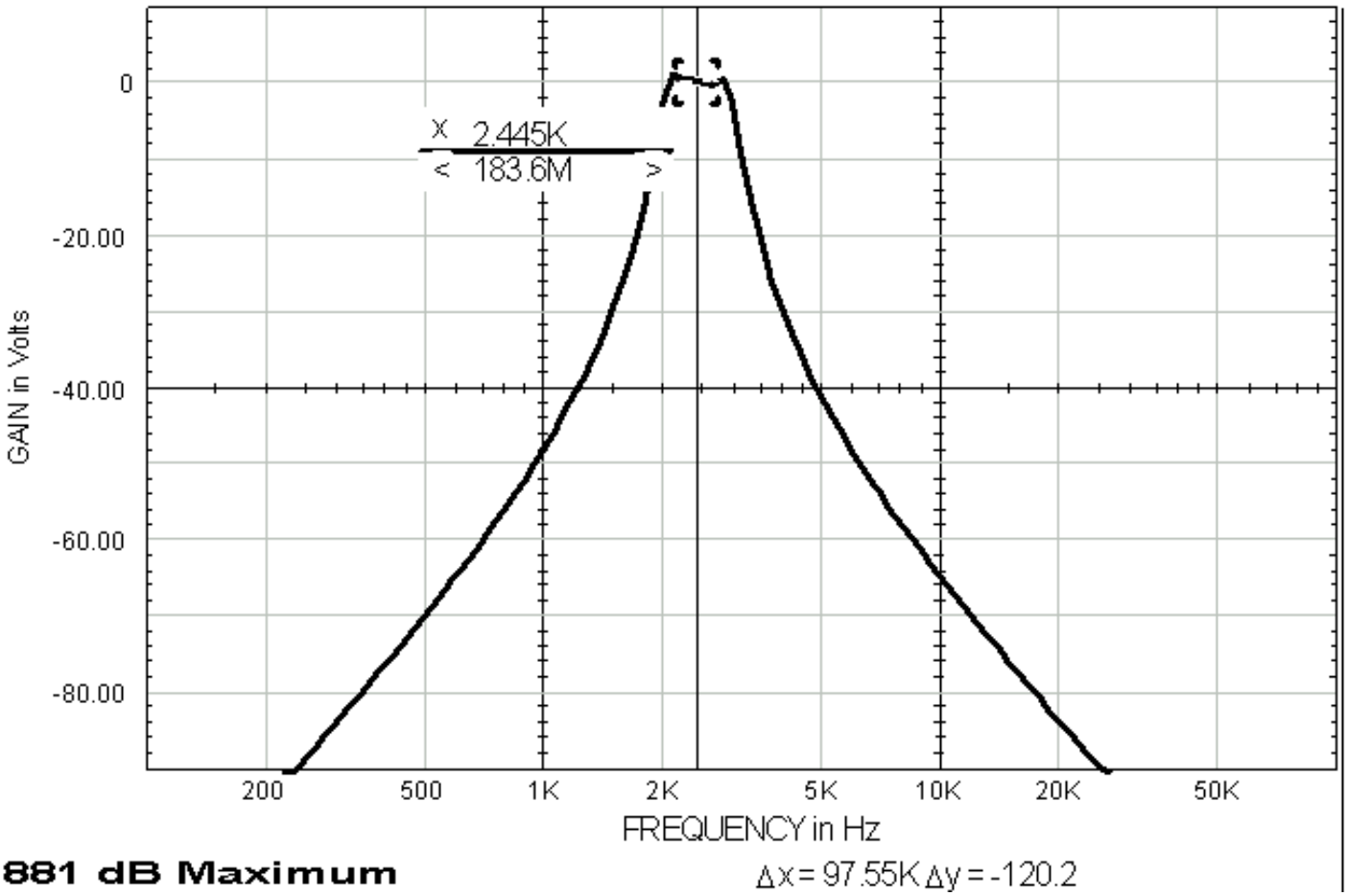
$$R_6 := 4 \cdot Q_o^2 \cdot K_{m2}$$

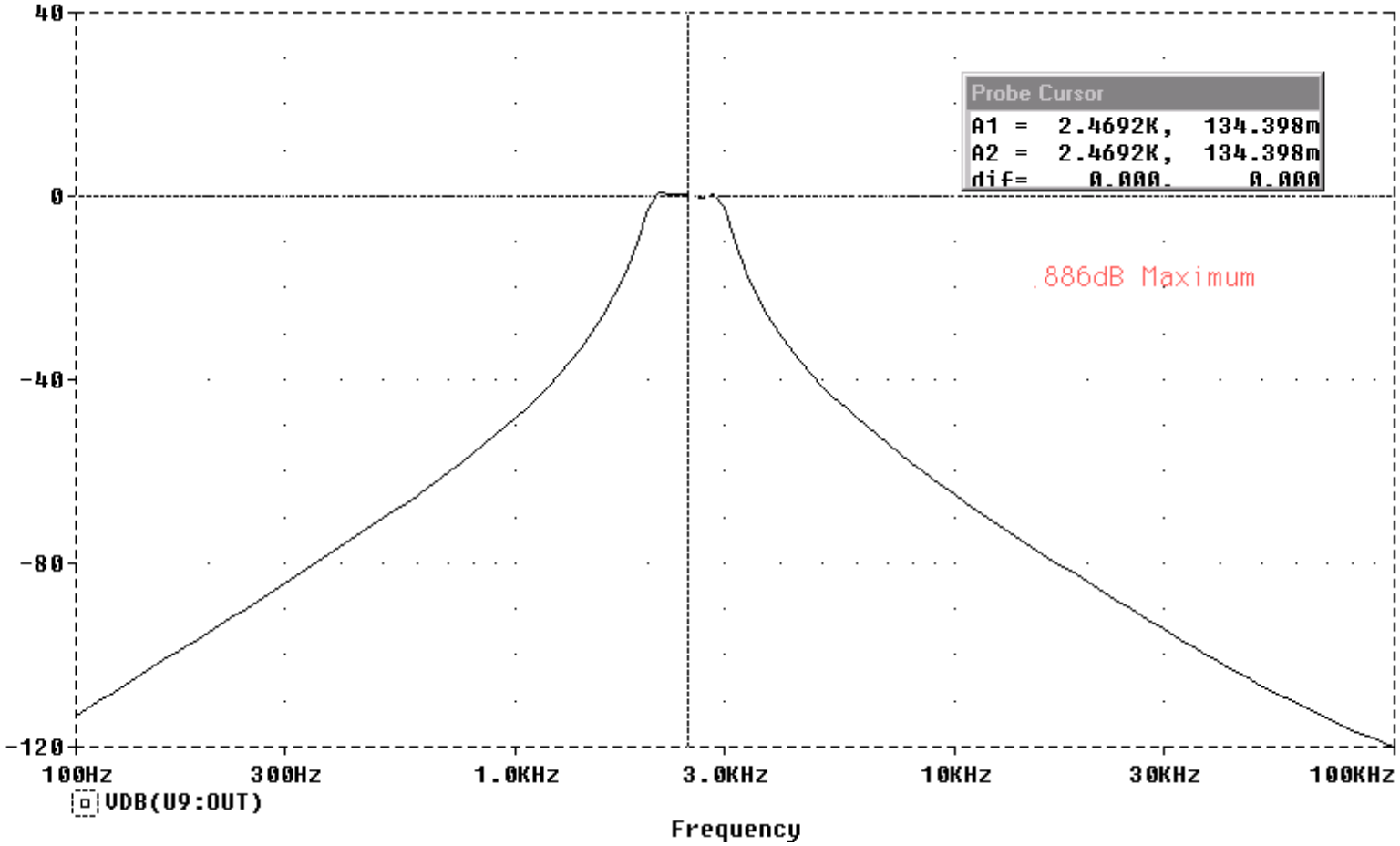
$$R_7 := \left(T_3\right) \cdot K_m :$$

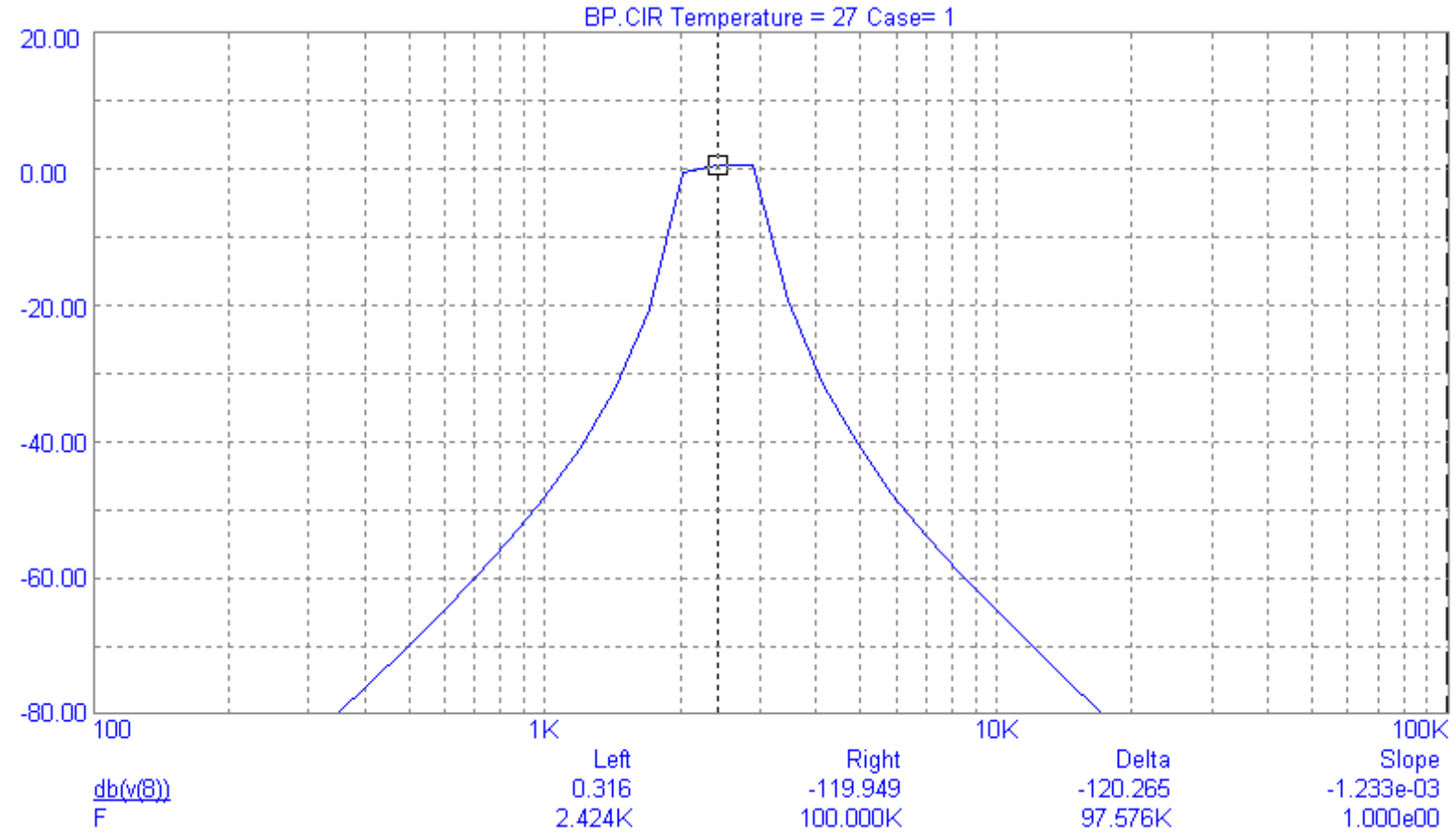
$$R_8 := \frac{1}{1 - \frac{1}{T_3}} \cdot K_{m3}$$

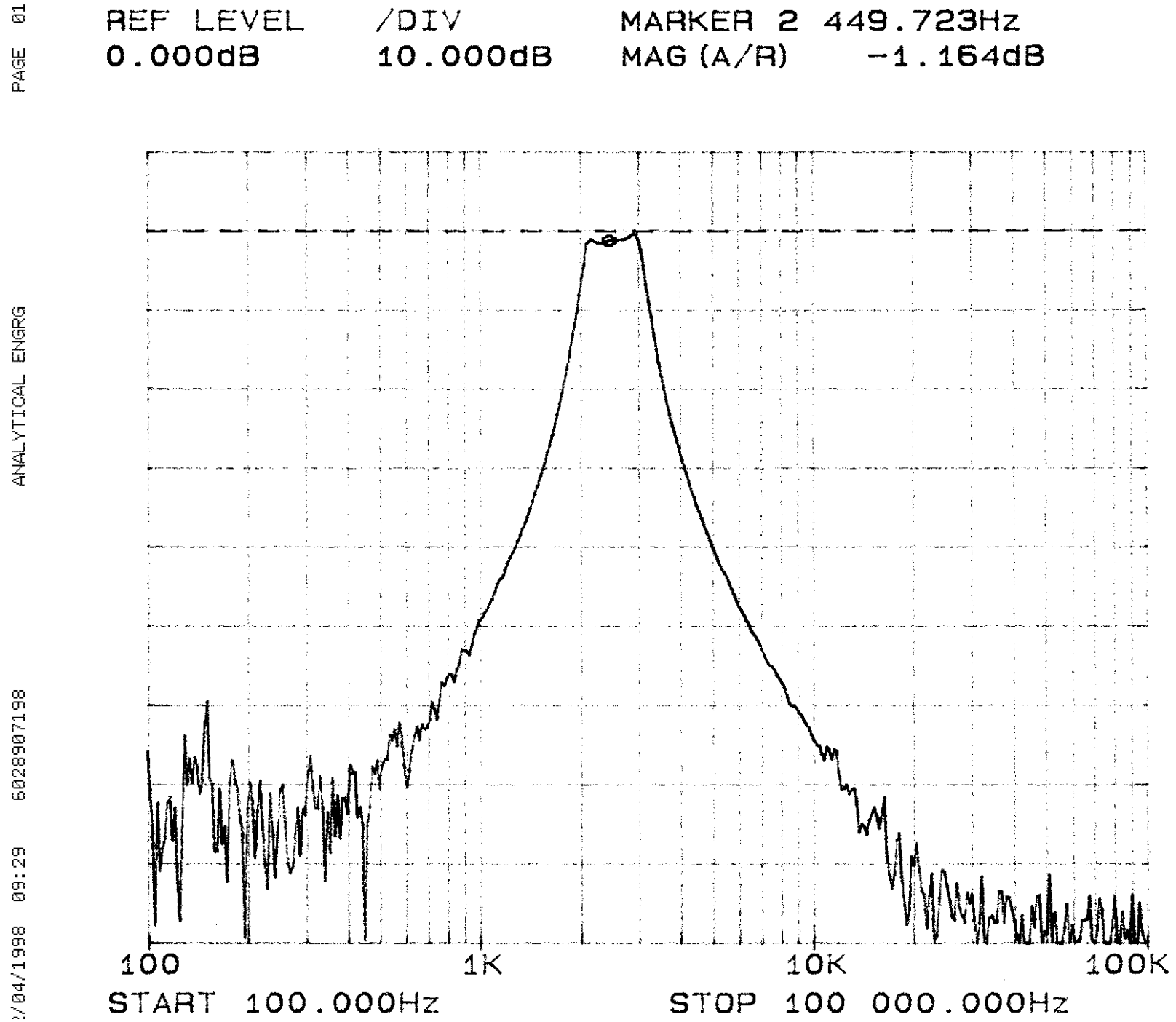
$$R_9 := 4 \cdot Q^2 \cdot K_{m3}$$

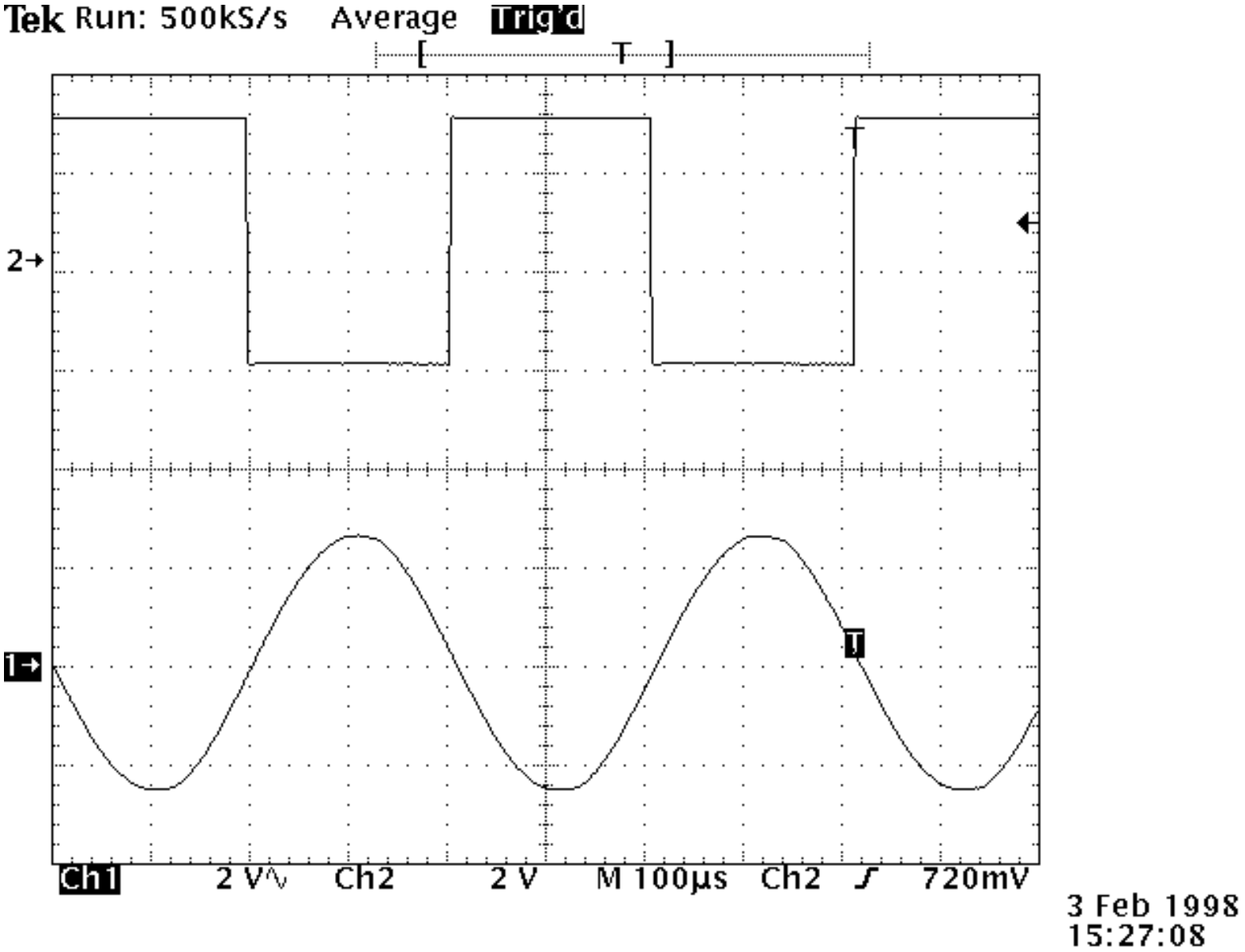

V(5)
VCC
V(9)
VEE
C8
.1U
R10
13.68K
R12
1.99K
R11
43.1
C7
.1U
VCC
VEE
R15
2.88K
R14
76.7
C10
.1U
R13
5.644K
C9
.1U
R18
1.374K
R17
29.5
C12
.1U
R16
9.77K
C11
.1U

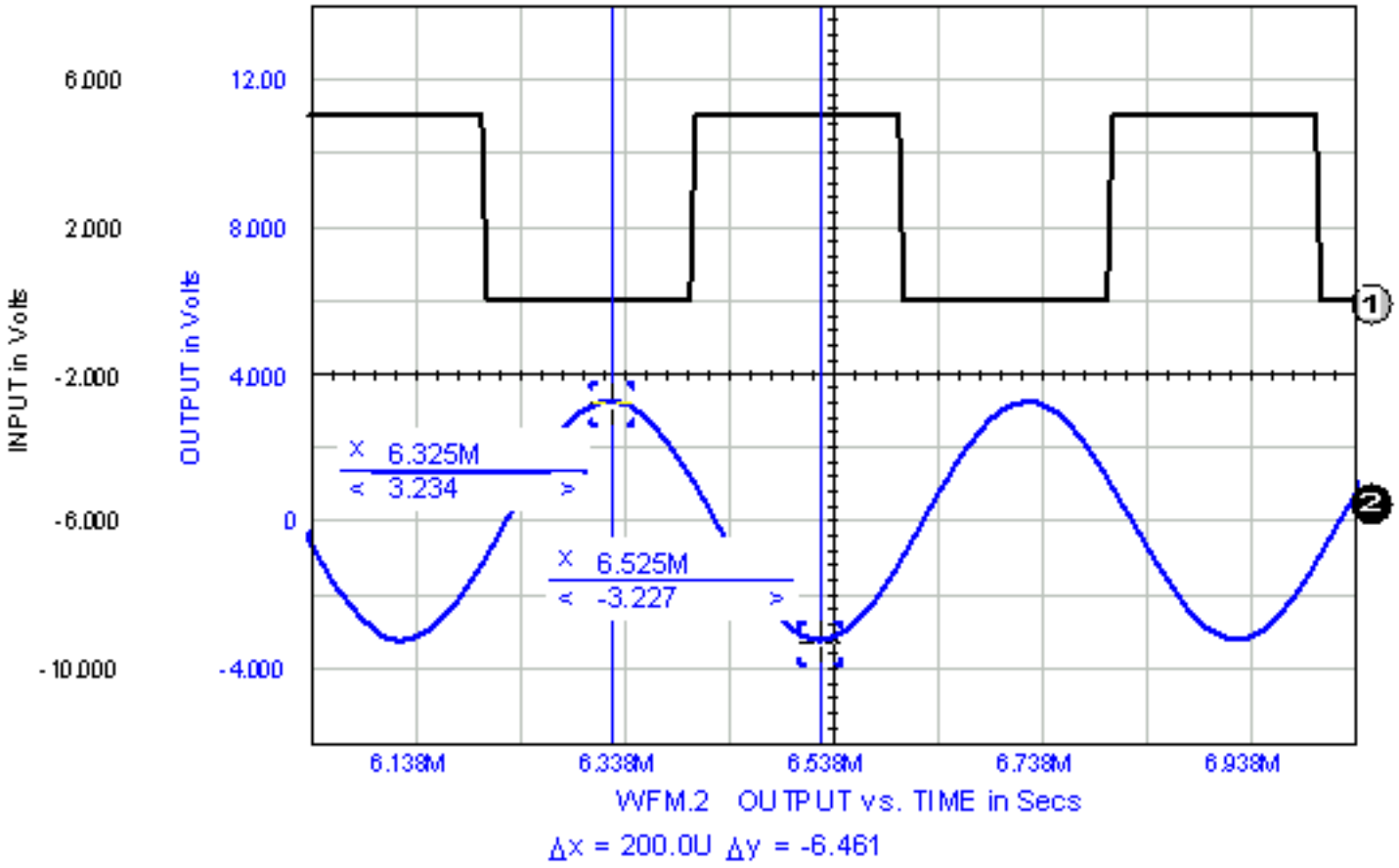

0
-20.00
-40.00
-60.00
-80.00
GAIN in Volts
X 2.445K
< 183.6M >
200
500
1K
2K
5K
10K
20K
50K
FREQUENCY in Hz
.881 dB Maximum
Δx = 97.55K Δy = -120.2

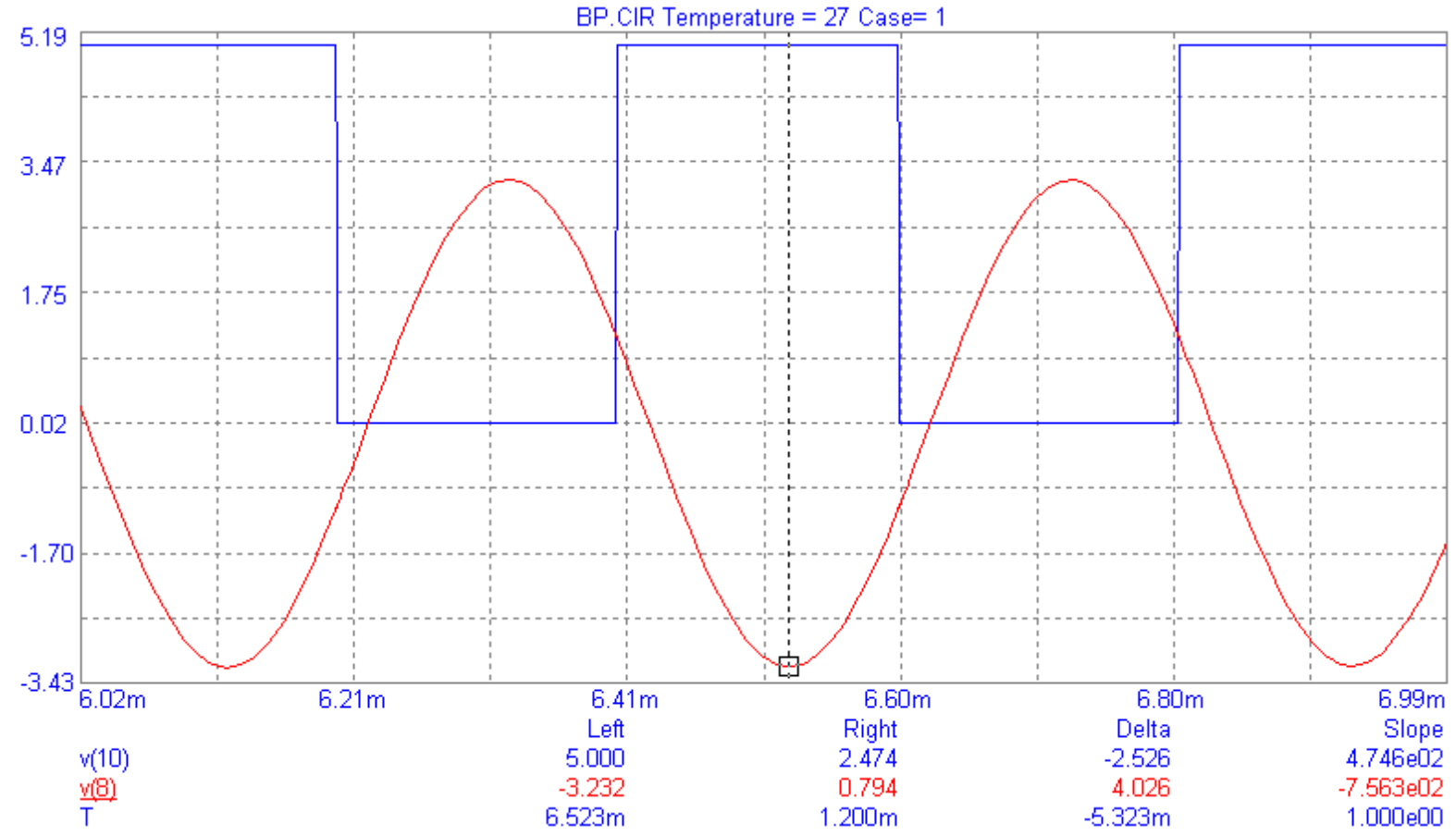

40
0
-40
-80
-120
Probe Cursor
A1 = 2.4692K, 134.398m
A2 = 2.4692K, 134.398m
dif= 0.000, 0.000
.886dB Maximum
100Hz
300Hz
1.0KHz
3.0KHz
10KHz
30KHz
100KHz
V(U9:OUT)
Frequency

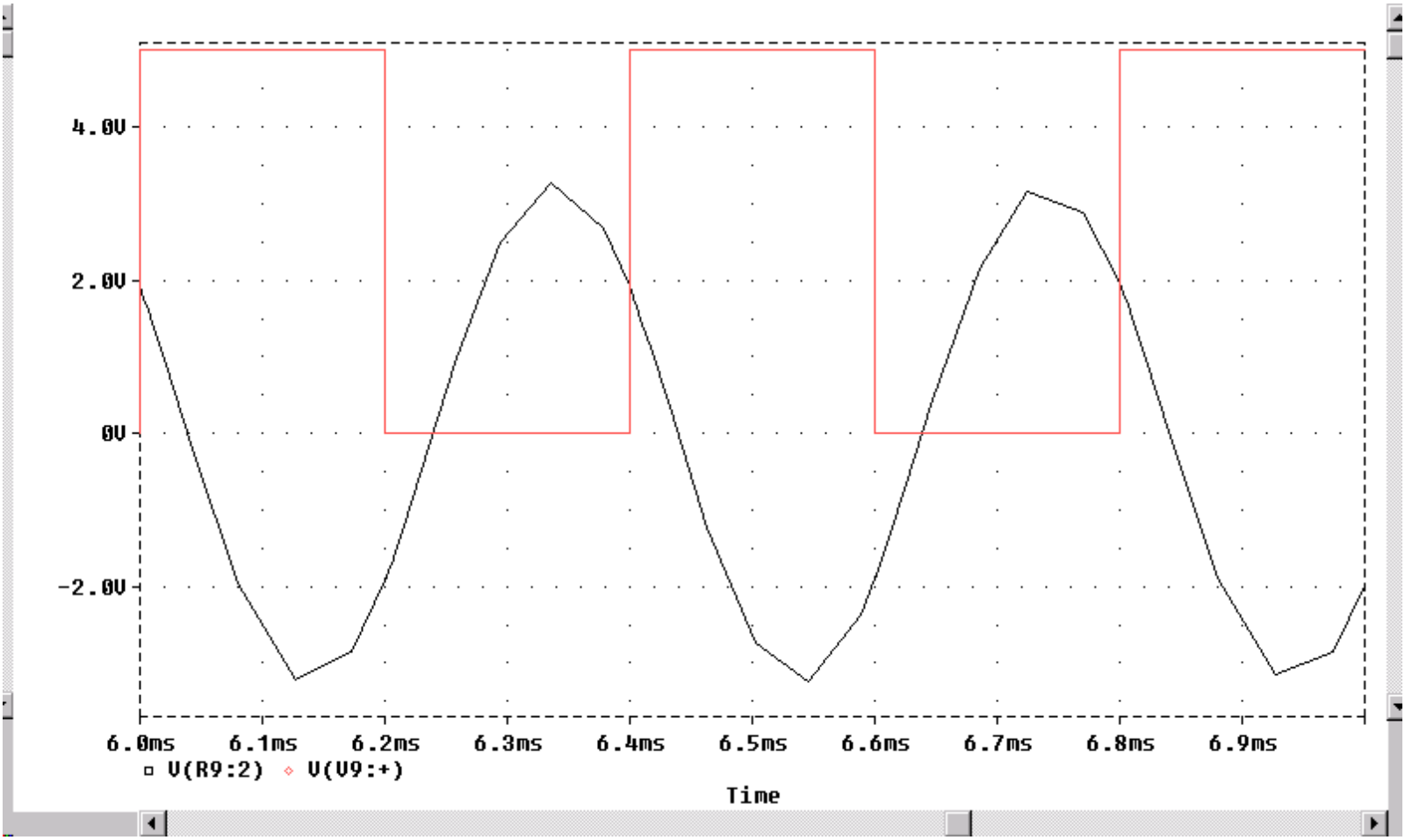

BP.CIR Temperature = 27 Case= 1
20.00
0.00
-20.00
-40.00
-60.00
-80.00
100
1K
10K
100K
Left
Right
Delta
Slope
db(v(8))
0.316
-119.949
-120.265
-1.233e-03
F
2.424K
100.000K
97.576K
1.000e00


REF LEVEL
0.000dB
/DIV
10.000dB
MARKER 2 449.723Hz
MAG (A/R) -1.164dB
PAGE 01
ANALYTICAL ENGRG
6028907198
09:29
/04/1998
100
1K
10K
100K
START 100.000Hz
STOP 100 000.000Hz


Tek Run: 500kS/s Average Trig'd
2→
1→
Ch1 2 V Ch2 2 V M 100µs Ch2 720mV
3 Feb 1998
15:27:08


6.000
2.000
-2.000
-6.000
-10.000
INPUT in Volts
12.00
8.000
4.000
0
-4.000
OUTPUT in Volts
X 6.325M
< 3.234 >
X 6.525M
< -3.227 >
1
2
6.138M
6.338M
6.538M
6.738M
6.938M
WFM.2 OUTPUT vs. TIME in Secs
Δx = 200.0U Δy = -6.461


BP.CIR Temperature = 27 Case= 1
5.19
3.47
1.75
0.02
-1.70
-3.43
6.02m
6.21m
6.41m
6.60m
6.80m
6.99m
Left
Right
Delta
Slope
v(10)
5.000
2.474
-2.526
4.746e02
v(8)
-3.232
0.794
4.026
-7.563e02
T
6.523m
1.200m
-5.323m
1.000e00


4.0V
2.0V
0V
-2.0V
6.0ms
6.1ms
6.2ms
6.3ms
6.4ms
6.5ms
6.6ms
6.7ms
6.8ms
6.9ms
V(R9:2)
V(V9:+)
Time

#9: Chebyshev Highpass Filter

The Chebyshev filter response offers higher attenuation and a steeper roll-off near the cutoff frequency, than the Butterworth filter response. There is a tradeoff to achieve the higher attenuation. The cost of utilizing a Chebyshev filter is higher values of Q, which leads to difficulties in hardware realization, and nonlinear phase characteristics, which can result in difficulties in predicting circuit performance.

A Chebyshev highpass filter was constructed with the component values that are shown in the schematic in Figure 9-1. The measured results are shown in Figure 9-2, and Figure 9-3.

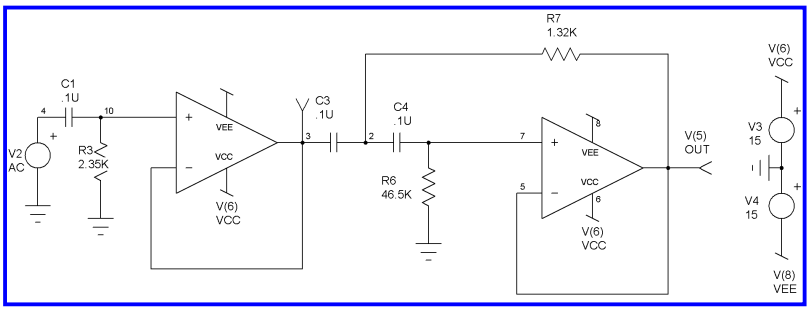


Figure 9-1: Chebyshev Highpass Filter

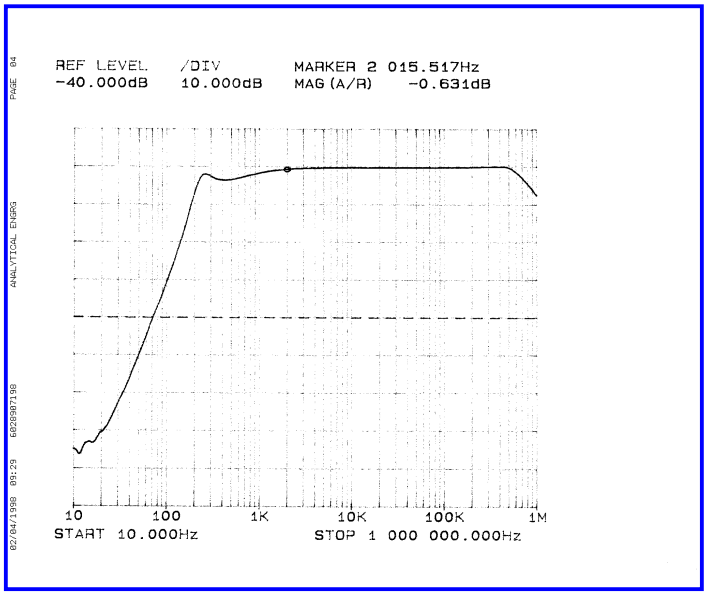


Figure 9-2: Chebyshev Highpass Filter Measured Results

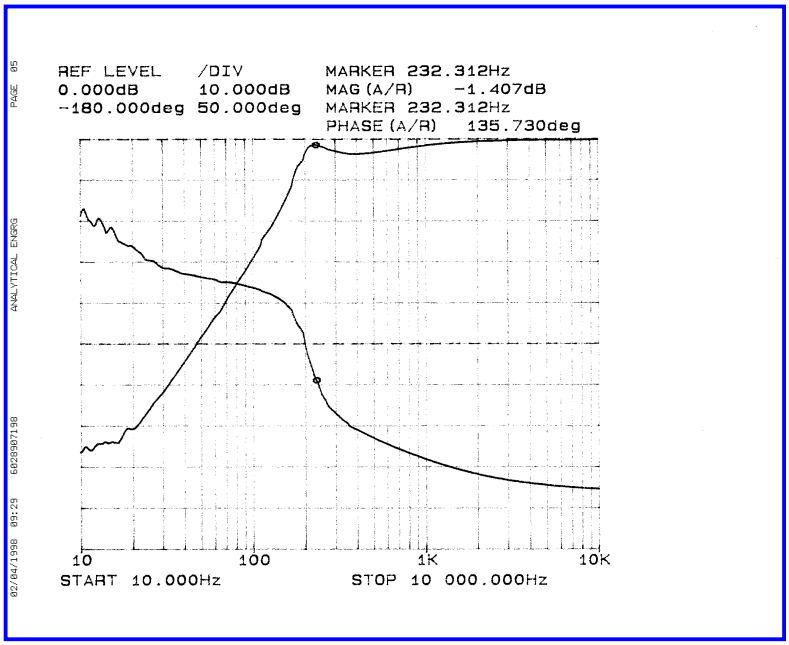


Figure 9-3: Chebyshev Highpass Filter Measured Results

The results of the three simulators are shown in Figure 9-4 through Figure 9-7. All of the simulators accurately predict the phase and gain of the Chebyshev highpass circuit.

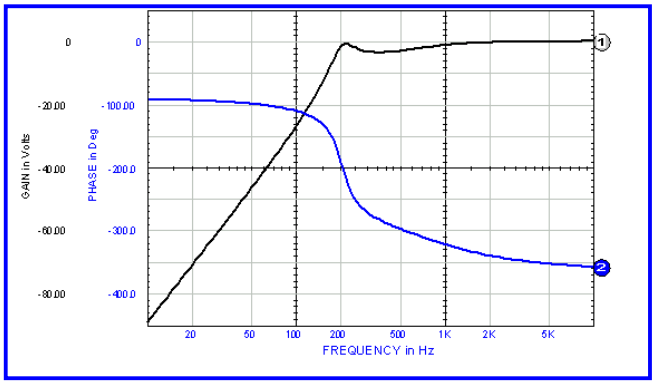


Figure 9-4: Ispice Chebyshev Highpass Filter

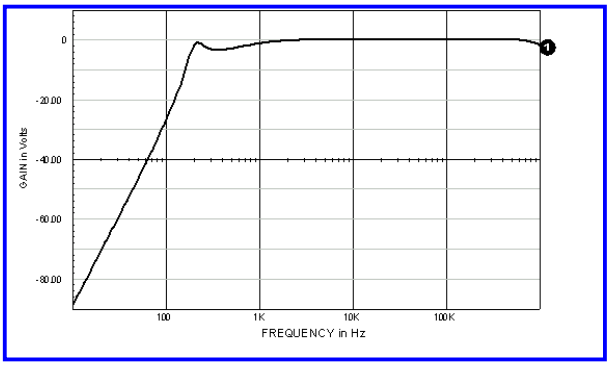


Figure 9-5: Ispice Chebyshev Highpass Filter

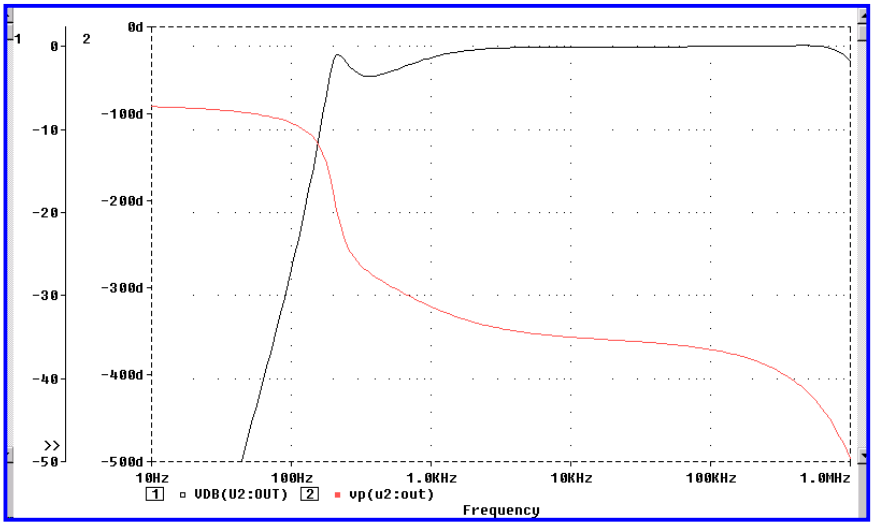


Figure 9-6: Pspice Chebyshev Highpass Filter

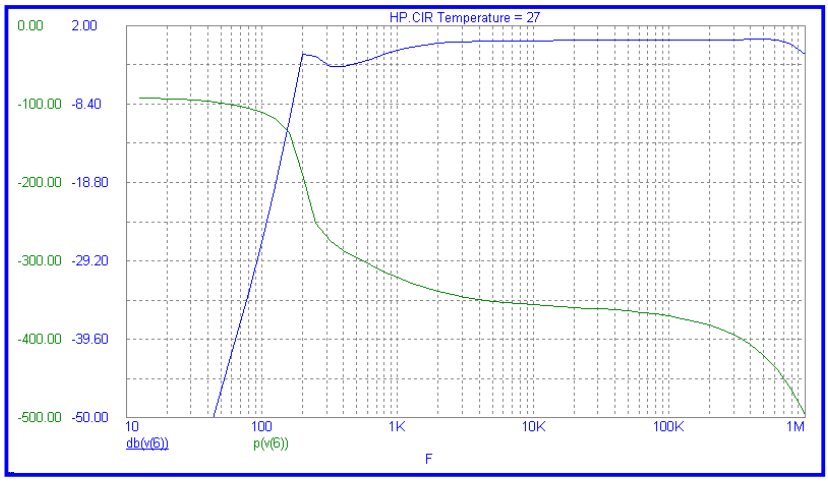


Figure 9-7: Micro-Cap V Chebyshev Highpass Filter

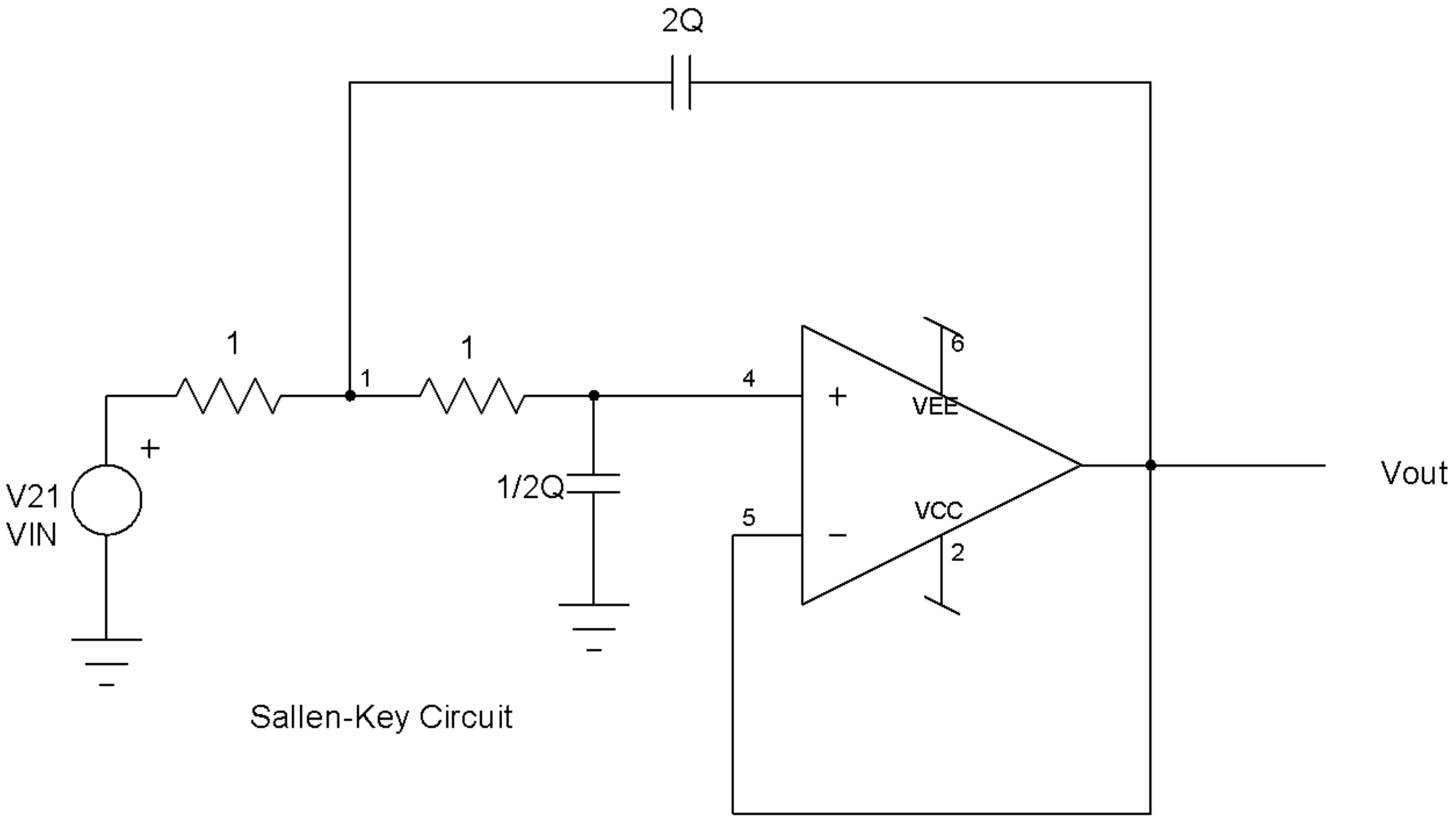
Table 9-1: Spice Statistics

Simulator	File Name	Run Time
Pspice	hp_2	2.93 Sec
Micro-Cap V	hp	1.728 Sec
Ispice	hp_n2	1.166 Sec

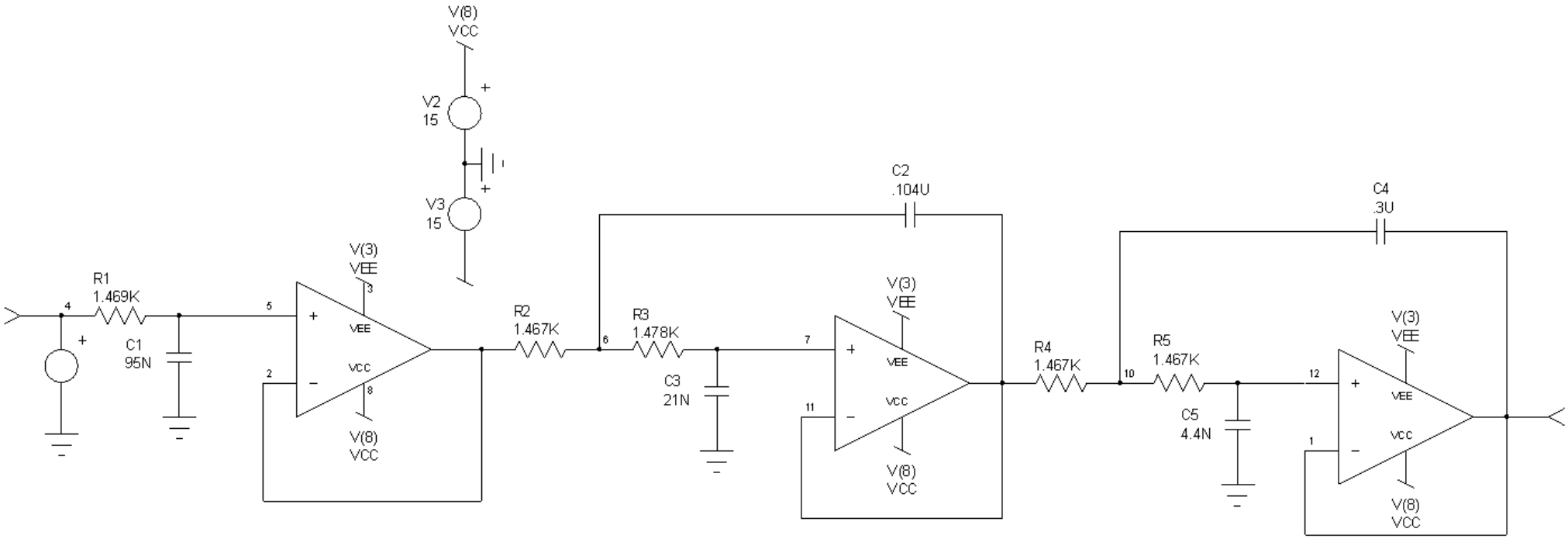
References

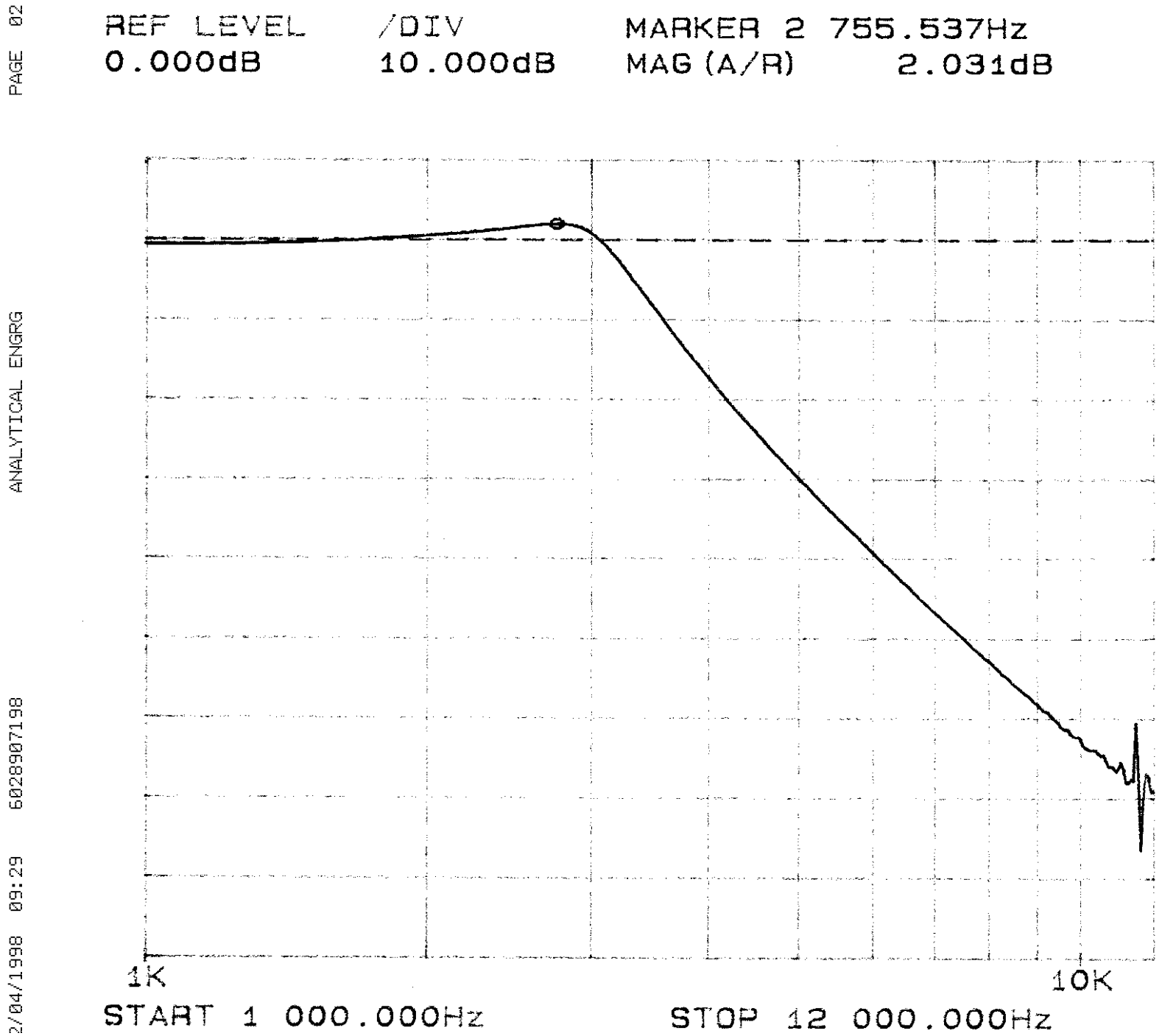
Parker, Sybil, ed. 1984. Concise Encyclopedia of Science and Technology. New York: McGraw Hill

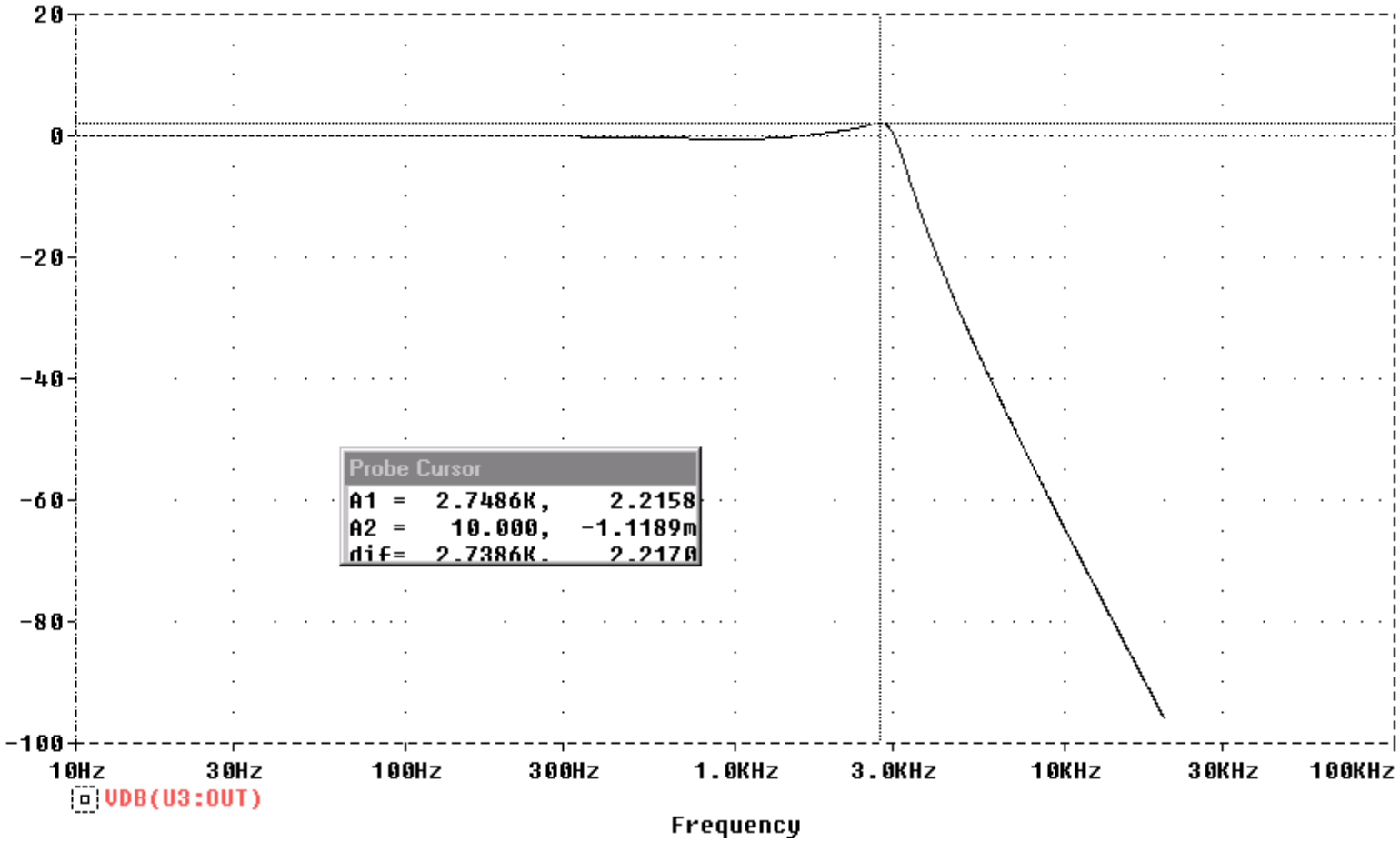
Van Valkenburg, M.E. 1982. Analog Filter Design. New York: Harcort Brace Jovanovich College Publishers.

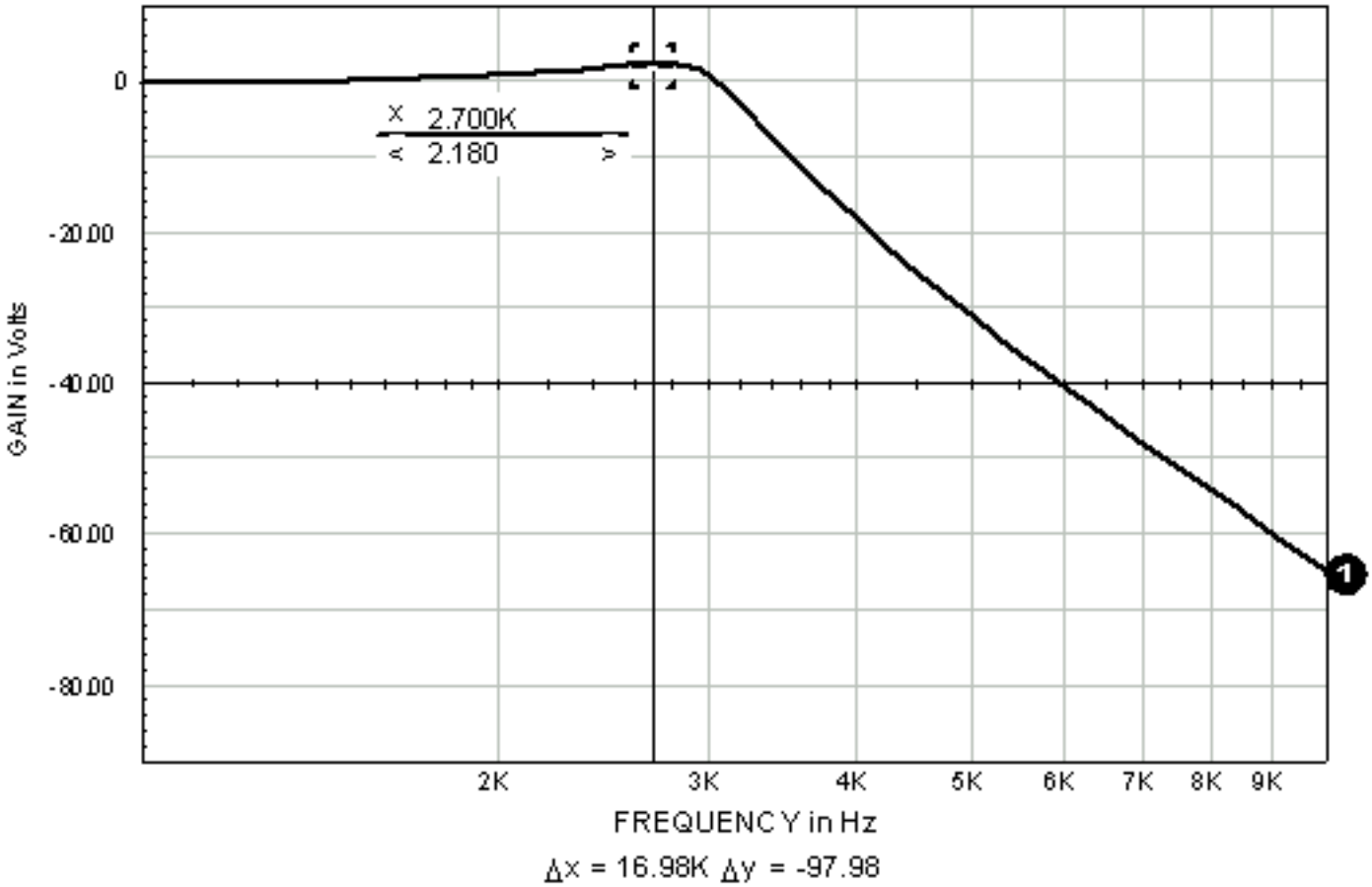


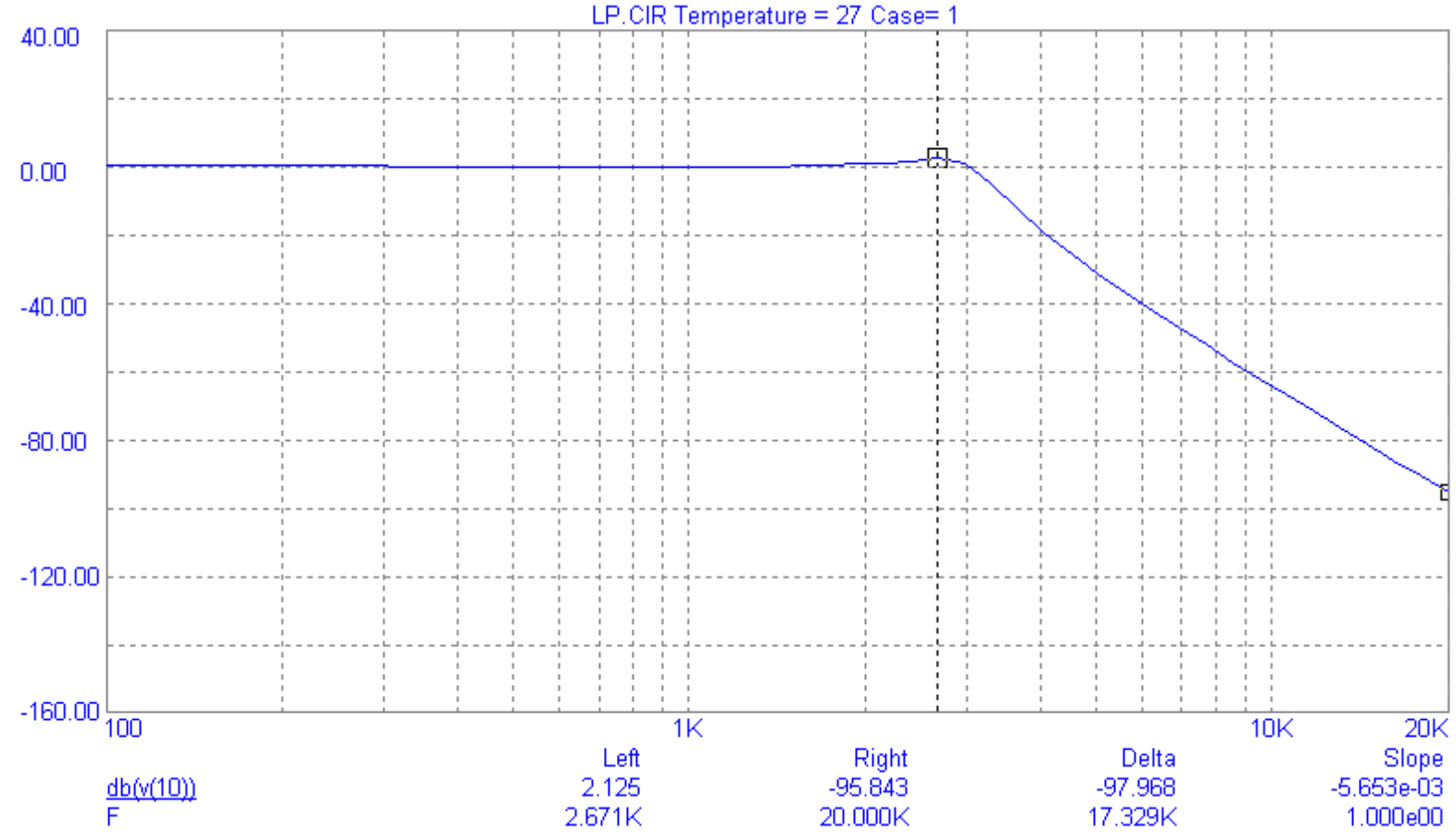
Sallen-Key Circuit


V(8)
VCC
V2
15
V3
15
R1
1.469K
C1
95N
V(3)
VEE
V(8)
VCC
R2
1.467K
R3
1.478K
C2
.104U
C3
21N
R4
1.467K
R5
1.467K
C4
.3U
C5
4.4N
VEE
VCC


REF LEVEL
0.000dB
/DIV
10.000dB
MARKER 2 755.537Hz
MAG (A/R) 2.031dB
PAGE 02
ANALYTICAL ENGRG
2/04/1998 09:29 6028907198
1K
10K
START 1 000.000Hz
STOP 12 000.000Hz


20
0
-20
-40
-60
-80
-100
Probe Cursor
A1 = 2.7486K, 2.2158
A2 = 10.000, -1.1189m
dif= 2.7386K, 2.2270
10Hz
30Hz
100Hz
300Hz
1.0KHz
3.0KHz
10KHz
30KHz
100KHz
VDB(U3:OUT)
Frequency


0
-20.00
-40.00
-60.00
-80.00
GAIN in Volts
X 2.700K
< 2.180 >
2K
3K
4K
5K
6K
7K
8K
9K
FREQUENCY in Hz
Δx = 16.98K Δy = -97.98


LP.CIR Temperature = 27 Case= 1
40.00
0.00
-40.00
-80.00
-120.00
-160.00
100
1K
10K
20K
Left
Right
Delta
Slope
db(v(10))
2.125
-95.843
-97.968
-5.653e-03
F
2.671K
20.000K
17.329K
1.000e00

#10: Electromagnetic Interference (EMI) Filter

The last filter that will be looked at in this book is the EMI filter. This filter is commonly used on the input of a power circuit to reduce conducted and reflected emissions. For instance, a flyback converter can draw current from the bus that looks like a sawtooth waveform with a peak amplitude that is dependent on the load. An EMI filter can be designed to smooth these large spikes down to where they are nearly invisible to the bus. The EMI presented in this chapter is designed for the flyback topology which converts as low as a 10 volt input to a 5 volt output.

Their are several concerns when designing an EMI filter. The parameters of the EMI filter examined in this book reflect these concerns. If the EMI filter is to be used on a converter, the input impedance of the converter must be greater then the output impedance of the filter at all frequencies. It is good practice to allow 6 dB of margin for this parameter. If the output impedance of the filter gets too close to the input impedance of the converter, it can cause problems with the stability of the converter. It may be important to note here that this output impedance is sensitive to the effective series resistance (ESR) of the output capacitors. For the hardware data taken for this unit, tantalum capacitors were used which have unspecified ESR. The ESR of a similar capacitor was measured for the simulations.

Other important characteristics of the converter are the reflected ripple attenuation, and the turn on characteristics. It is expected that the turn on characteristics will be difficult to simulate due to the non-linear characteristics of a saturating core. A non-saturating core is simply described by faradays law, and should be easily modeled by any of our spice simulators. The model used for the EMI filter is shown in Figure 10-1, and the results of each of the simulators output and the measured impedance plots are shown as Figure 10-2 through 10-5.

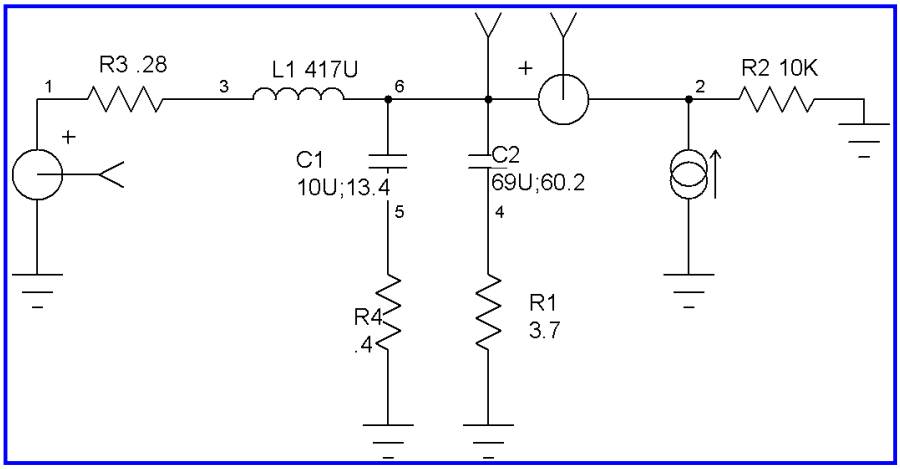


Figure 10-1: EMI filter model (linear)

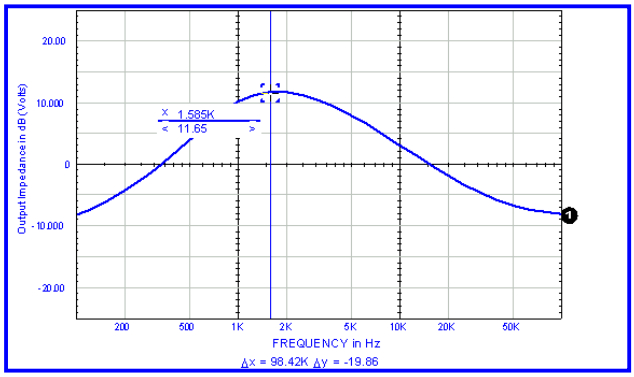


Figure 10-2: IsSpice non-linear core results of output impedance

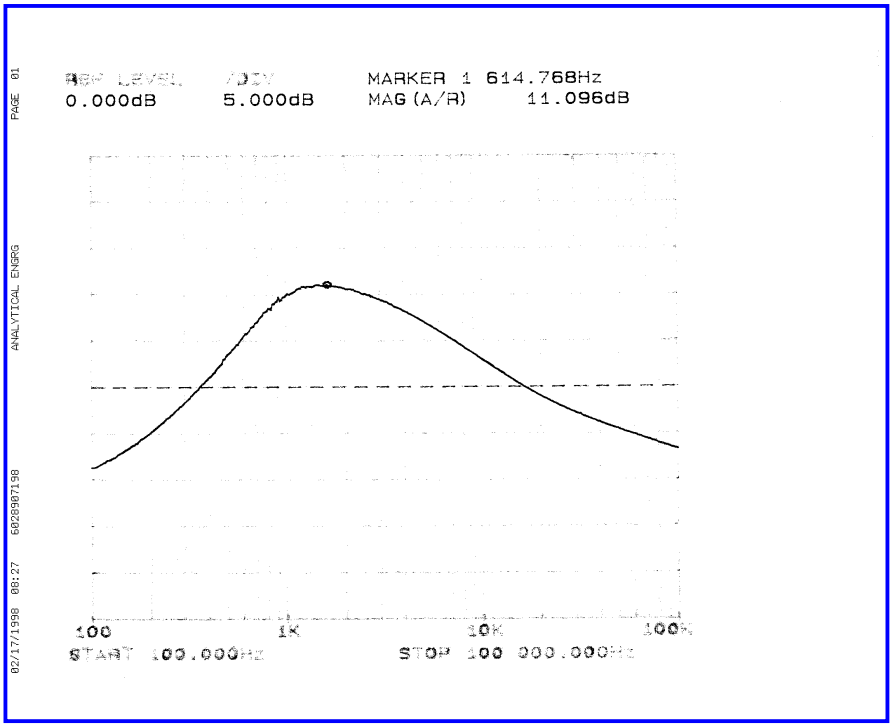


Figure 10-3: Measured results of filter output impedance

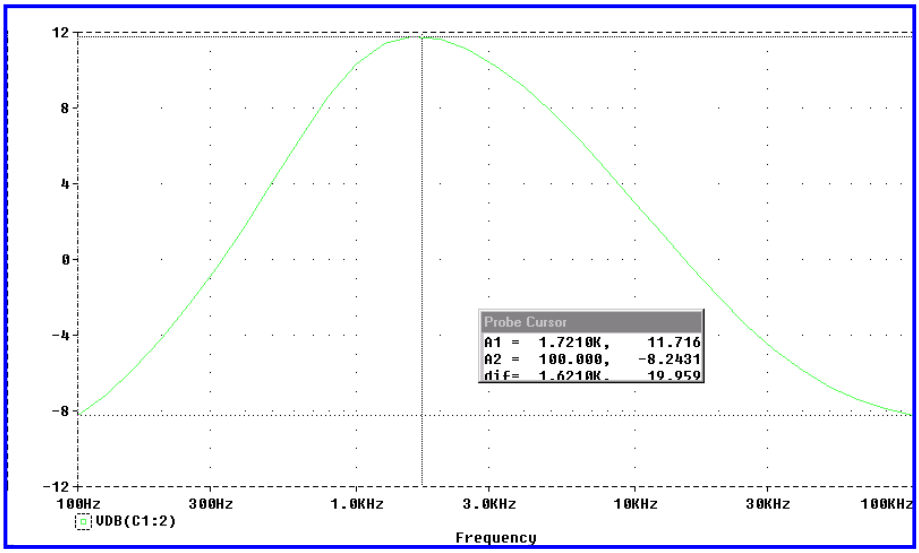


Figure 10-4: Pspice filter output impedance results

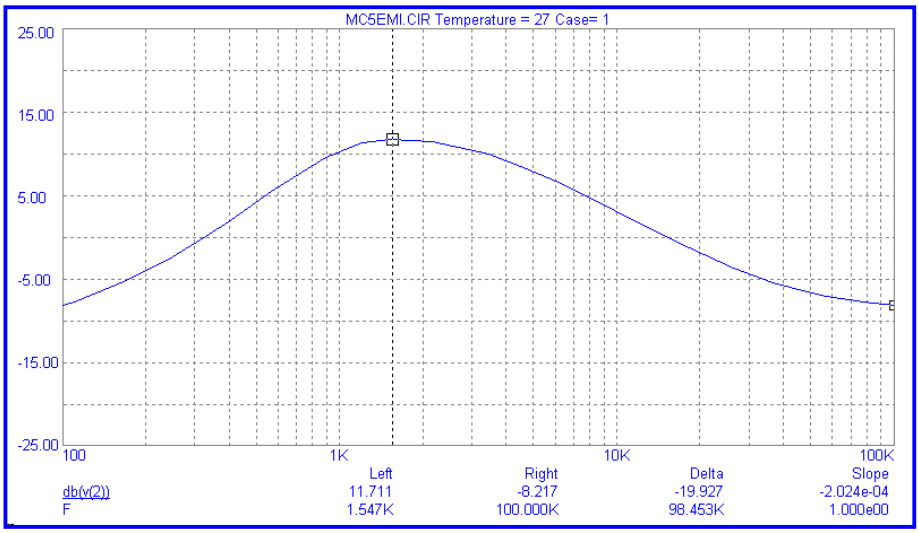


Figure 10-5: Microcap filter output impedance results

The inrush current of an EMI filter is usually examined to insure no parts are overstressed during power up. If the inductor does not saturate, the inrush current is described by faradays law and can easily be modeled by mathematics or a simple spice model. It is also not to difficult to determine if a core is saturated during turn on. A slightly more difficult calculation is to determine what the maximum current will be under a given turn on condition. The hardware used for measurements used a transformer made of two stacked 55025 cores with 40 turns around them. This was modeled in IsSpice as shown in Figure 10-6.

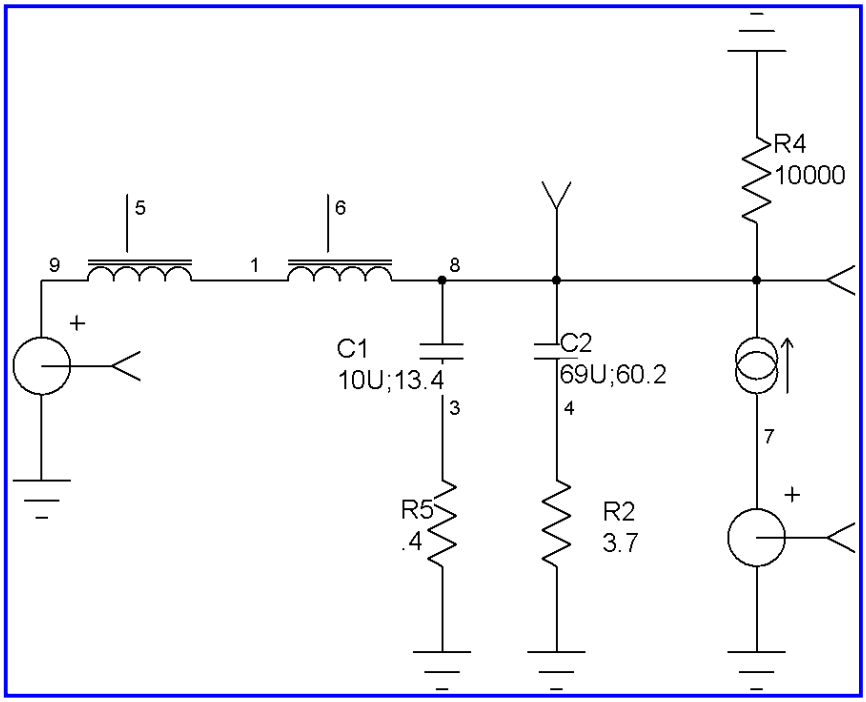


Figure 10-6: IsSpice Non-linear Core Model

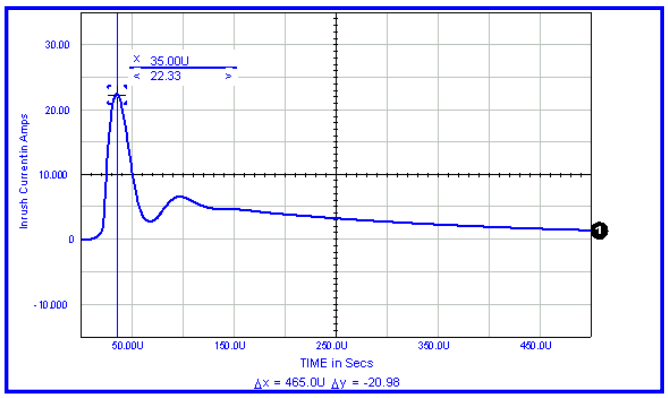


Figure 10-7: IsSpice result of non-linear model for Inrush Current simulation

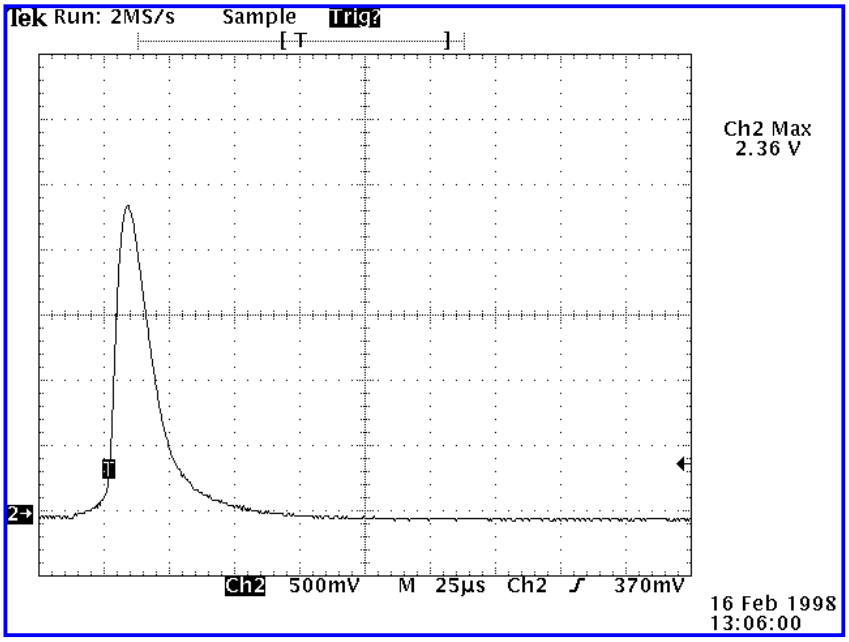


Figure 10-8: Measured results of Inrush current

Note on measured response: A current probe was used to measure the inrush current. It was set on 10 mA/mV setting which means the plot above y axis settings are in 5 amps/div.

This filter was designed to have an attenuation of 60 dB. The attenuation is calculated as 20*Log(Δ Iout/Δ Iin). Figure 10-11 shows the input verses output current waveforms to demonstrate the lowest reported attenuation.

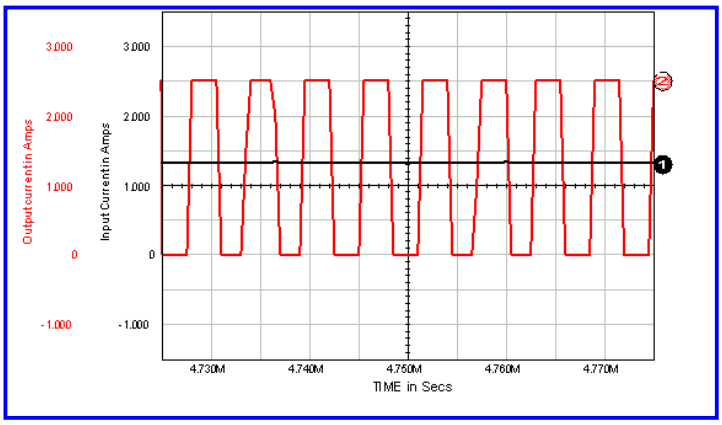


Figure 10-11: IsSpice attenuation results (Non-linear model)

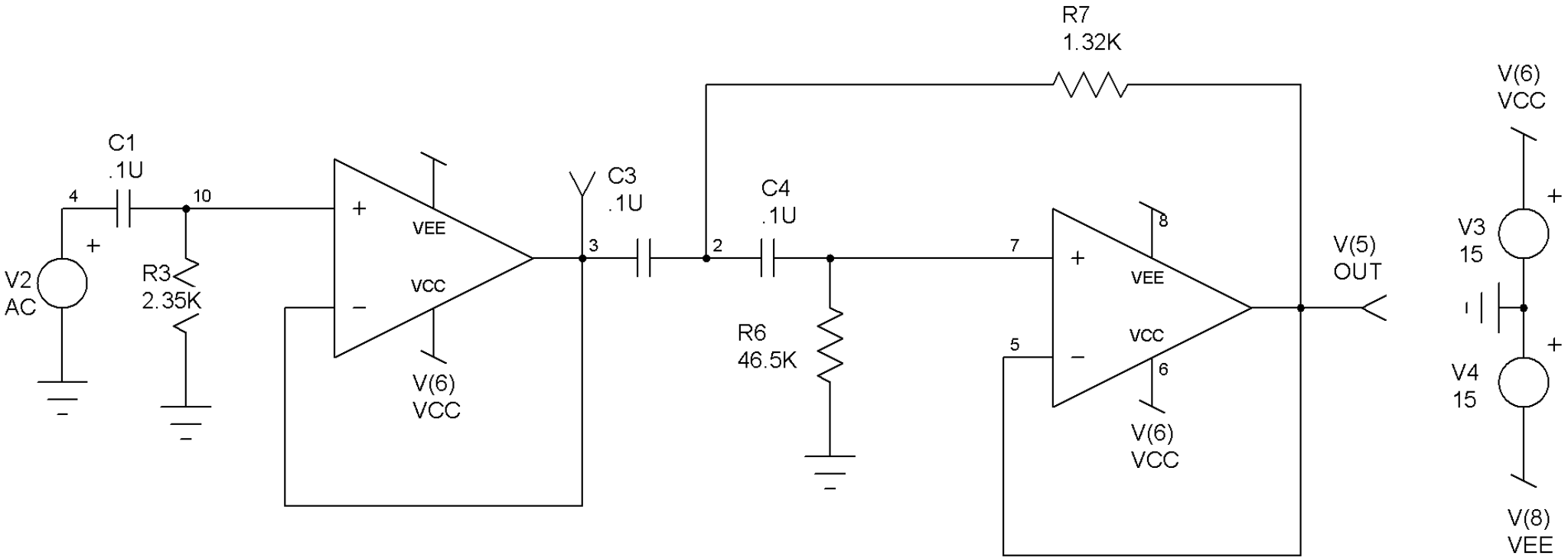
Note: Only the saturating model from IsSpice results are shown because they are the worst case attenuation. This figure is shown to give a visual representation of the effects of an EMI filter.

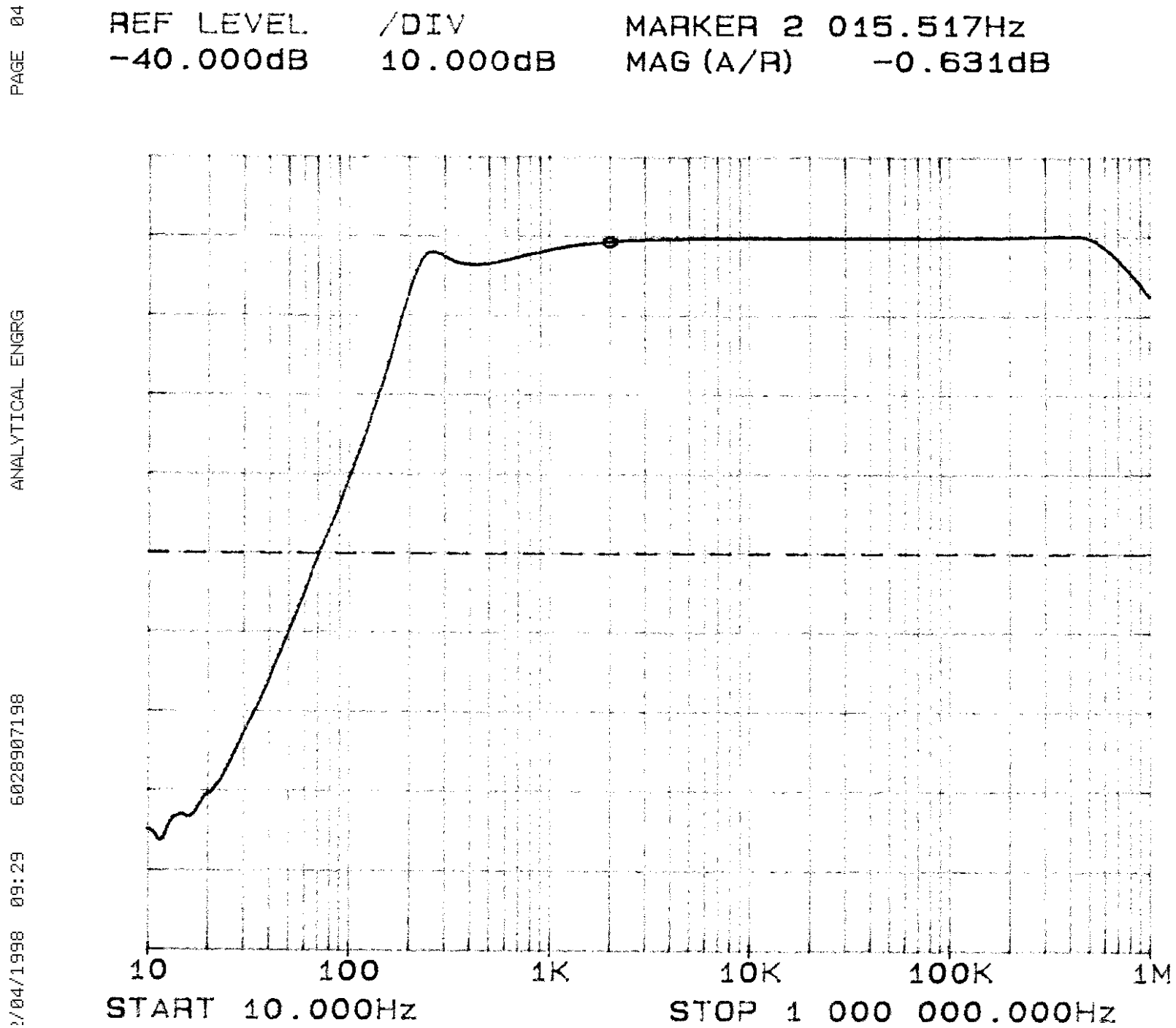
Comparison of Results						
Parameter	Conditions	IsSpice (non-saturating)	IsSpice (Saturating)	Pspice	Microcap V	Hardware Data
Output impedance		11.74 dB	11.65 dB	11.71 dB	11.7 dB	11.1 dB
Maximum inrush Current	Turn on	6.17 amps	22.33 amps	6.11 amps	6.16 amps	23.6 amps
Attenuation	Freq=170 kHz Iout=2.5 A_max Duty=50%	56.7 dB	46.7 dB	58.2 dB	58.4 dB	59.3 dB

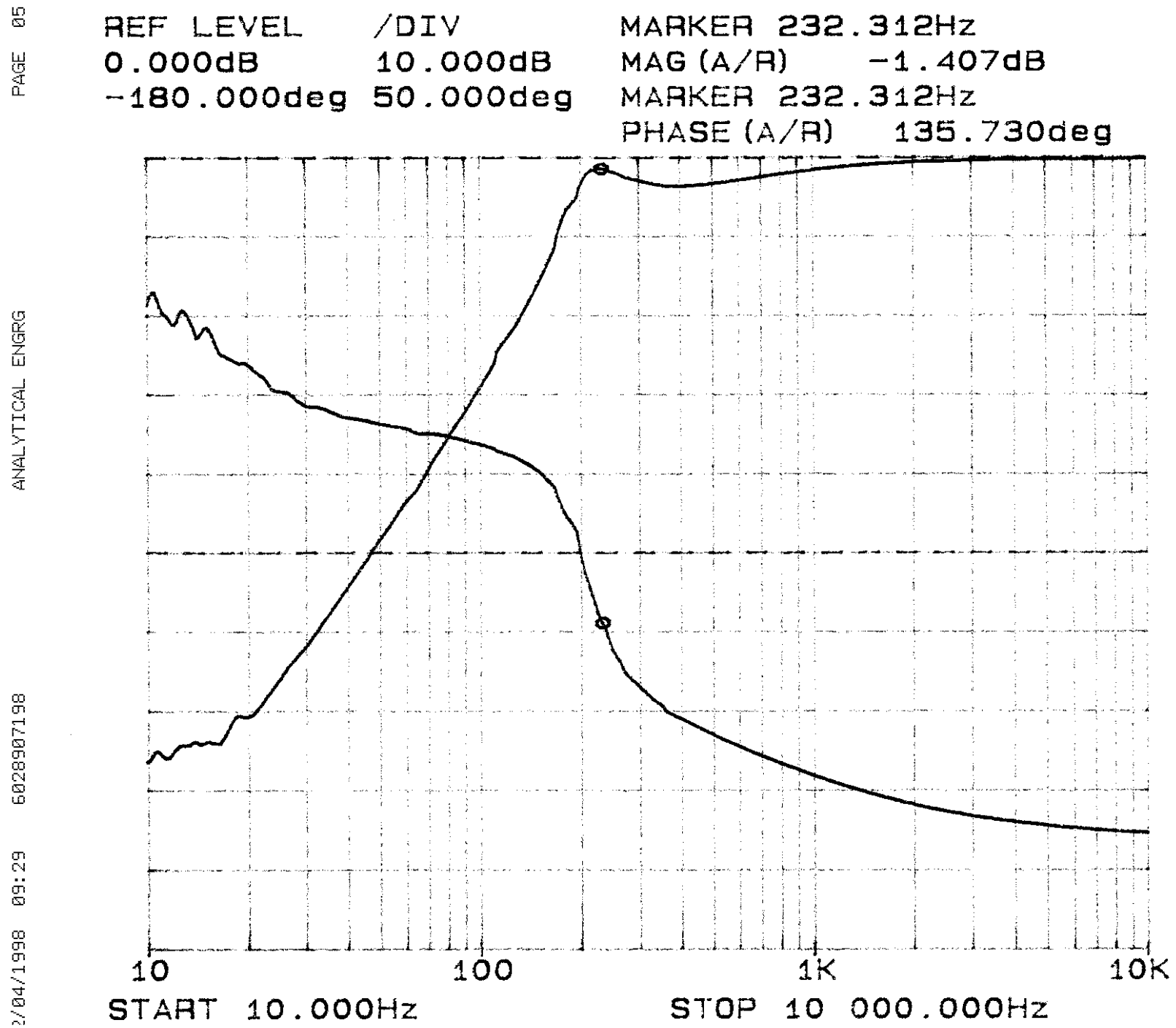
Table 10-1: Comparison of results

Run Time Summary		
IsSpice v 7.6	Pspice v 6.3	Micro-Cap V v2
15.98 sec	18.52 sec	43.45 sec
Advantages: Attenuates noise on bus for power converters.		
Disadvantages: Requires an inductor which is physically a large and expensive part.		

Filenames: Filter (IsSpice), non_emi (IsSpice), PS_emi (Pspice), MIC_emi (Microcap)


R7
1.32K
V(6)
VCC
C1
.1U
4
10
+
V2
AC
R3
2.35K
+
VEE
VCC
V(6)
VCC
C3
.1U
3
C4
.1U
2
R6
46.5K
7
8
+
VEE
VCC
5
6
V(6)
VCC
V(5)
OUT
V3
15
V4
15
+
+
V(8)
VEE


REF LEVEL
-40.000dB
/DIV
10.000dB
MARKER 2 015.517Hz
MAG (A/R)
-0.631dB
PAGE 04
ANALYTICAL ENGRG
6028907198
09:29
/04/1998
10
100
1K
10K
100K
1M
START 10.000Hz
STOP 1 000 000.000Hz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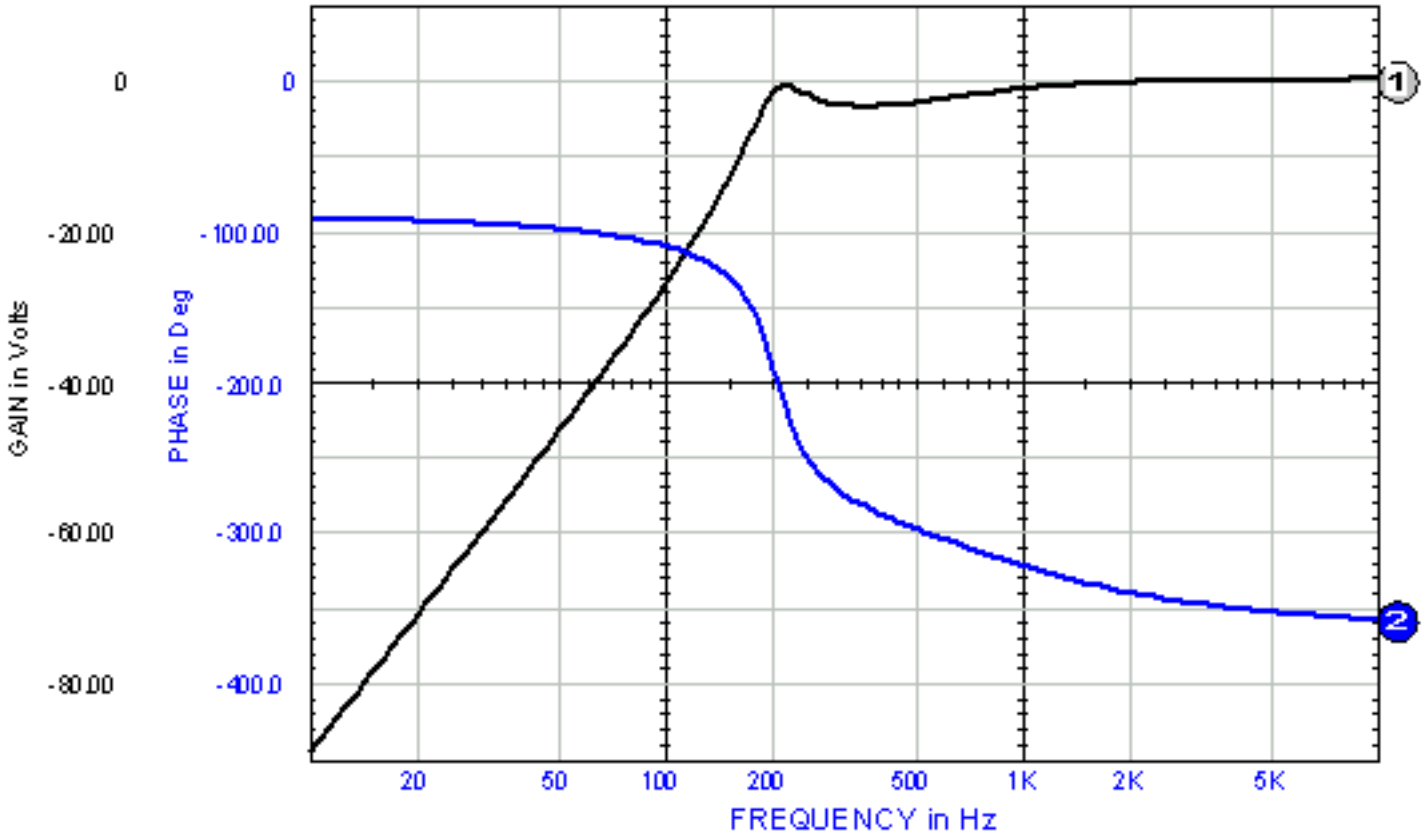
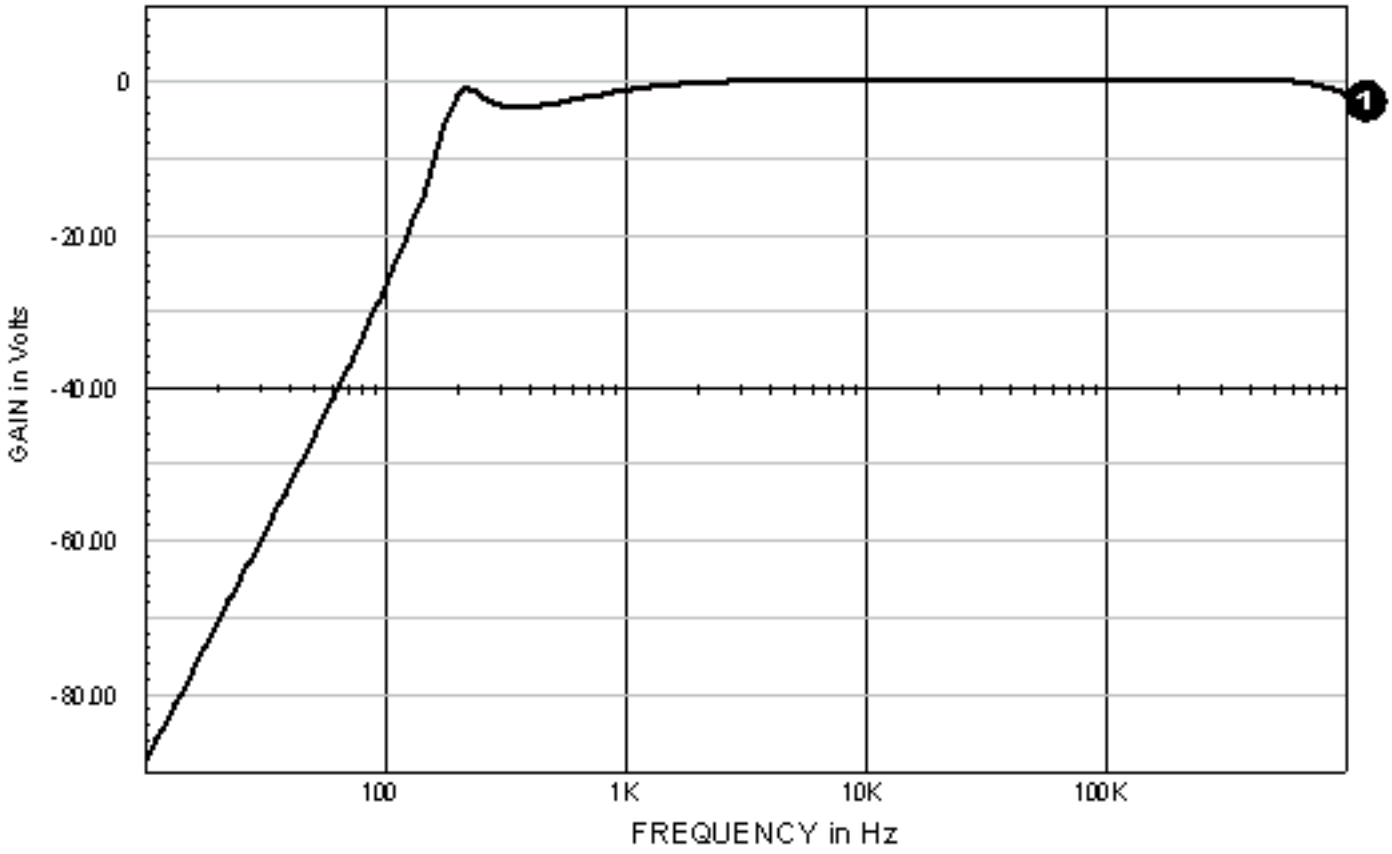
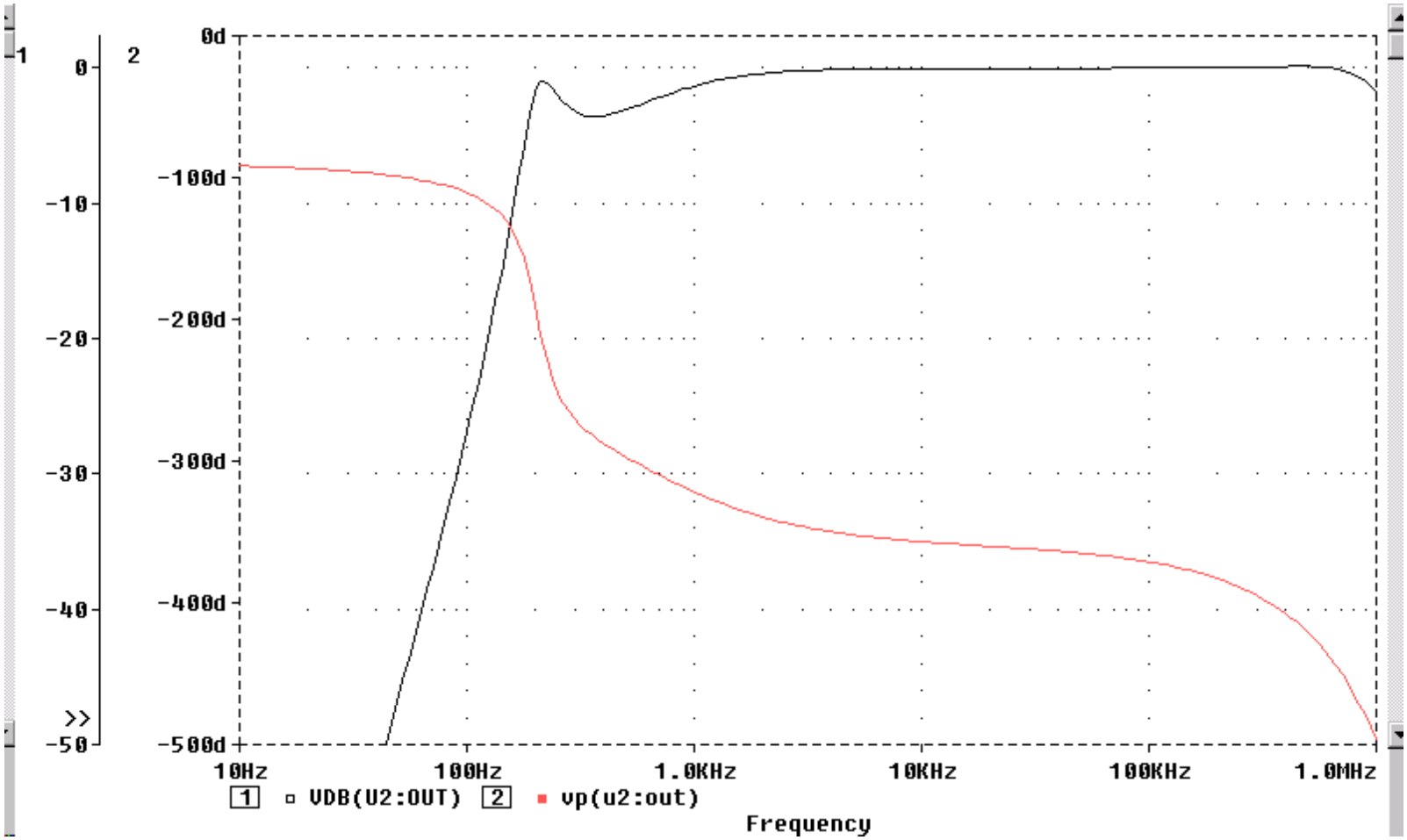
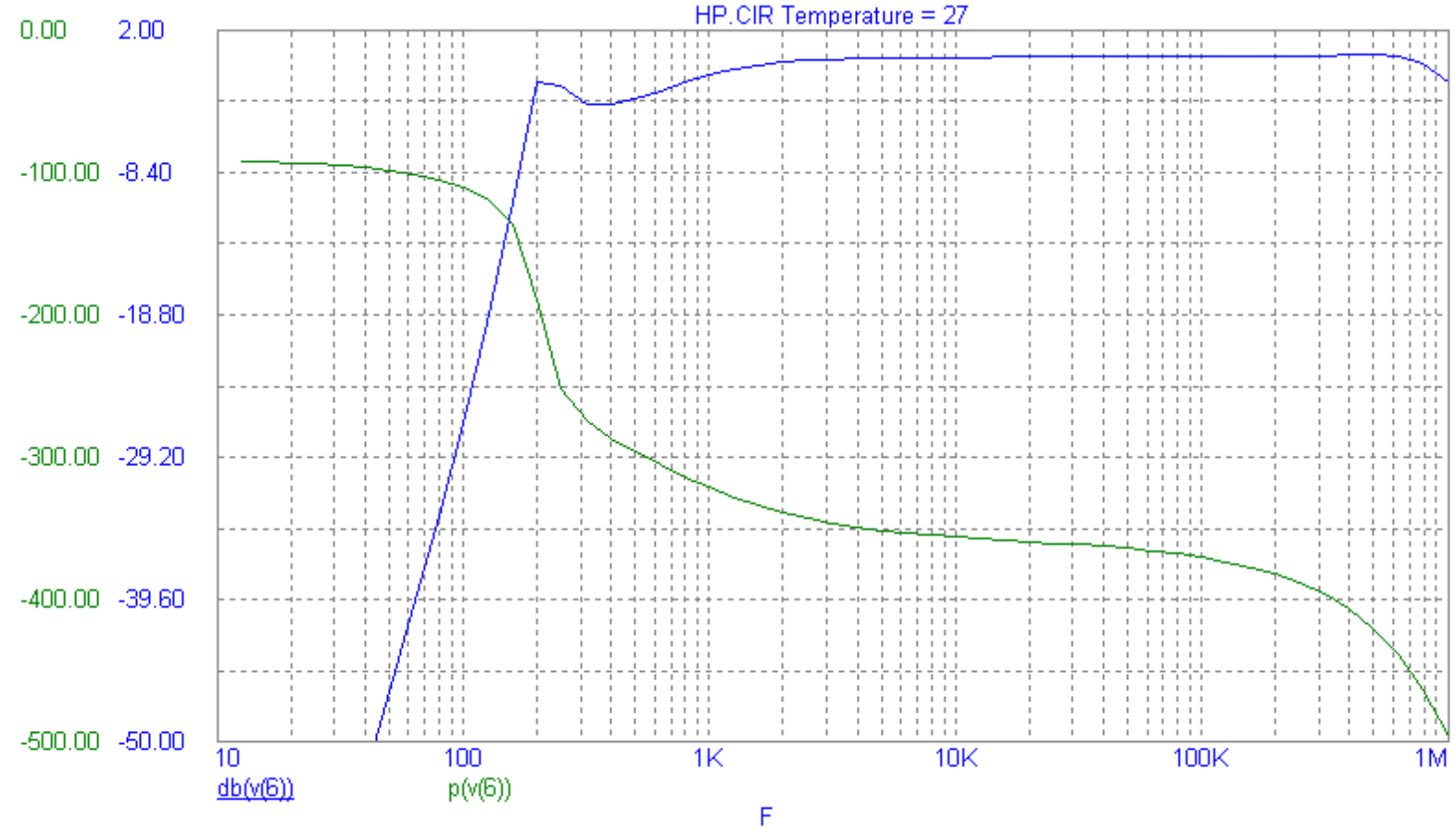
-180.000deg
/DIV
10.000dB
50.000deg
MARKER 232.312Hz
MAG (A/R) -1.407dB
MARKER 232.312Hz
PHASE (A/R) 135.730deg
10
100
1K
10K
START 10.000Hz
STOP 10 000.000Hz
PAGE 05
ANALYTICAL ENGRG
2/04/1998 09:29 6028907198


0
-20.00
-40.00
-60.00
-80.00
GAIN in Volts
0
-100.00
-200.0
-300.0
-400.0
PHASE in Deg
20
50
100
200
500
1K
2K
5K
FREQUENCY in Hz
1
2


0
-20.00
-40.00
-60.00
-80.00
GAIN in Volts
100
1K
10K
100K
FREQUENCY in Hz
1


1
2
0
-10
-20
-30
-40
>>
-50
0d
-100d
-200d
-300d
-400d
-500d
10Hz
100Hz
1.0KHz
10KHz
100KHz
1.0MHz
1 VDB(U2:OUT) 2 vp(u2:out)
Frequency


HP.CIR Temperature = 27
0.00
2.00
-100.00
-8.40
-200.00
-18.80
-300.00
-29.20
-400.00
-39.60
-500.00
-50.00
10
100
1K
10K
100K
1M
db(v(6))
p(v(6))
F

Power Conversion Circuits

Power converter circuits are often the most overlooked aspect of a system. During the engineering phase, power is not a concern. There are plenty of bench power supplies scattered around the laboratory for use in breadboards. Even in SPICE, the trusty voltage source element provides infinite voltage and infinite current for new circuit designs.

Unfortunately, when the time comes to put the system together, it is remembered that without circuits to condition the power to the system, the system is of little use to anyone. Operational amplifiers frequently need positive and negative DC voltages to operate correctly; amplifiers need both AC and DC voltages, sometimes at high currents, in order to perform their functions. Window comparators and precision sensors need highly accurate AC and DC voltages for the circuit to succeed in it's mission. What will power the system when the bench supplies are gone?

Luckily, there are circuits that fill all of the power requirements listed above and more. Also, SPICE can be a valuable tool in aiding the engineer in designing, troubleshooting, and characterizing power conversion circuits.

A simple definition of a power conversion circuit is a circuit that converts power source of a certain characteristic

(110 VAC, Battery voltage, Spacecraft bus) into power sources with a more desirable characteristic for an individual circuit (regulated + 5 VDC for digital logic, constant current sources). A wide variety of these circuits are presented in this chapter.

#11: LM117 Three Terminal Linear Regulator

Three terminal linear regulator devices have been popular for some time. The combination of simplicity, small package, good regulation, versatility, and reasonable price is attractive to engineers looking to optimize designs. When examining the operation of a three terminal regulator, simulation may not make much sense. An input voltage begets a regulated output voltage. Why simulate this? The answer may be explained below.

The following circuit (Figure 11-1) is a typical application configuration for an LM117 circuit. The input voltage is 22 volts DC. Resistors R1 and R2 set the regulated output voltage at 16.7 volts.

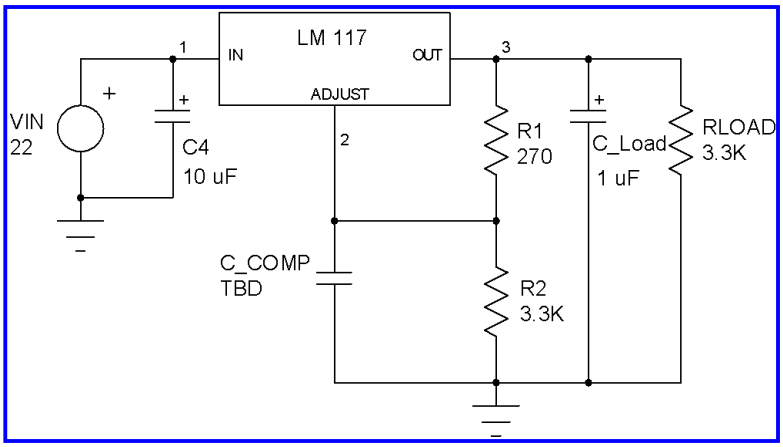


Figure 11-1: Typical application for an LM117 Three terminal linear regulator

One interesting measurement that can be made on this component would be the stability. In order to measure the stability in the lab, a special test configuration was used. This test set up is shown in Figure 11-2. The injection signal must be kept very small (700 uV is suggested) and the measurement probes should be placed at R and A on the diagram in Figure 11-2 as shown, with the ground referenced to the output (make sure the power supply in not tied to earth ground).

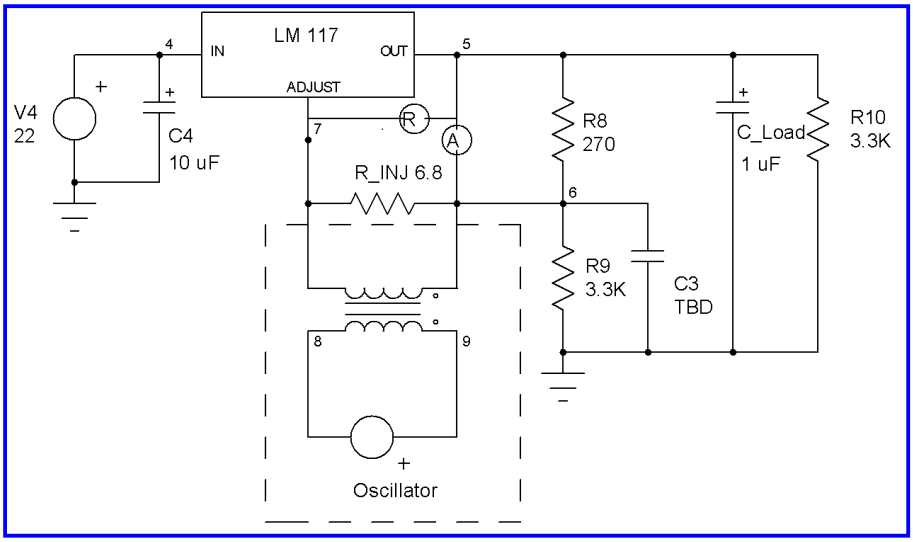


Figure 11-2: Stability measurement setup for three terminal regulator

Using the test set up in Figure 11-2, several configurations were measured on the breadboard. The cases will be measured one at a time, with comparisons to the SPICE results at each case. The first case is the recommended operational use by the Linear Technology ® databook [page 4-137, Linear Technology]. Linear recommends a 1 uF tantalum input bypass capacitor, a 1 uF capacitor at the output, and a 10 uF capacitor at the adjustment pin. The recommended type of capacitor is a solid tantalum. The SPICE configuration for testing stability is shown in Figure 11-3.

Click Here to see the larger Image

Figure 11-3: SPICE Stability measurement setup for three terminal regulator

The resulting breadboard measurement is shown in Figure 11-4. The IsSpice result at the same test configuration is shown in Figure 11-5.

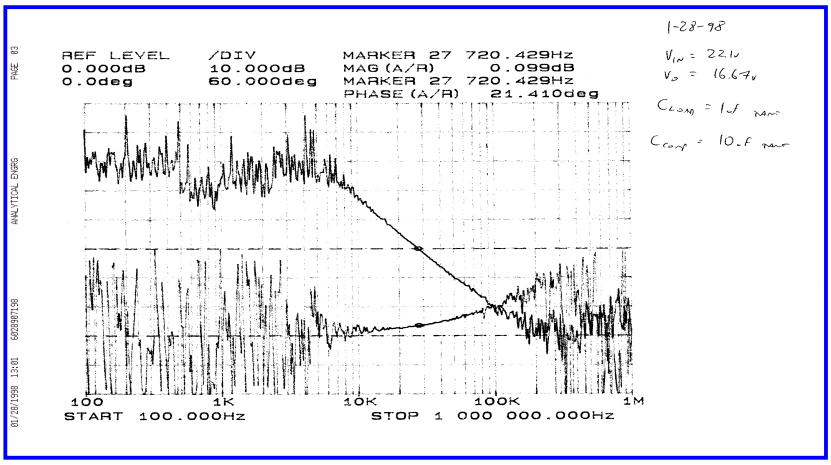


Figure 11-4: Breadboard bode plot (C_Comp=10uF)

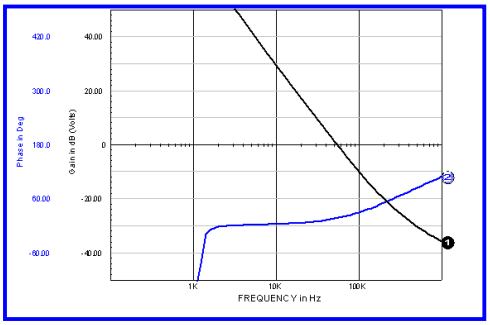


Figure 11-5: IsSpice bode plot (C_Comp=10uF)

Comparing the results of Figure 11-4 and 11-5, the phase margin is 21.4 degrees in the breadboard plot, compared to 15.85 degrees in the IsSpice plot. The crossover in the breadboard plot was 27.7 Khz, compared to 53.7 Khz in the IsSpice plot. The general shapes of the curves are also very similar.

- SPICE tip: Interestingly, there are three models of the LM117 in the Intusoft model library. One model gave the correct DC output voltage and the correct bode response. One model gave an incorrect DC output voltage but the correct bode response, and one model didn't converge. Surprisingly, all three models are transistor level. This is just another example of the necessity of testing previously unused models against their datasheet performance in order to ensure model accuracy. Incidentally, the model used in these simulations is the **LM317TI** model.

The LM117 configuration was also tested without a C_COMP capacitor. The breadboard results are shown in Figure 11-6. The IsSpice results are shown in Figure 11-7.

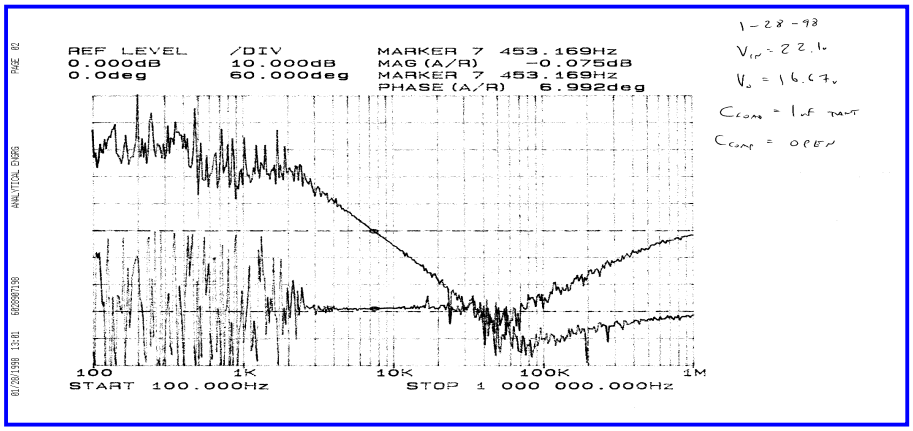


Figure 11-6: breadboard bode plot (C_Comp=open)

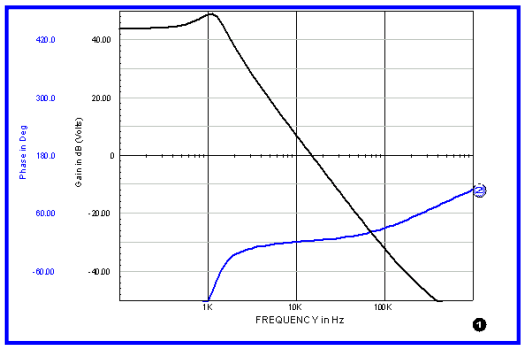


Figure 11-7: IsSpice bode plot (C_Comp=open)

The bread board phase margin and crossover frequency is 7 degrees and 7.4 Khz. The SPICE simulation phase margin and crossover frequency is 1.7 degrees and 14.7 Khz. Good engineering practice suggests a minimum phase margin of 45 degrees. The final configuration approaches this value. The C_COMP capacitor is changed to 4700 pF. The breadboard measurements are shown in Figure 11-8 while the IsSpice results are shown in Figure 11-9.

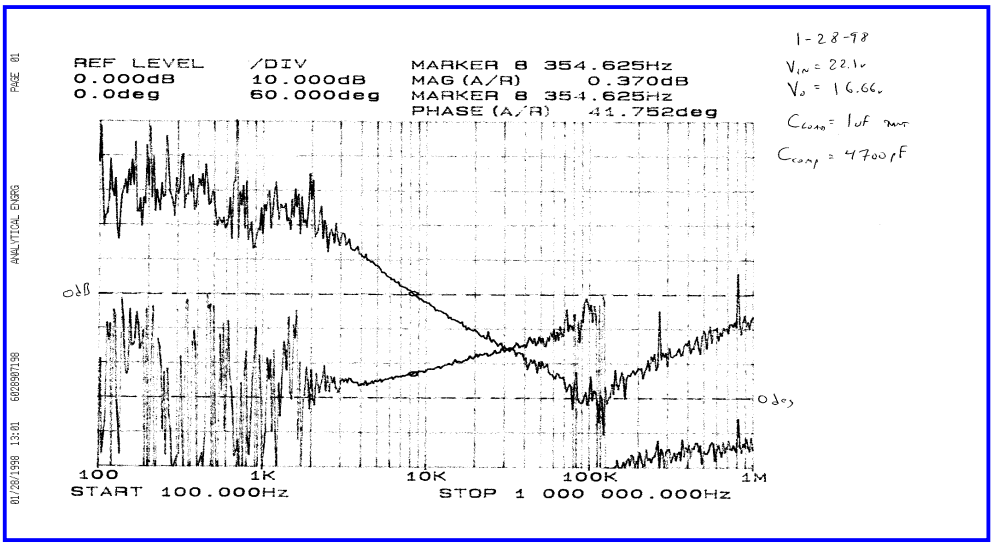


Figure 11-8: Breadboard bode plot (C_Comp=4700 pF)

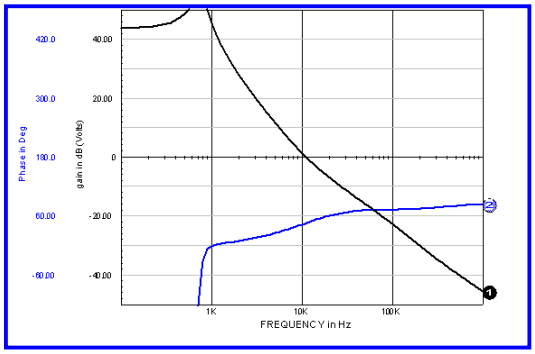


Figure 11-9: IsSpice bode plot (C_Comp=4700 pF)

The breadboard phase margin and crossover frequency is 41.7 degrees and 8.3 Khz. The IsSpice simulation results show a phase margin of 44.6 degrees and a 11 Khz crossover. Examining the results of the testing and simulation, we can conclude there is an optimal value of the C_COMP capacitor value in order to maximize phase margin and create an optimally stable three terminal regulator. An excellent tool for determining this optimal capacitance is SPICE.

- SPICE tip: The optimizer function of the SPICE simulators is tailor made for this problem. The optimization feature can be performed in Microcap by using the **STEPPING** feature in the AC menu and Pspice by using the **PARAMETRIC** sweep in the setup dialogue box. In IsSpice, the **OPTIMIZER** sweep menu is selected by selecting the SIMULATION CONTROL item in the ACTIONS menu of ICAP.

The resulting graph from the optimizer sweep is shown in Figure 11-10. Notice the optimal capacitance value is approximately a 6.8 nF capacitor which produces a phase margin of 66.5 degrees.

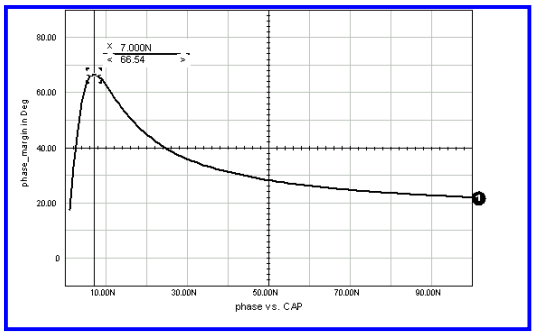


Figure 11-10: Optimizer sweep to determine optimal C_COMP capacitance

Simulations of this circuit were also performed in Microcap. The configuration shown in Figure 11-3 was simulated with a C_COMP value of 4700pF. The resulting Microcap Bode plot is shown in Figure 11-11. Simulation of the LM317 circuit in Pspice was attempted, however, the netlist contains too many transistor elements for the evaluation version.

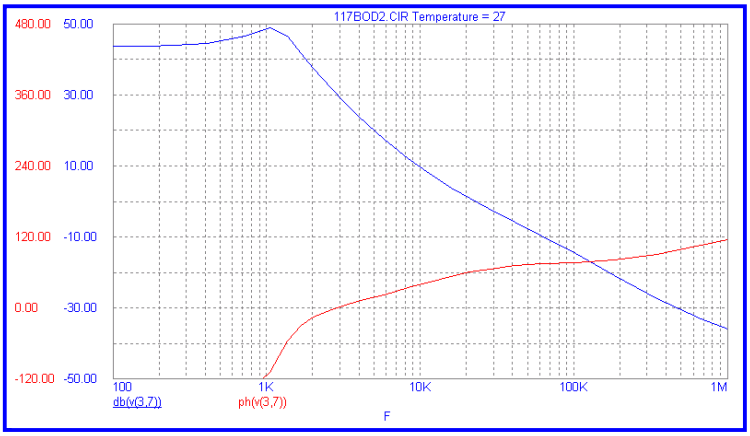


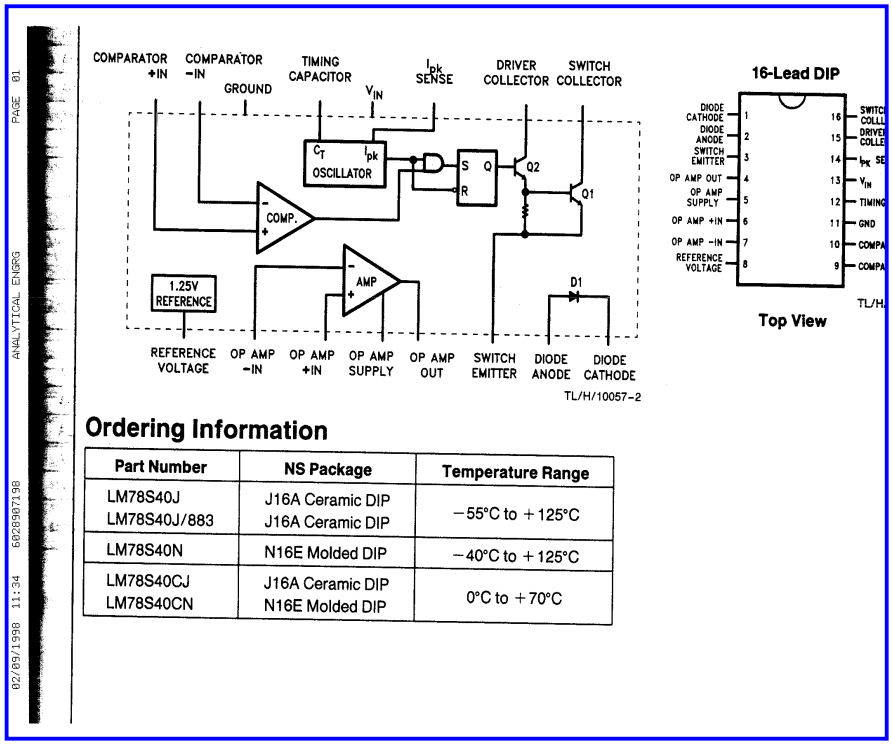
Figure 11-11: Microcap results with C_COMP=4700 pF

Run Time Summary		
IsSpice v 7.6	PsPice v 6.3	Micro-Cap V v2
1.033 Sec	xxx Sec	0.704 Sec
Advantages: low parts count, inexpensive, good accuracy, good ripple rejection		
Disadvantages: excessive power dissipation at higher currents, not as efficient as other topologies (due to headroom requirements).		

Filenames: 117Bod, 117opt (IsSpice) 117bod2 (Microcap) 117bod3 (Pspice)

#12: LM78S40 Simple Switcher DC to DC converter

Many semiconductor manufacturers make an IC that encompasses all of the necessary logic and analog circuitry required to construct a switching regulator circuit. An example of this universal approach to design is the National ® LM78S40 IC. This IC contains an oscillator, temperature compensated precision voltage reference, Mosfet driver logic, current limiting, error amplifier, and even a built in rectifying diode. IC's like this one are excellent for DC to DC applications that require more power than a three terminal linear regulator can provide, but do not require isolation. The block diagram and connection diagram for this IC is shown in Figure 12-1. The schematic for our test circuit IC is shown in Figure 12-2. The test circuit takes a DC 20 volt input and provides a regulated 10 volt DC output.



Ordering Information

Part Number	NS Package	Temperature Range
LM78S40J LM78S40J/883	J16A Ceramic DIP J16A Ceramic DIP	−55°C to +125°C
LM78S40N	N16E Molded DIP	−40°C to +125°C
LM78S40CJ LM78S40CN	J16A Ceramic DIP N16E Molded DIP	0°C to +70°C

Figure 12-1: Block and Connection Diagrams for LM78S40 IC (Reprinted with permission from National Semiconductor ®)

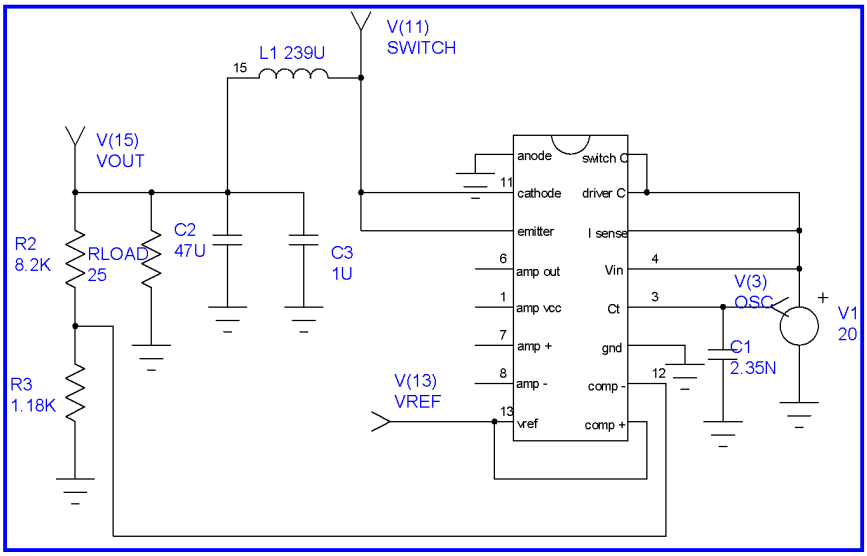


Figure 12-2: Test Schematic for 78S40 Simple switcher IC

The SPICE equivalent circuit schematic is shown in Figure 12-3. Notice the DCR (DC Resistance) of the inductor L1 has been added (R_DCR) to the circuit. Also added to the circuit is a voltage source added between the inductor and the output in order to measure current. The input voltage is pulsed from 0 volts to 20 volts in order to aid in convergence.

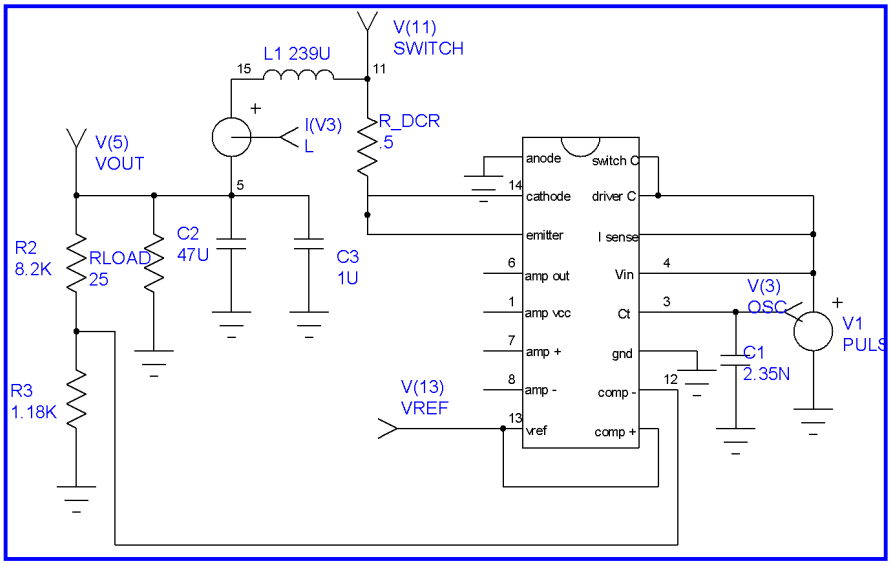


Figure 12-3: SPICE equivalent schematic for 78S40 Simple switcher IC

Also to aid in convergence, the following .OPTIONS statement is included:

.OPTIONS ABSTOL=1U ITL4=1000 ITL6=100 METHOD=GEAR

The transient simulation is run from 2.15 mSec to 2.35 mSec with a minimum time step of 50 nSec and a maximum time step of 100 nSec. The transient line also contains the UIC statement which will use the initial conditions specified in the schematic and not attempt to find a DC operating point.

The results of the breadboard waveforms and the IsSpice waveforms are compared side by side in Figures 12-4 and 12-5. Figure 12-4 shows the output ripple voltage on top, with the inductor voltage on the bottom. Figure 12-5 shows the oscillator frequency on top, with the inductor voltage on the bottom. The output voltage of the IsSpice model was 9.872, while the output voltage of the Breadboard was 9.78 volts.

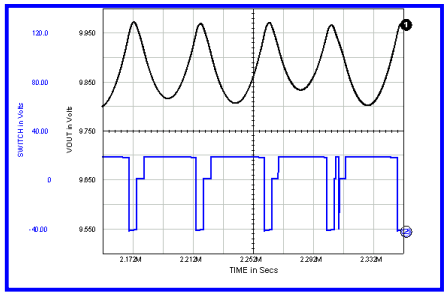


Figure 12-4A: IsSpice LM78S40 waveforms (top - output ripple, Bottom - inductor voltage)

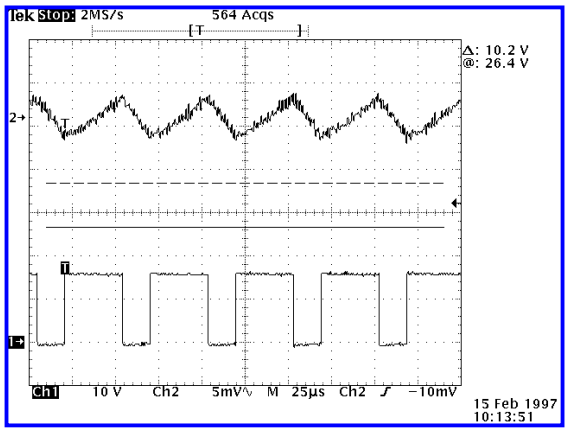


Figure 12-4B: Breadboard LM78S40 waveforms (top - output ripple, Bottom - inductor voltage)

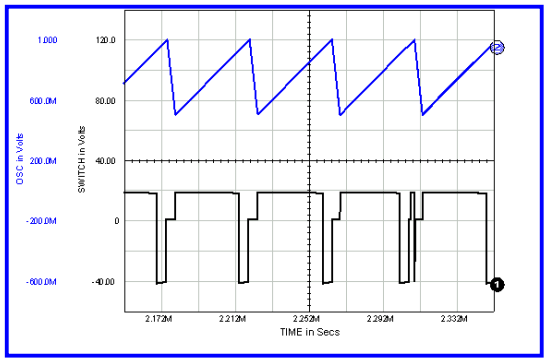


Figure 12-5A: IsSpice LM78S40 waveforms (top - Oscillator voltage, Bottom - inductor voltage)

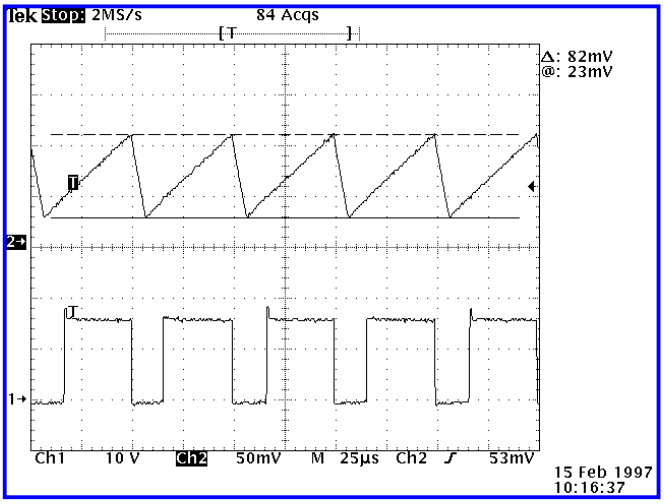


Figure 12-5B: Breadboard LM78S40 waveforms (top - Oscillator voltage, Bottom - inductor voltage)

- SPICE TIP: SPICE models for the LM78S40 were not provided in the Microcap or Pspice evaluation version software packages. This circuit was simulated using IsSpice only.

Run Time Summary		
IsSpice v 7.6	PsPice v 6.3	Micro-Cap V v2
207.3 Sec	xxx Sec	xxx Sec
Advantages: medium parts count, good output voltage line and load regulation, versatile, can provide step up or step down voltages		
Disadvantages: No isolation from input to output		

Filenames: 7840_1 (IsSpice)

#13: UA723 Hysteretic Buck Regulator

The UA723 can be configured to form a simple, low parts count Buck regulator. The UA723 is designed for use in positive or negative power supplies. This type of regulator is popular because it has excellent dynamic response. It can be configured as a series, switching, shunt, or floating regulator. The circuit has variable frequency, because it essentially an uncompensated oscillator. The output ripple is a function of the hysteresis. This comes at a cost, which is a decrease in the ability to maintain regulation. The schematic is shown in Figure 13-1. The breadboard data is shown in Figure 13-2 and Figure 13-3. The Ispice simulated data is shown in Figure 13-4 and Figure 13-5.

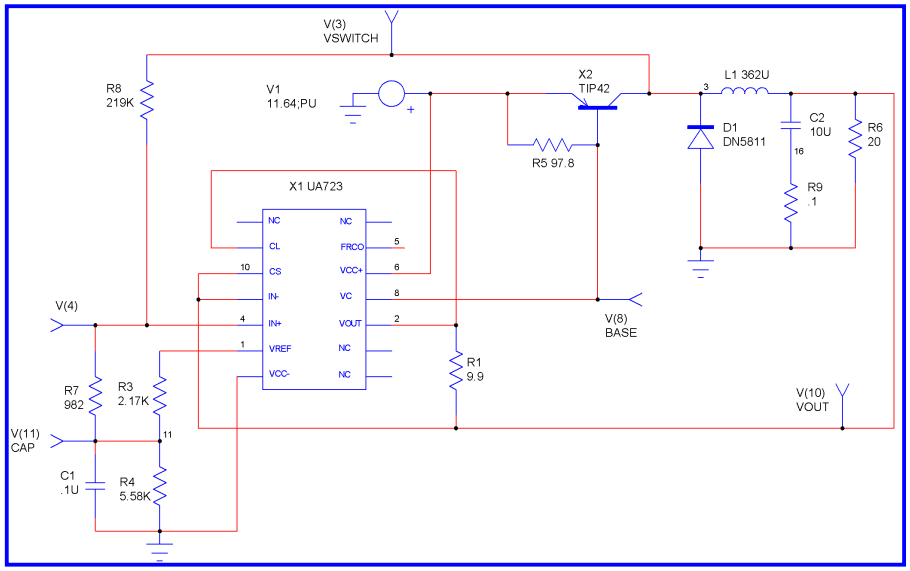


Figure 13-1: Schematic for UA723 Buck Regulator

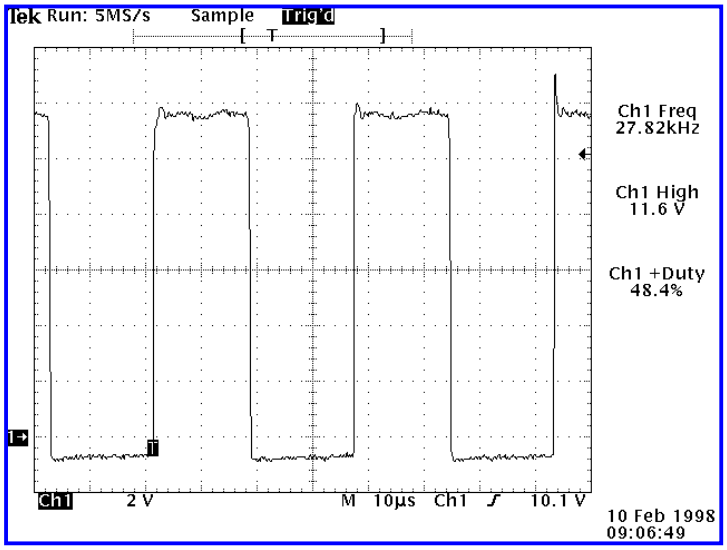


Figure 13-2: Breadboard Collector Voltage of UA723 Buck Regulator

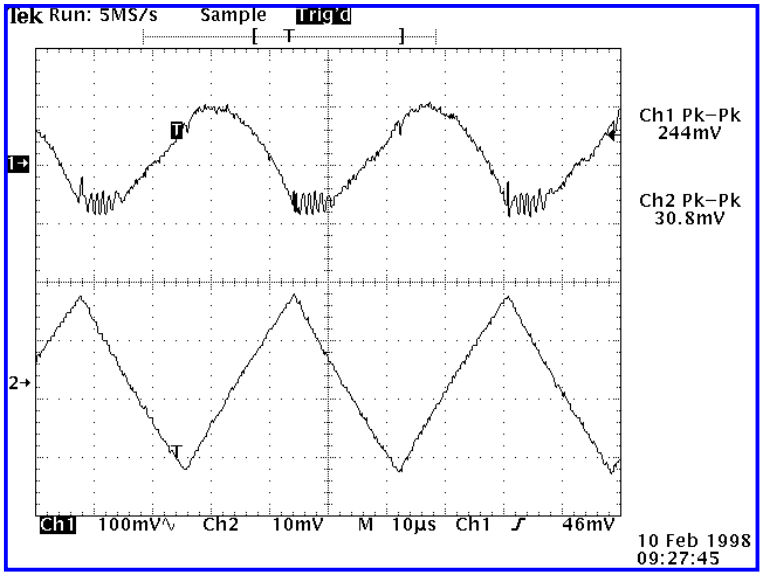


Figure 13-3: Breadboard UA723 waveforms (top - output ripple, Bottom - inductor voltage)

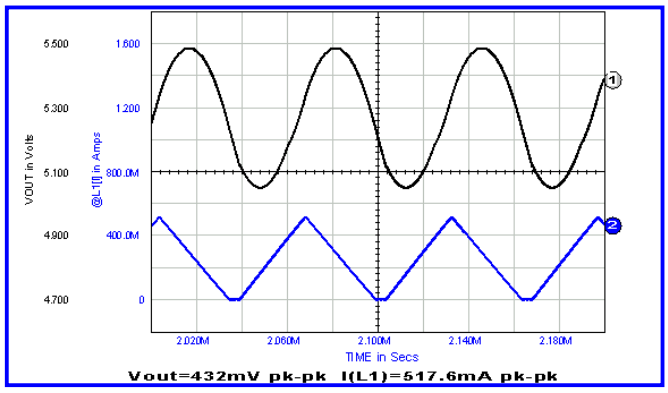


Figure 13-4: Ispice UA723 waveforms (top - output ripple, Bottom - inductor voltage)

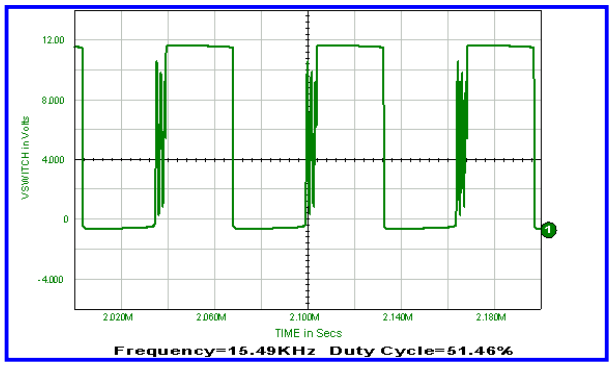


Figure 13-5: Ispice Collector Voltage of UA723 Buck Regulator

Transient domain models of a switching power supplies are extremely sensitive to the transistor model, as well as the edit controls used to govern the simulation. The turn on and turn off characteristics of the transistor model must be accurate to gain any useful information from a simulation, especially at higher frequencies. Convergence can be a major factor in the simulation of a transient domain model. By loosening the restraints on the numeric integration process (RELTOL, VNTOL, ABSTOL), convergence may be achieved, as well as a faster simulation times, at the expense of accuracy. Once convergence and proper simulation results has been established, simulation accuracy can be increased over a shorter run time to obtain accurate results, which was done in the previous simulation results. The simulation was performed substituting transistor TIP-42, with a QSB1071A. The results of this simulation, which is shown in Figure 13-6 and Figure 13-7 correlate better to the measured data. The only difference is the transistor model. To illustrate the importance of the .OPTIONS statement, the original simulation of circuit shown in Figure 13-1 was simulated with the following .OPTIONS statement:

.OPTIONS METHOD=GEAR RELTOL=.01 GMIN=1N

This was changed from the previous .OPTIONS statement of :

.OPTIONS METHOD=GEAR RELTOL=.001

The results of this simulation are shown in Figure 13-8. Notice the shape of the TIP-42 collector wave form.

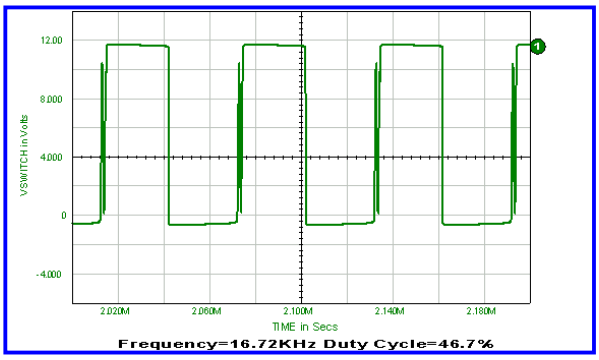


Figure 13-6: Ispice Collector Voltage of UA723 Buck Regulator With QSB1071A

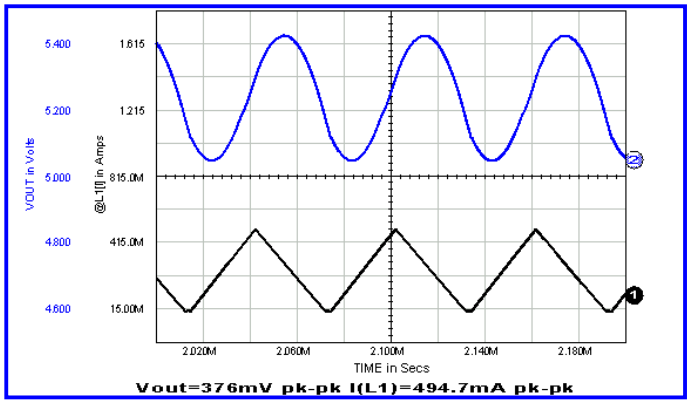


Figure 13-7: Ispice UA723 waveforms (top - output ripple, Bottom - inductor voltage) With QSB1071A

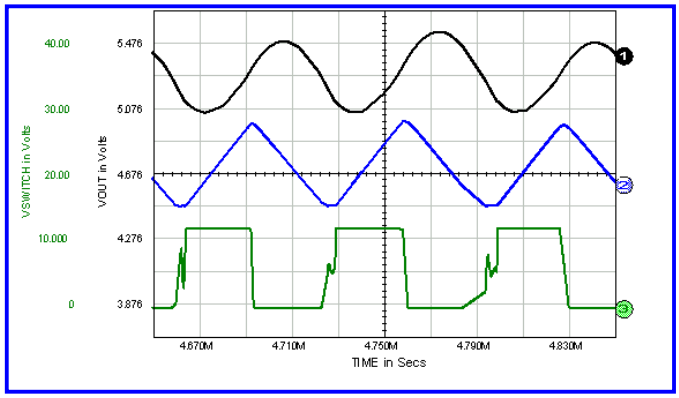


Figure 13-8: Ispice UA723 waveforms (top - output ripple, Bottom - inductor voltage) With TIP-42

Condition	Breadboard	TIP-42	TIP-42*	QSB1071A
Frequency	27.82KHz	15.49KHz	14.29KHz	16.72KHz
Vout pk-pk	244mV	422mV	626mV	376mV
Vout	5.22 V	5.27 V	5.28 V	5.24 V
Inductor Current	308mA	517.6mA	550.8mA	494.7mA
Run Time	NA	82.93 Sec	27.31 Sec	68.42 Sec

Table 13-1:Summary of Results

*.OPTIONS METHOD=GEAR RELTOL=.01 GMIN=1N

The results indicate a trade off between simulation run time and simulation accuracy. Also, the selection on the transistor can have dramatic effects on the results of the simulation.

The simulation results do not correlate well to the hardware. A possible cause is the ESR of a Mallory TDC106K505WSG 10uF capacitor, C2. The feedback loop is originated at the collector of the PNP transistor to avoid sensitivity to the ESR of the output capacitor. However, investigation into the poor correlation indicates that the circuit is sensitive to the ESR of capacitor C2. A measurement of the ESR was made using a HP 3577A network analyzer, which is shown in Figure 13-10.

The setup to make the measurement of capacitor C2, inverted the signal, which is why the ESR measurement is inverted. The ESR of capacitor C2 is dependant on frequency. The hardware frequency is approximately 27KHz. The ESR at this frequency is approximately 386 mOhms.

Another schematic, which reflects the appropriate ESR of C2 and the DCR of inductor L1, is shown below in Figure 13-9. The schematic includes the circuitry that was used to measure the transient response of the hardware.

The measured and simulated data is shown in Figure 13-10 through Figure 13-15.

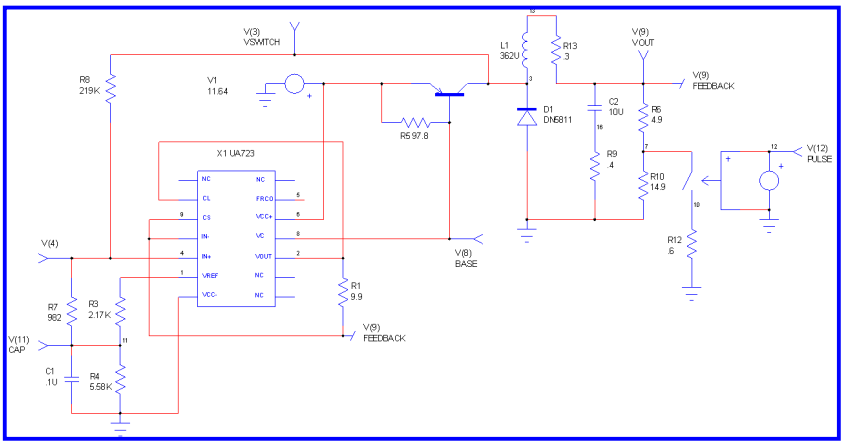


Figure 13-9: UA723 Buck Regulator with Measured ESR and DCR.

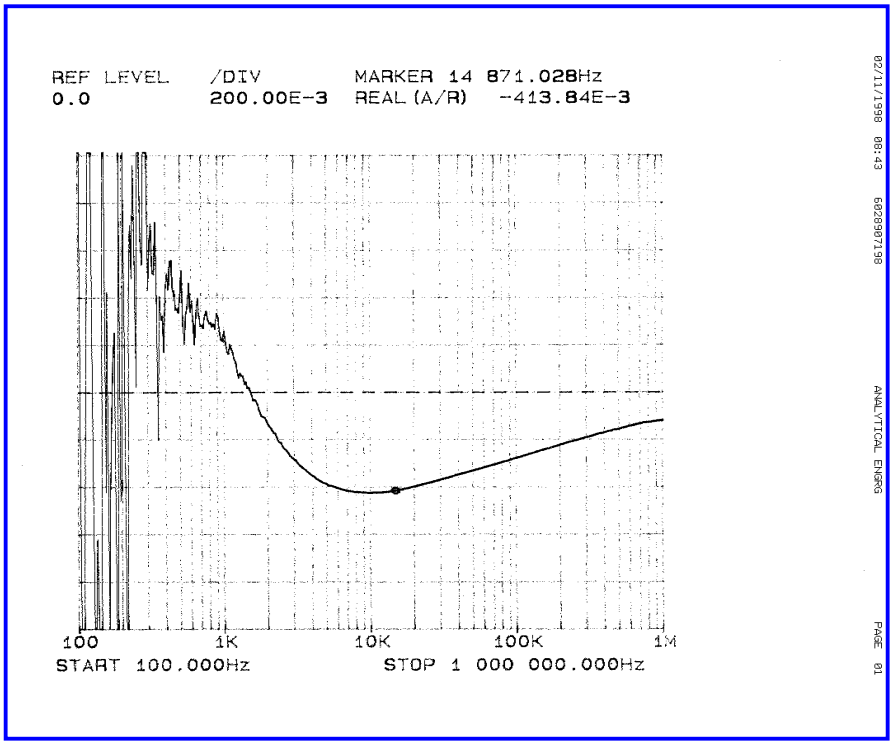


Figure 13-10: Measured ESR of C2

A precarious dilemma results when creating a model that can accurately depict a transient response of the converter as well as the output ripple. The ESR of capacitor C2 is a function of frequency. When simulating the output ripple of the converter, the frequency is essentially constant, approximately 25KHz. However, when the converter encounters a transient, the response is at a much lower frequency, approximately 5KHz. ESR for the transient response simulation is different from the output ripple simulation. The solution is to either create a capacitor model that has ESR, which varies with frequency, or change the ESR to the appropriate value for each simulation. The ESR of capacitor C2 maintains relatively constant from 5KHz through 20KHz, but varies immensely outside of these frequencies.

In correlating to the transient response, many difficulties arose. The ESR of C2 determines the magnitude of the transient response, as well as the frequency of the output ripple. Varying the ESR of C2, varies where in the period of the output ripple that the transient occurred. A larger magnitude of the transient response corresponds to the transient occurring while the transistor is conducting, which indicates that the simulation results are dependent on when the transient occurs.

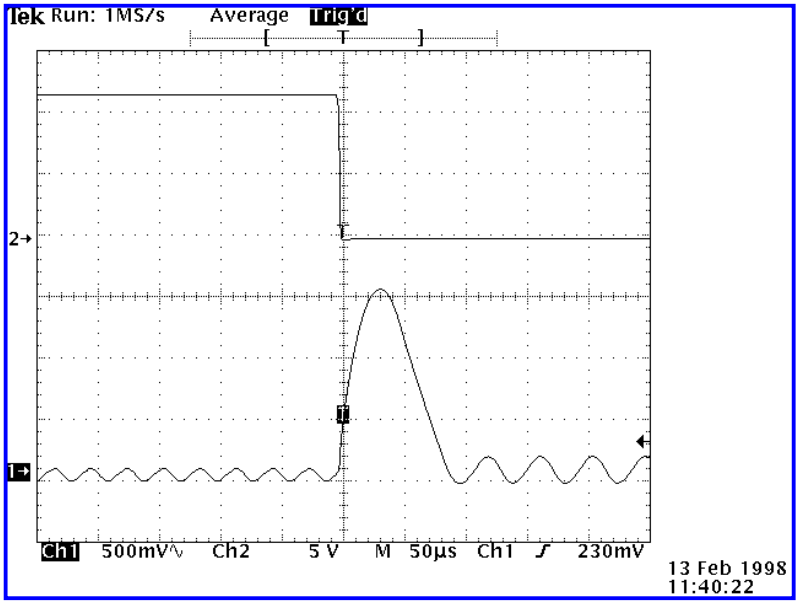


Figure 13-11: Measured UA723 Buck Regulator Transient Response

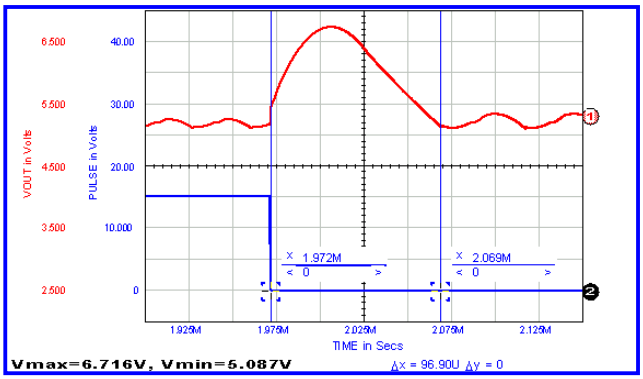


Figure 13-12: Ispice UA723 Buck Regulator Transient Response

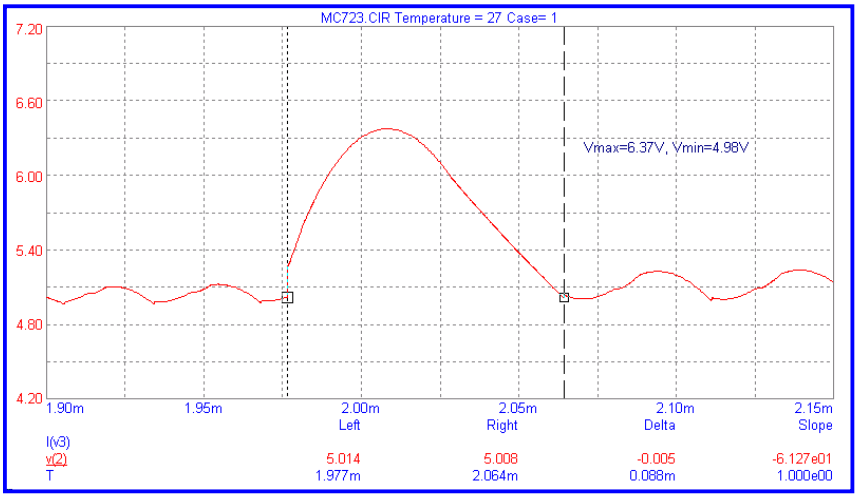


Figure 13-15: Micro-Cap V UA723 Buck Regulator Transient Response

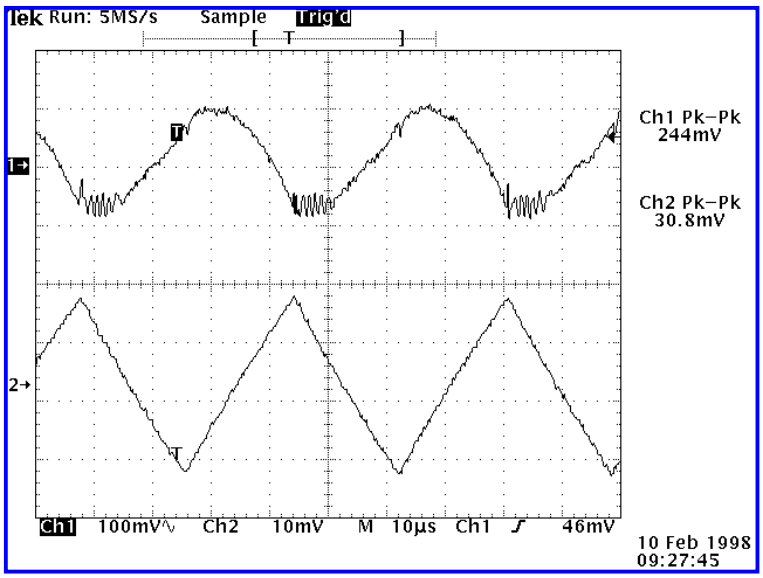


Figure 13-3: Breadboard UA723 waveforms (top - output ripple, Bottom - inductor voltage)

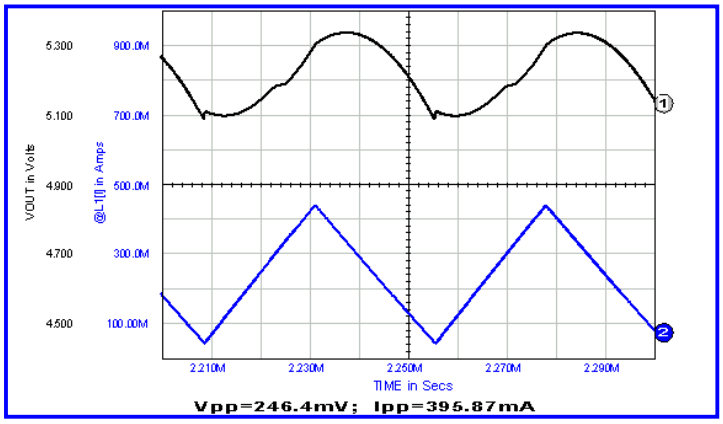


Figure 13-13: Ispice UA723 Buck Regulator Output Ripple

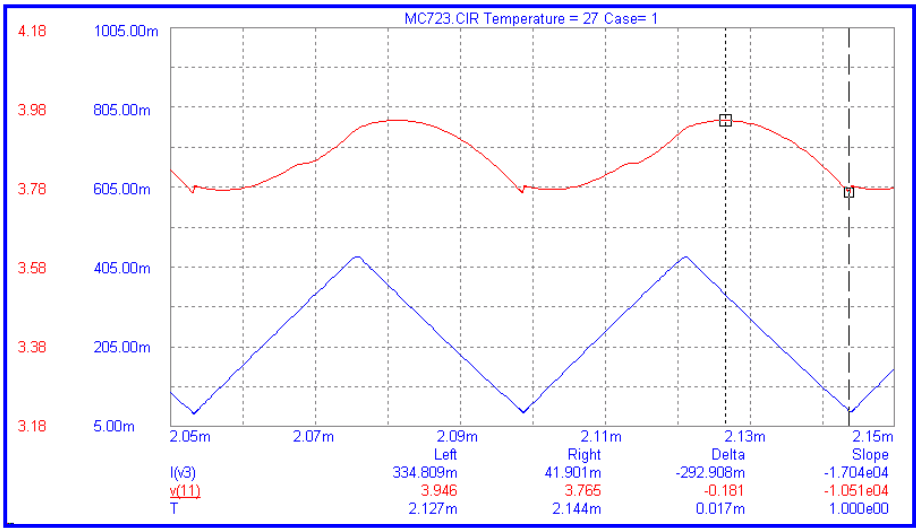


Figure 13-14: Micro-Cap V UA723 Buck Regulator Output Ripple

Condition	Breadboard	Ispice	Micro-Cap V
Frequency	27.82KHz	21.3KHz	22KHz
Vout (pk-pk)	244mV	246mV	292mV
Vout (Avg)	5.22 V	5.21	5.11
Inductor Current	308mA	395.9mA	396mA
Transient Response (pk-pk)	1.6V	1.63V	1.39V
Response Duration	90uS	97uS	88uS
Run Time of Transient Response	NA	147.88 sec	74.56 sec

Table 13-2: Summary of Results

The circuit consisted of too many nodes for the Pspice evaluation version.

References

1990 Linear Databook, Linear Technology.

1990 Linear Applications Handbook Volume I, Linear Technology.

Mimms, Forrest M. III, 1983. Getting Started In Electronics.

Parker, Sybil, ed. 1984. Concise Encyclopedia of Science and Technology. New York: McGraw Hill

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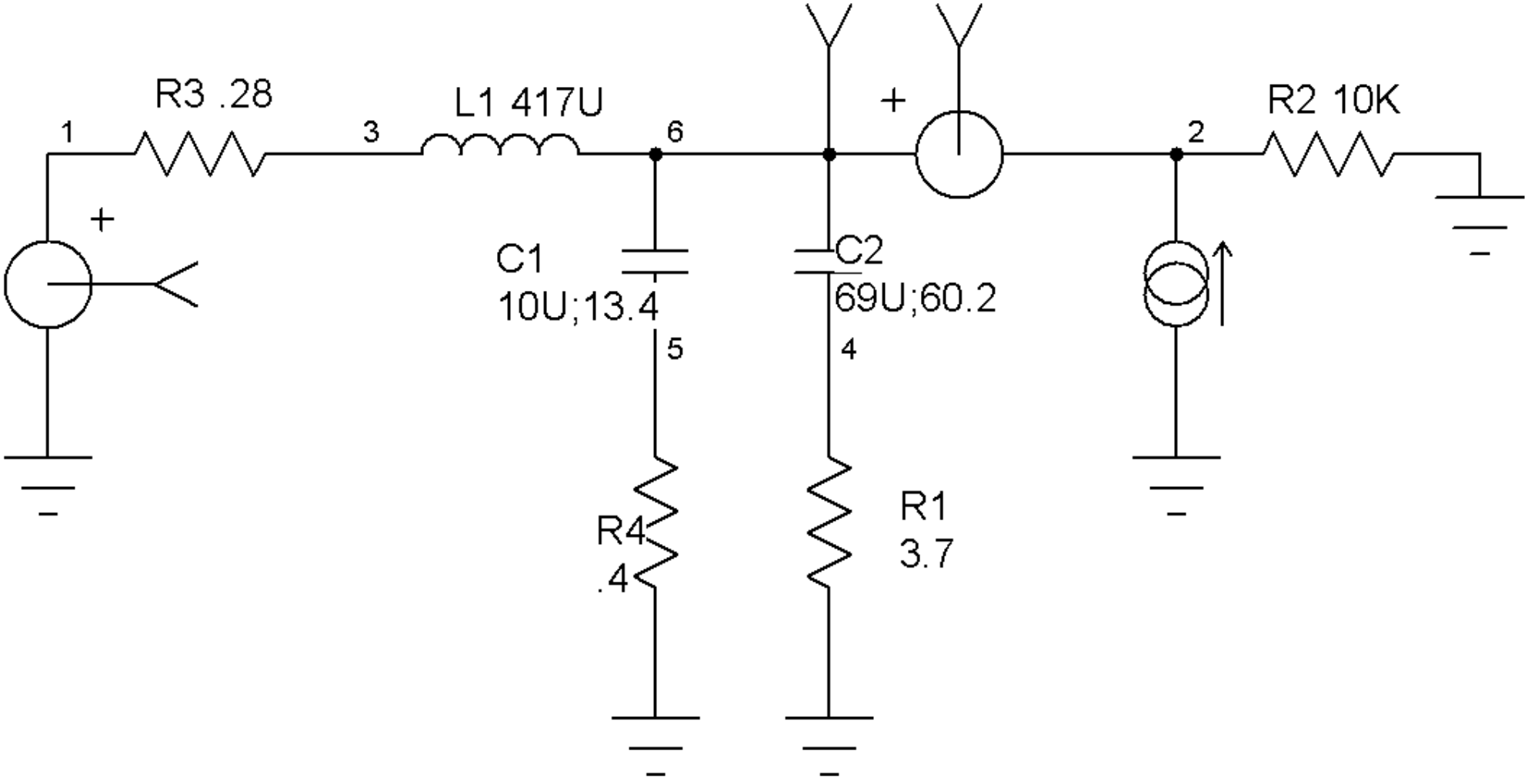
Sandler, Steven M. SMPS Simulation with SPICE. 1996. McGraw Hill.

Van Valkenburg, M.E. 1982. Analog Filter Design. New York: Harcort Brace Jovanovich College Publishers.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3
6
2
+
+
C1
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C2
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R4
.4
R1
3.7
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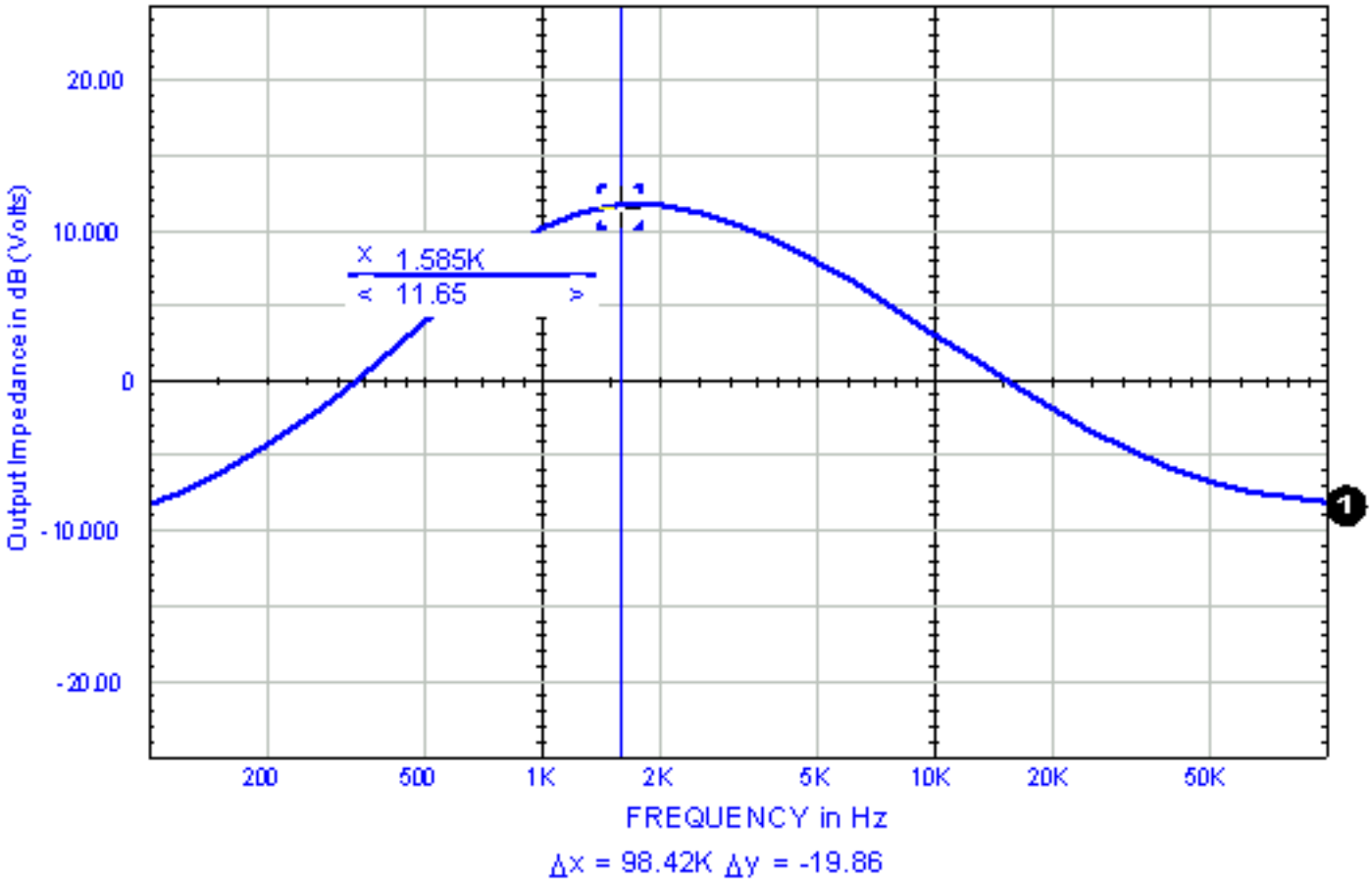
–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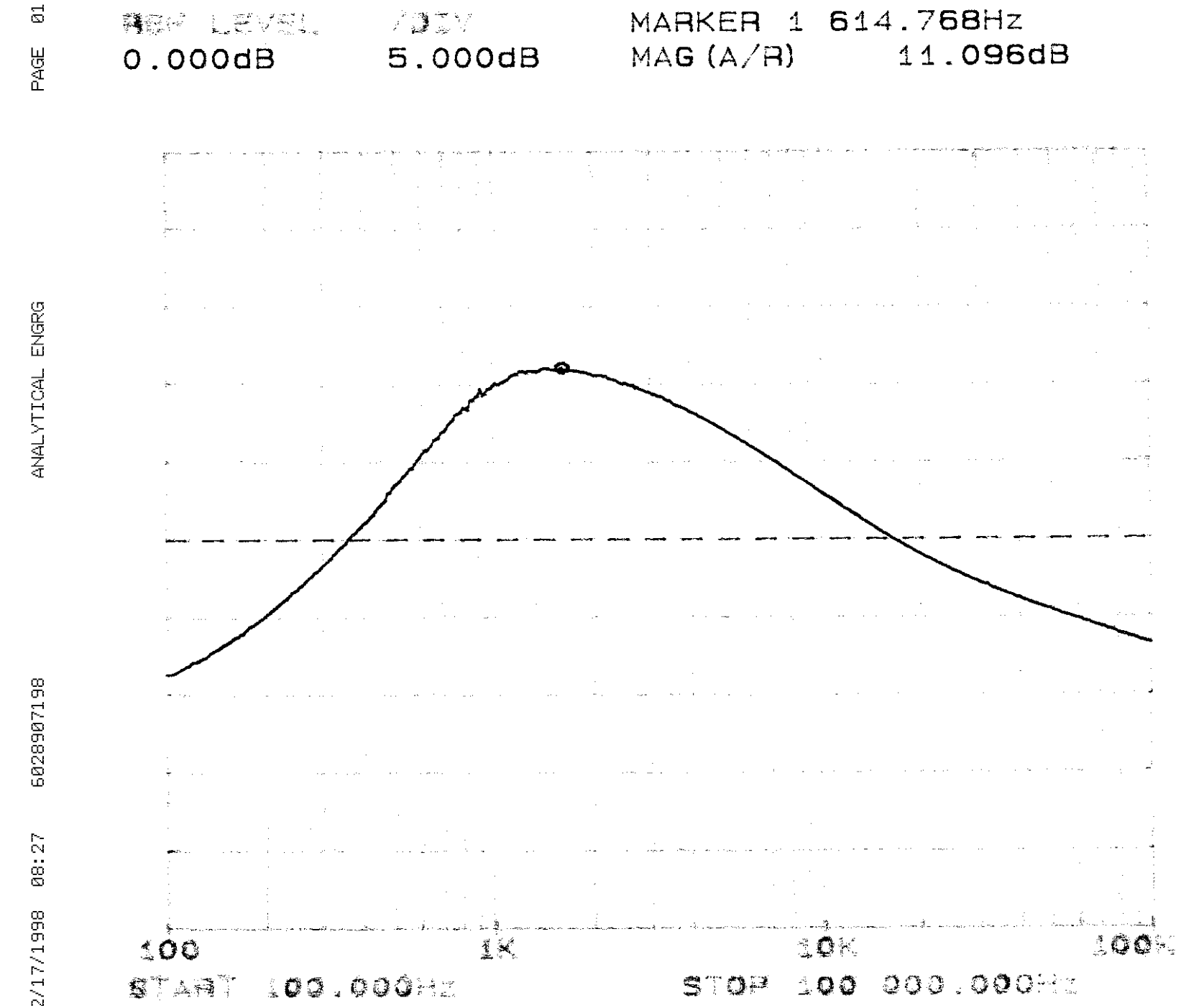
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10K
100K
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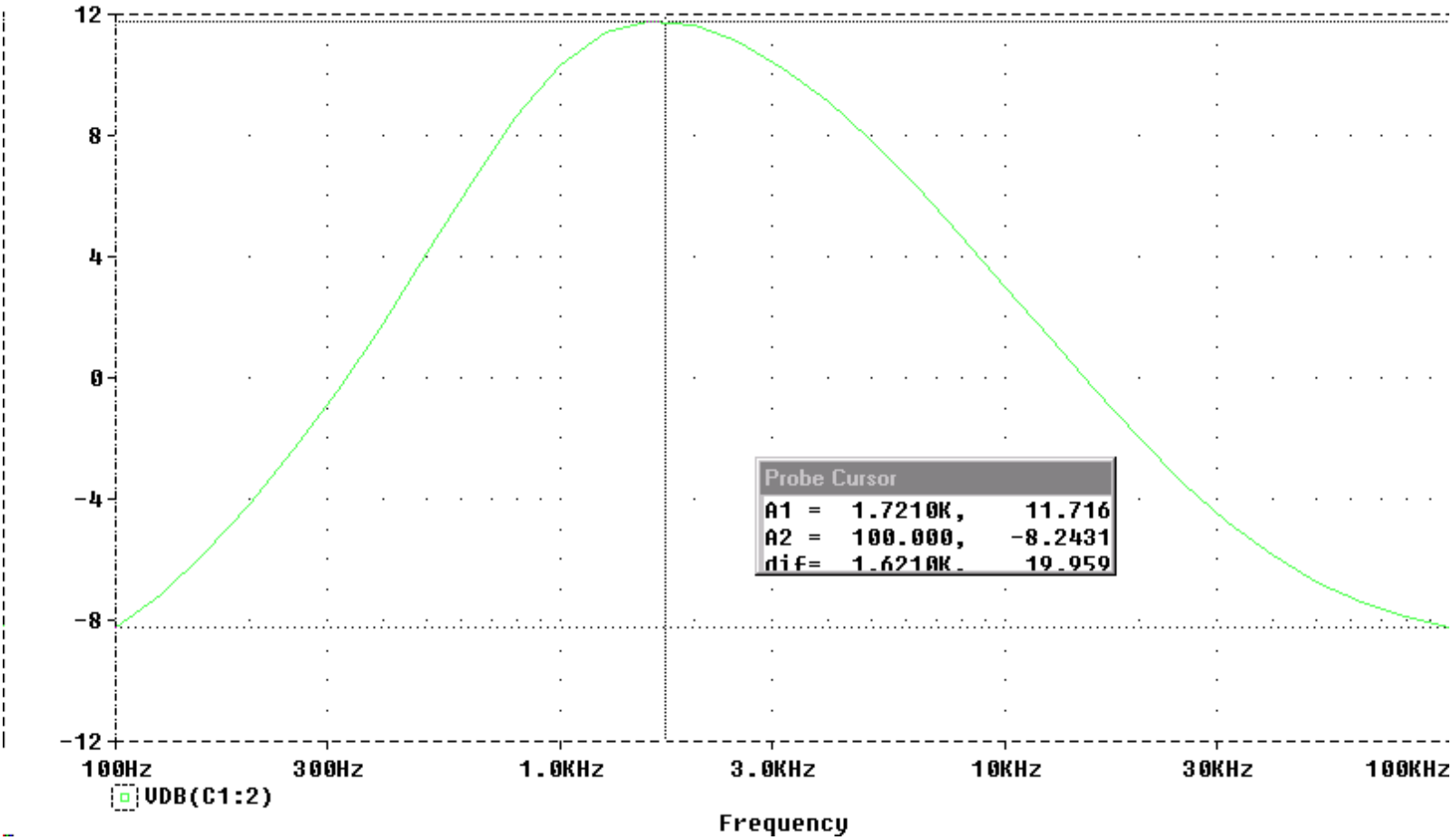
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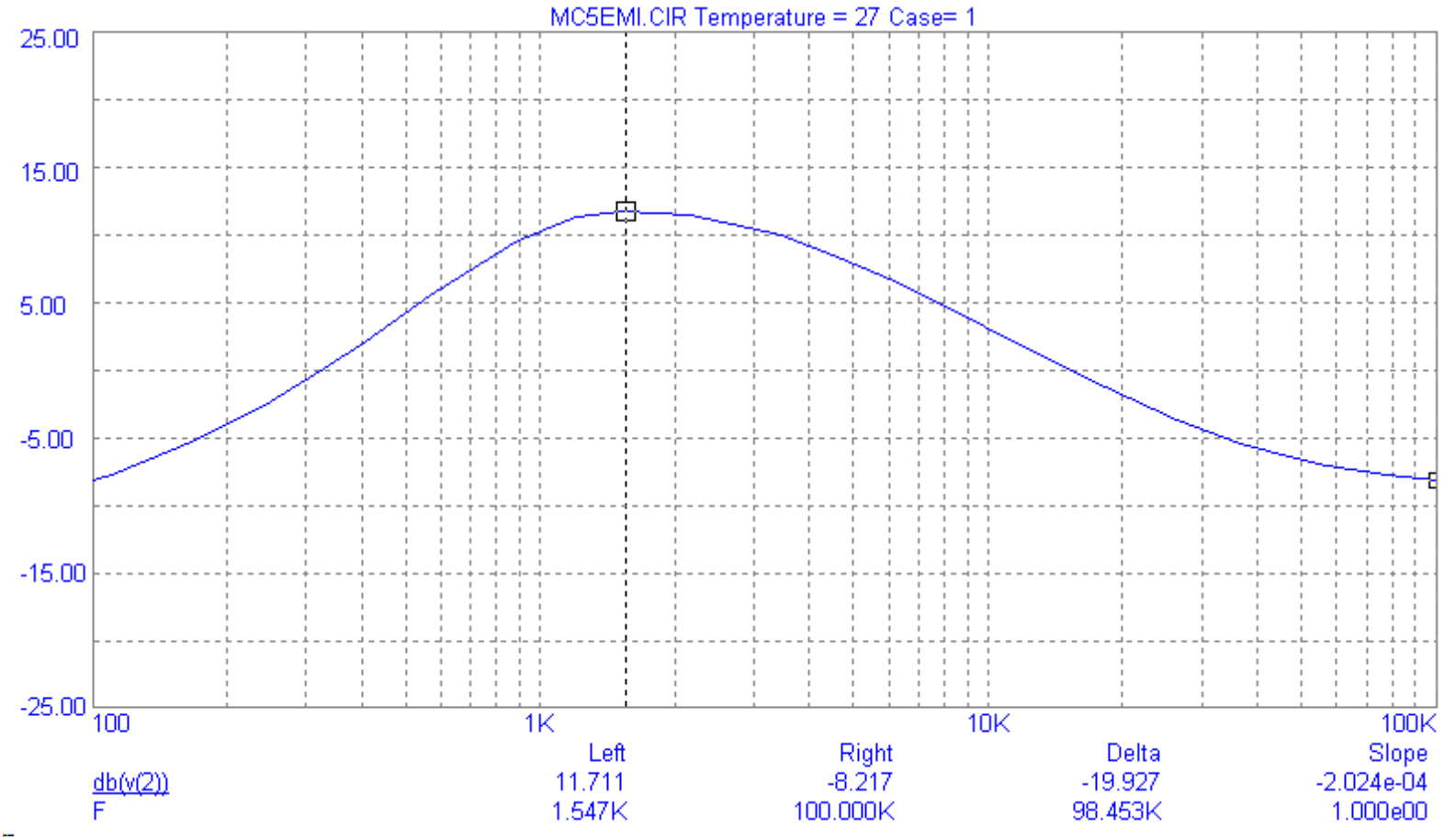
Frequency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-5.00
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100K
Left
Right
Delta
Slope
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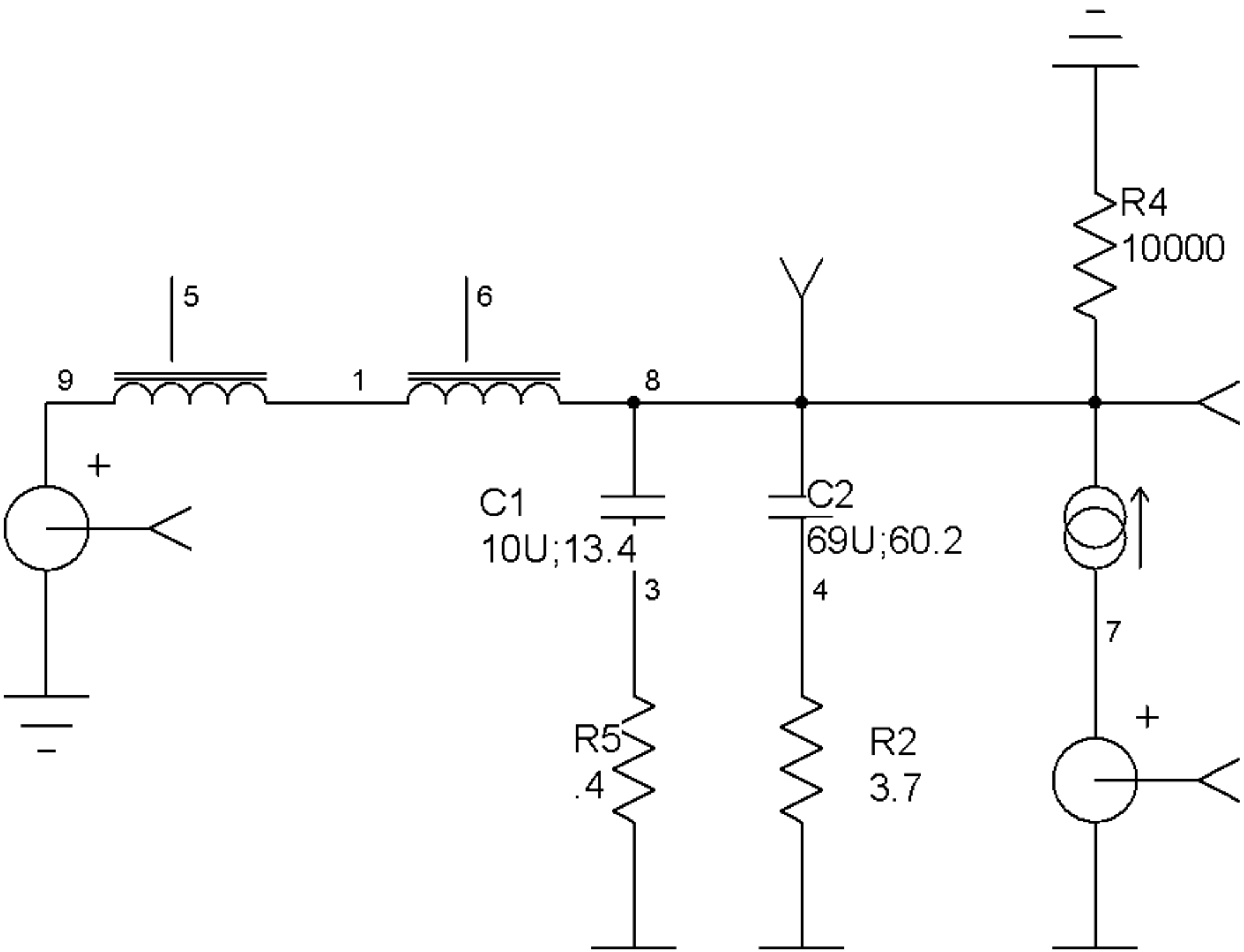
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8
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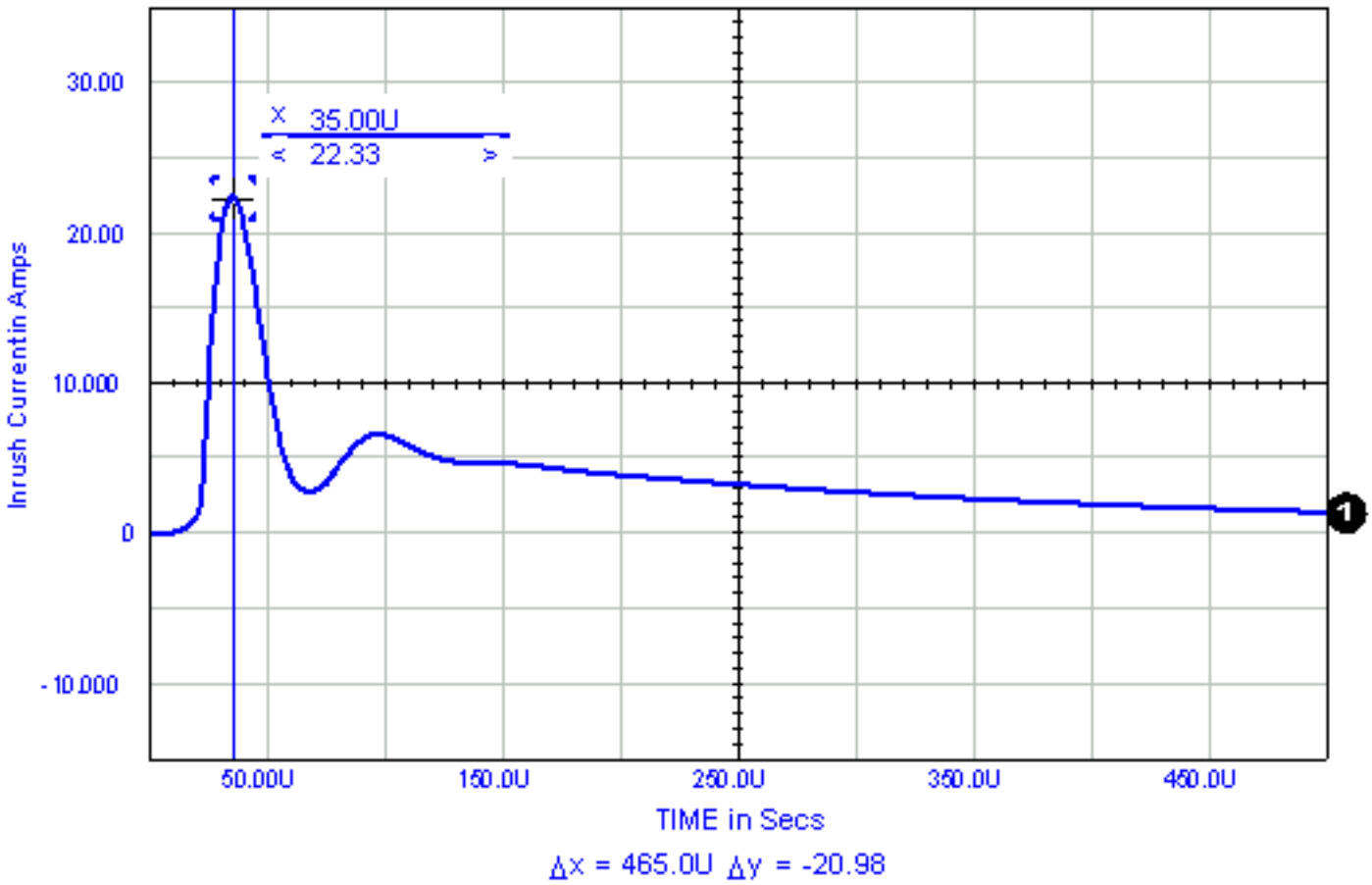
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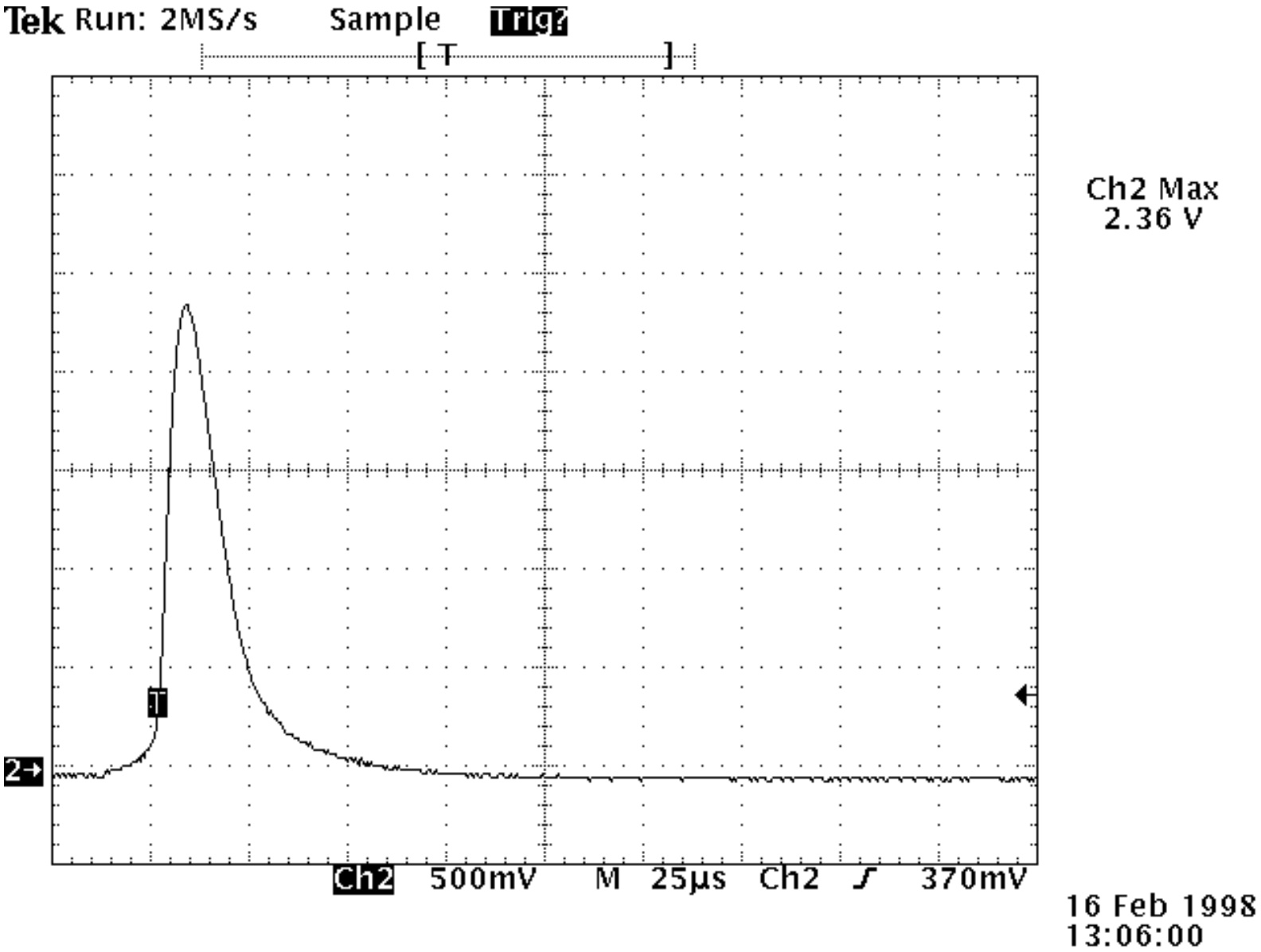
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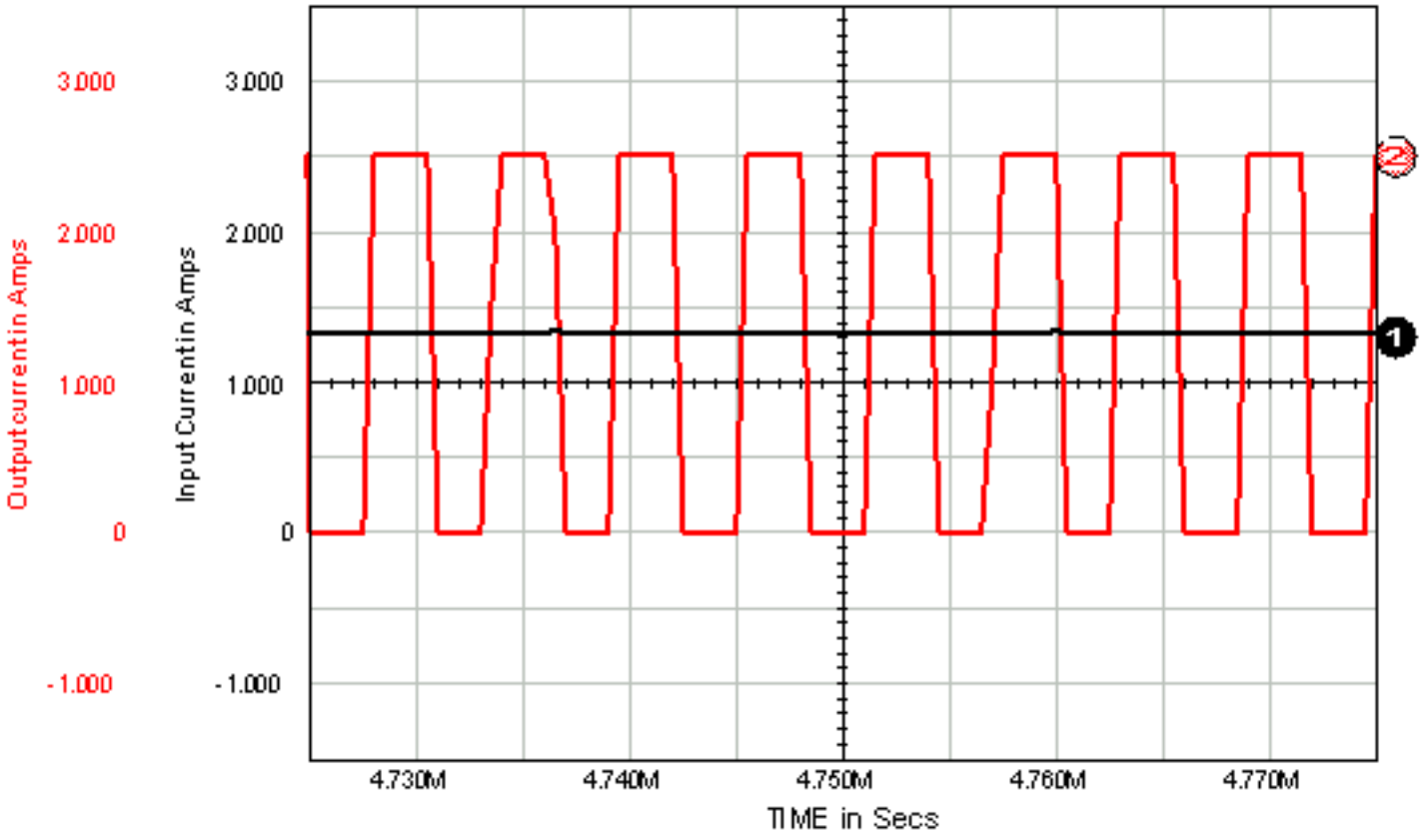
16 Feb 1998
13:06:00


3.000
2.000
1.000
0
-1.000
Output current in Amps
3.000
2.000
1.000
0
-1.000
Input Current in Amps
4.730M
4.740M
4.750M
4.760M
4.770M
TIME in Secs
2
1

Comparison of Results						
Parameter	Conditions	IsSpice (non-saturating)	IsSpice (Saturating)	Pspice	Microcap V	Hardware Data
Output impedance		11.74 dB	11.65 dB	11.71 dB	11.7 dB	11.1 dB
Maximum inrush Current	Turn on	6.17 amps	22.33 amps	6.11 amps	6.16 amps	23.6 amps
Attenuation	Freq=170 kHz Iout=2.5 A_max Duty=50%	56.7 dB	46.7 dB	58.2 dB	58.4 dB	59.3 dB

4
Power Conversion Circuits

Power converter circuits are often the most overlooked aspect of a system. During the engineering phase, power is not a concern. There are plenty of bench power supplies scattered around the laboratory for use in breadboards. Even in SPICE, the trusty voltage source element provides infinite voltage and infinite current for new circuit designs.

Unfortunately, when the time comes to put the system together, it is remembered that without circuits to condition the power to the system, the system is of little use to anyone. Operational amplifiers frequently need positive and negative DC voltages to operate correctly; amplifiers need both AC and DC voltages, sometimes at high currents, in order to perform their functions. Window comparators and precision sensors need highly accurate AC and DC voltages for the circuit to succeed in it's mission. What will power the system when the bench supplies are gone?

Luckily, there are circuits that fill all of the power requirements listed above and more. Also, SPICE can be a valuable tool in aiding the engineer in designing, troubleshooting, and characterizing power conversion circuits.

A simple definition of a power conversion circuit is a circuit that converts power source of a certain characteristic (110 VAC, Battery voltage, Spacecraft bus) into power sources with a more desirable characteristic for an individual circuit (regulated + 5 VDC for digital logic, constant current sources). A wide variety of these circuits are presented in this chapter.

#11: LM117 Three Terminal Linear Regulator

Three terminal linear regulator devices have been popular for some time. The combination of simplicity, small package, good regulation, versatility, and reasonable price is attractive to engineers looking to optimize designs. When examining the operation of a three terminal regulator, simulation may not make much sense. An input voltage begets a regulated output voltage. Why simulate this? The answer may be explained below.

The following circuit (Figure 11-1) is a typical application configuration for an LM117 circuit. The input voltage is 22 volts DC. Resistors R1 and R2 set the regulated output voltage at 16.7 volts.

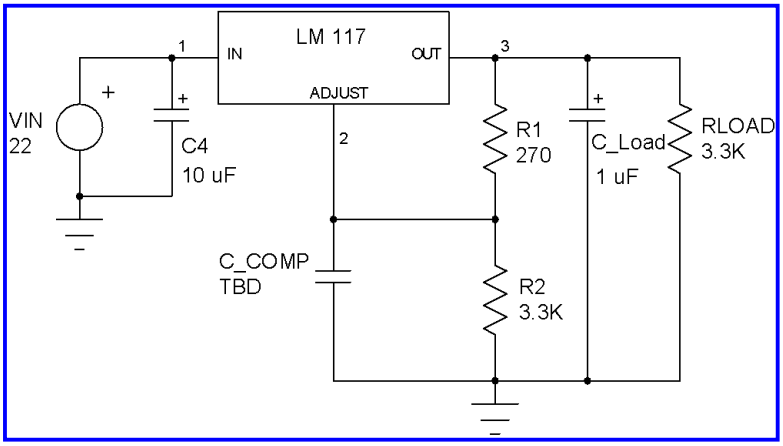


Figure 11-1: Typical application for an LM117 Three terminal linear regulator

One interesting measurement that can be made on this component would be the stability. In order to measure the stability in the lab, a special test configuration was used. This test set up is shown in Figure 11-2. The injection signal must be kept very small (700 uV is suggested) and the measurement probes should be placed at R and A on the diagram in Figure 11-2 as shown, with the ground referenced to the output (make sure the power supply in not tied to earth ground).

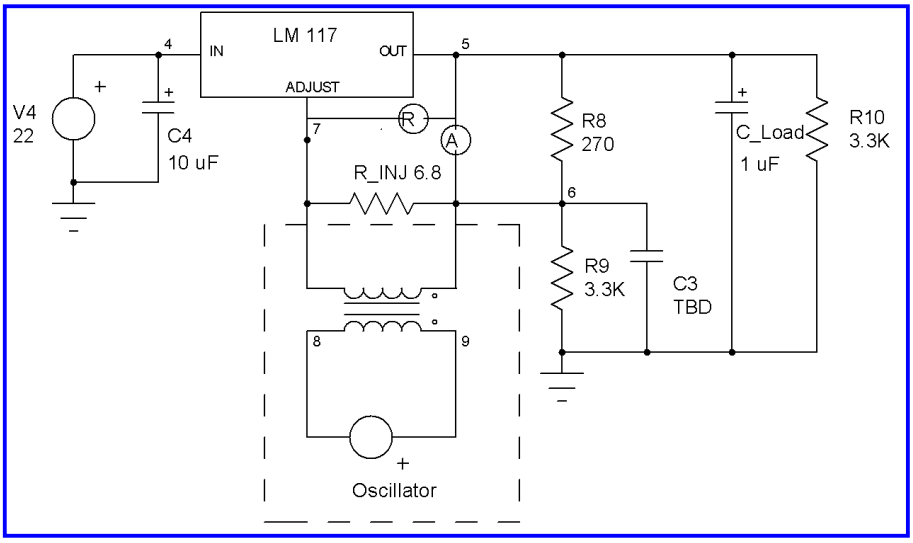


Figure 11-2: Stability measurement setup for three terminal regulator

Using the test set up in Figure 11-2, several configurations were measured on the breadboard. The cases will be measured one at a time, with comparisons to the SPICE results at each case. The first case is the recommended operational use by the Linear Technology ® databook [page 4-137, Linear Technology]. Linear recommends a 1 uF tantalum input bypass capacitor, a 1 uF capacitor at the output, and a 10 uF capacitor at the adjustment pin. The recommended type of capacitor is a solid tantalum. The SPICE configuration for testing stability is shown in Figure 11-3.

Click Here to see the larger Image

Figure 11-3: SPICE Stability measurement setup for three terminal regulator

The resulting breadboard measurement is shown in Figure 11-4. The IsSpice result at the same test configuration is shown in Figure 11-5.

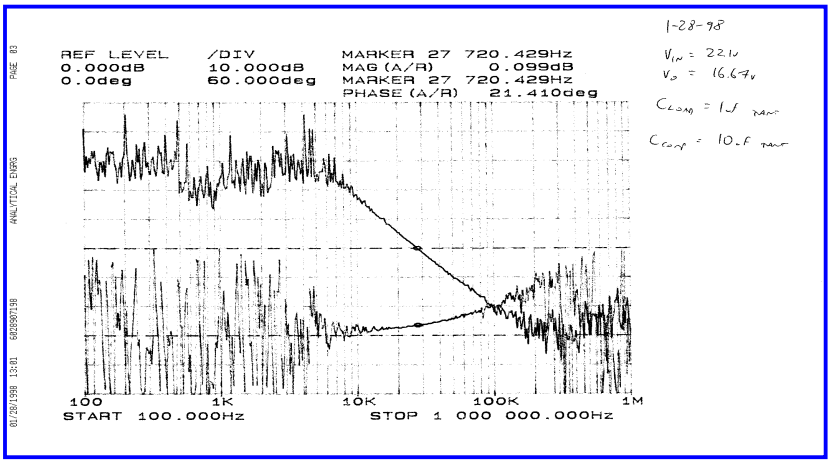


Figure 11-4: Breadboard bode plot (C_Comp=10uF)

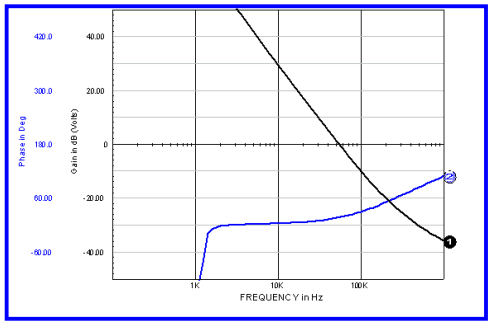


Figure 11-5: IsSpice bode plot (C_Comp=10uF)

Comparing the results of Figure 11-4 and 11-5, the phase margin is 21.4 degrees in the breadboard plot, compared to 15.85 degrees in the IsSpice plot. The crossover in the breadboard plot was 27.7 Khz, compared to 53.7 Khz in the IsSpice plot. The general shapes of the curves are also very similar.

- SPICE tip: Interestingly, there are three models of the LM117 in the Intusoft model library. One model gave the correct DC output voltage and the correct bode response. One model gave an incorrect DC output voltage but the correct bode response, and one model didn't converge. Surprisingly, all three models are transistor level. This is just another example of the necessity of testing previously unused models against their datasheet performance in order to ensure model accuracy. Incidentally, the model used in these simulations is the **LM317TI** model.

The LM117 configuration was also tested without a C_COMP capacitor. The breadboard results are shown in Figure 11-6. The IsSpice results are shown in Figure 11-7.

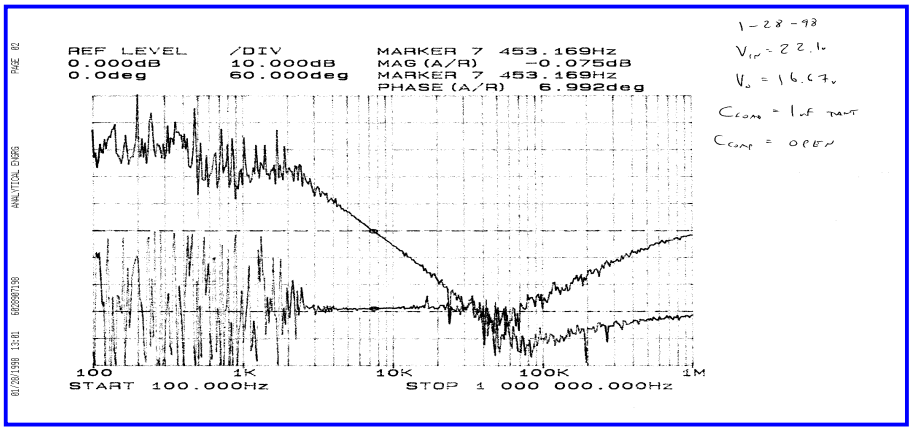


Figure 11-6: breadboard bode plot (C_Comp=open)

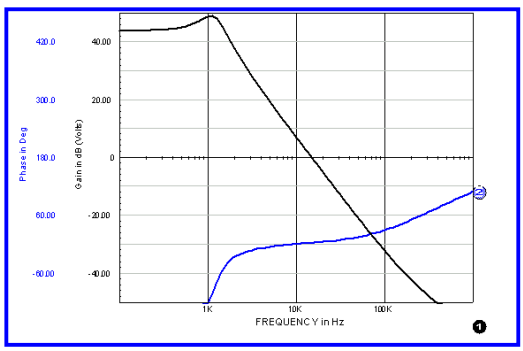


Figure 11-7: IsSpice bode plot (C_Comp=open)

The bread board phase margin and crossover frequency is 7 degrees and 7.4

Khz. The SPICE simulation phase margin and crossover frequency is 1.7 degrees and 14.7 Khz. Good engineering practice suggests a minimum phase margin of 45 degrees. The final configuration approaches this value. The C_COMP capacitor is changed to 4700 pF. The breadboard measurements are shown in Figure 11-8 while the IsSpice results are shown in Figure 11-9.

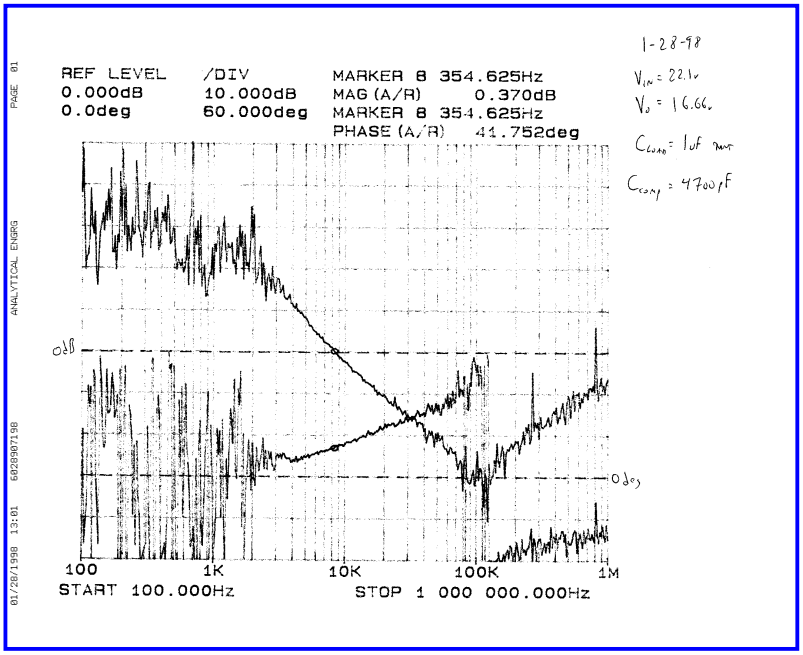


Figure 11-8: Breadboard bode plot (C_Comp=4700 pF)

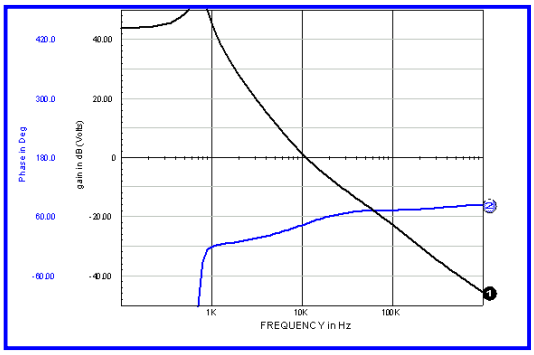


Figure 11-9: IsSpice bode plot (C_Comp=4700 pF)

The breadboard phase margin and crossover frequency is 41.7 degrees and 8.3 Khz. The IsSpice simulation results show a phase margin of 44.6 degrees and a 11 Khz crossover. Examining the results of the testing and simulation, we can conclude there is an optimal value of the C_COMP capacitor value in order to maximize phase margin and create an optimally stable three terminal regulator. An excellent tool for determining this optimal capacitance is SPICE.

- SPICE tip: The optimizer function of the SPICE simulators is tailor made for this problem. The optimization feature can be performed in Microcap by using the **STEPPING** feature in the AC menu and Pspice by using the **PARAMETRIC** sweep in the setup dialogue box. In IsSpice, the **OPTIMIZER** sweep menu is selected by selecting the SIMULATION CONTROL item in the ACTIONS menu of ICAP.

The resulting graph from the optimizer sweep is shown in Figure 11-10. Notice the optimal capacitance value is approximately a 6.8 nF capacitor which produces a phase margin of 66.5 degrees.

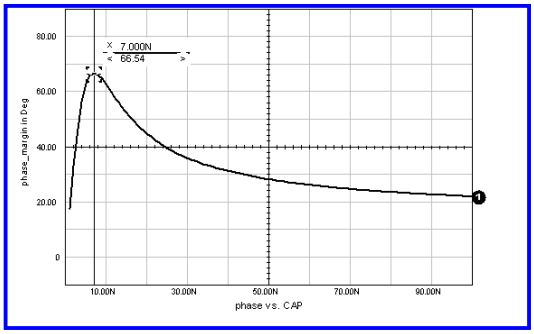


Figure 11-10: Optimizer sweep to determine optimal C_COMP capacitance

Simulations of this circuit were also performed in Microcap. The configuration shown in Figure 11-3 was simulated with a C_COMP value of 4700pF. The resulting Microcap Bode plot is shown in Figure 11-11. Simulation of the LM317 circuit in Pspice was attempted, however, the netlist contains too many transistor elements for the evaluation version.

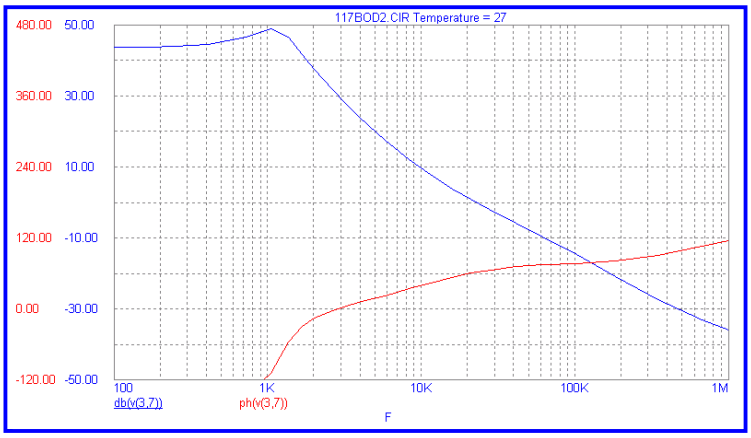


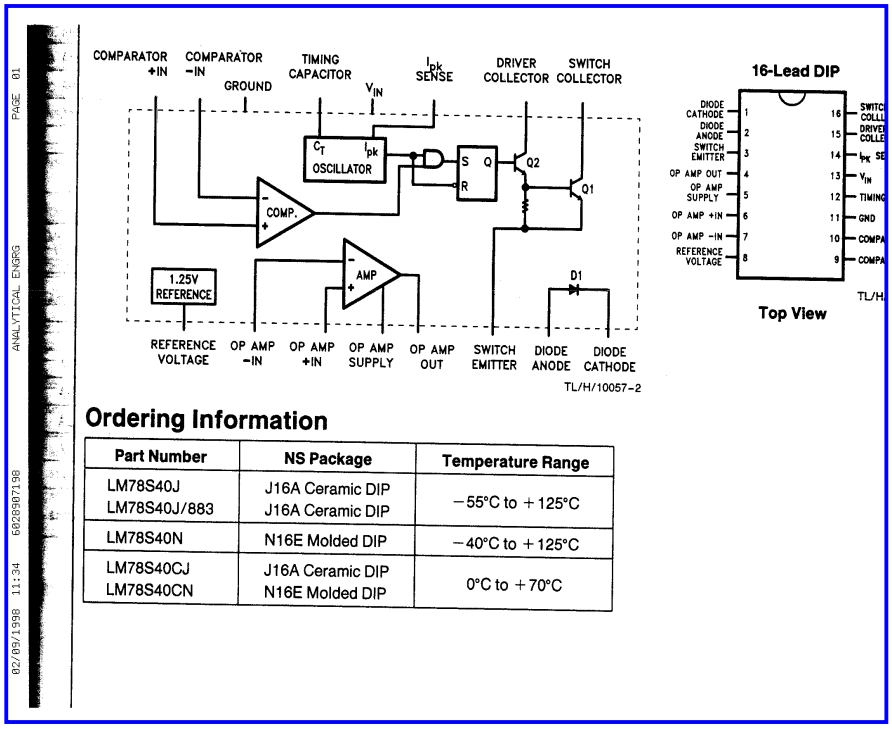
Figure 11-11: Microcap results with C_COMP=4700 pF

Run Time Summary		
IsSpice v 7.6	PsPice v 6.3	Micro-Cap V v2
1.033 Sec	xxx Sec	0.704 Sec
Advantages: low parts count, inexpensive, good accuracy, good ripple rejection		
Disadvantages: excessive power dissipation at higher currents, not as efficient as other topologies (due to headroom requirements).		

Filenames: 117Bod, 117opt (IsSpice) 117bod2 (Microcap) 117bod3 (Pspice)

#12: LM78S40 Simple Switcher DC to DC converter

Many semiconductor manufacturers make an IC that encompasses all of the necessary logic and analog circuitry required to construct a switching regulator circuit. An example of this universal approach to design is the National ® LM78S40 IC. This IC contains an oscillator, temperature compensated precision voltage reference, Mosfet driver logic, current limiting, error amplifier, and even a built in rectifying diode. IC's like this one are excellent for DC to DC applications that require more power than a three terminal linear regulator can provide, but do not require isolation. The block diagram and connection diagram for this IC is shown in Figure 12-1. The schematic for our test circuit IC is shown in Figure 12-2. The test circuit takes a DC 20 volt input and provides a regulated 10 volt DC output.



Part Number	NS Package	Temperature Range
LM78S40J LM78S40J/883	J16A Ceramic DIP J16A Ceramic DIP	−55°C to +125°C
LM78S40N	N16E Molded DIP	−40°C to +125°C
LM78S40CJ LM78S40CN	J16A Ceramic DIP N16E Molded DIP	0°C to +70°C

Figure 12-1: Block and Connection Diagrams for LM78S40 IC (Reprinted with permission from National Semiconductor ®)

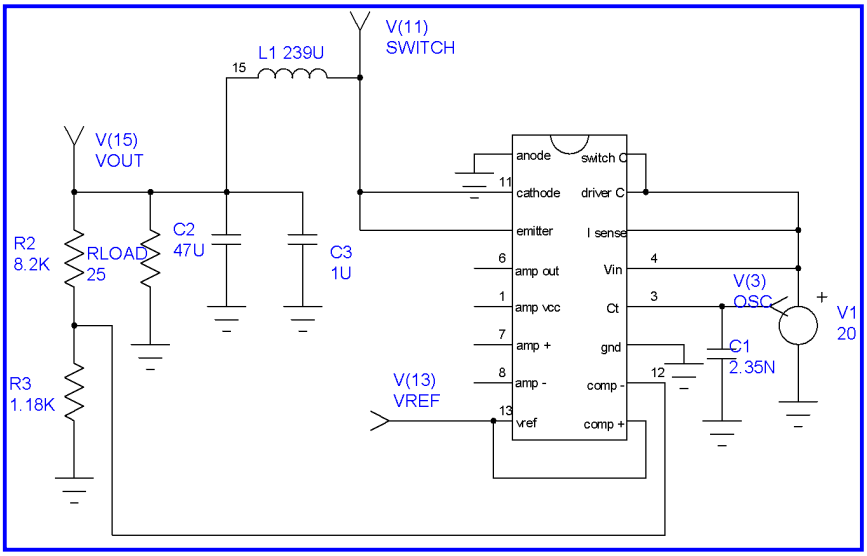


Figure 12-2: Test Schematic for 78S40 Simple switcher IC

The SPICE equivalent circuit schematic is shown in Figure 12-3. Notice the DCR (DC Resistance) of the inductor L1 has been added (R_DCR) to the circuit. Also added to the circuit is a voltage source added between the inductor and the output in order to measure current. The input voltage is pulsed from 0 volts to 20 volts in order to aid in convergence.

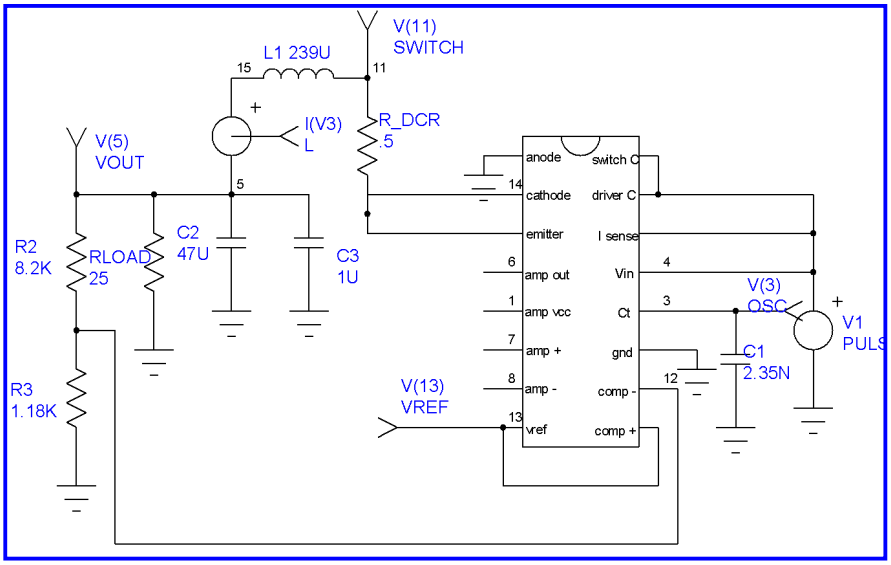


Figure 12-3: SPICE equivalent schematic for 78S40 Simple switcher IC

Also to aid in convergence, the following .OPTIONS statement is included:

.OPTIONS ABSTOL=1U ITL4=1000 ITL6=100 METHOD=GEAR

The transient simulation is run from 2.15 mSec to 2.35 mSec with a minimum time step of 50 nSec and a maximum time step of 100 nSec. The transient line also contains the UIC statement which will use the initial conditions specified in the schematic and not attempt to find a DC operating point.

The results of the breadboard waveforms and the IsSpice waveforms are compared side by side in Figures 12-4 and 12-5. Figure 12-4 shows the output ripple voltage on top, with the inductor voltage on the bottom. Figure 12-5 shows the oscillator frequency on top, with the inductor voltage on the bottom. The output voltage of the IsSpice model was 9.872, while the output voltage of

the Breadboard was 9.78 volts.

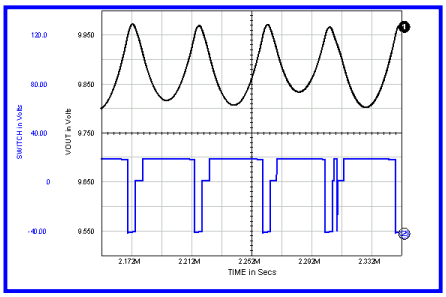


Figure 12-4A: IsSpice LM78S40 waveforms (top - output ripple, Bottom - inductor voltage)

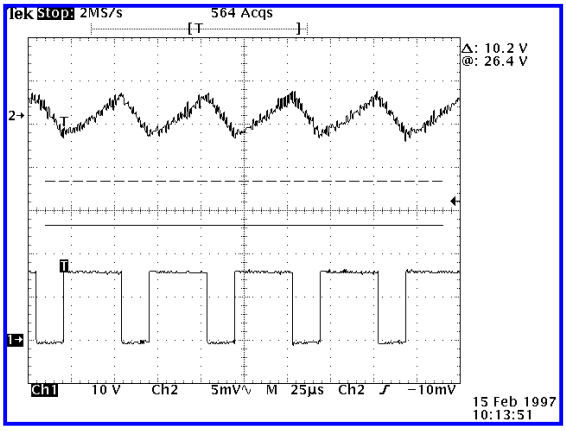


Figure 12-4B: Breadboard LM78S40 waveforms (top - output ripple, Bottom - inductor voltage)

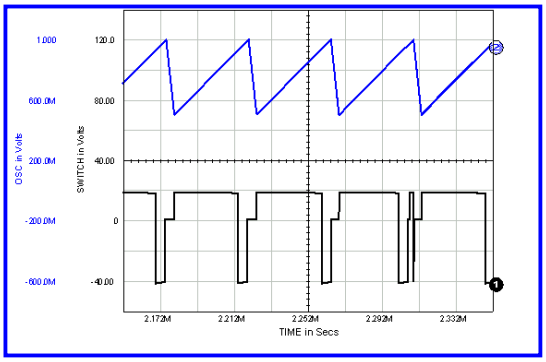


Figure 12-5A: IsSpice LM78S40 waveforms (top - Oscillator voltage, Bottom - inductor voltage)

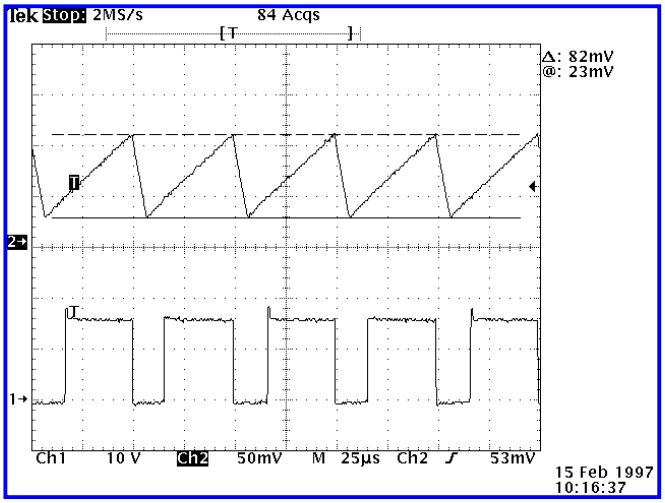
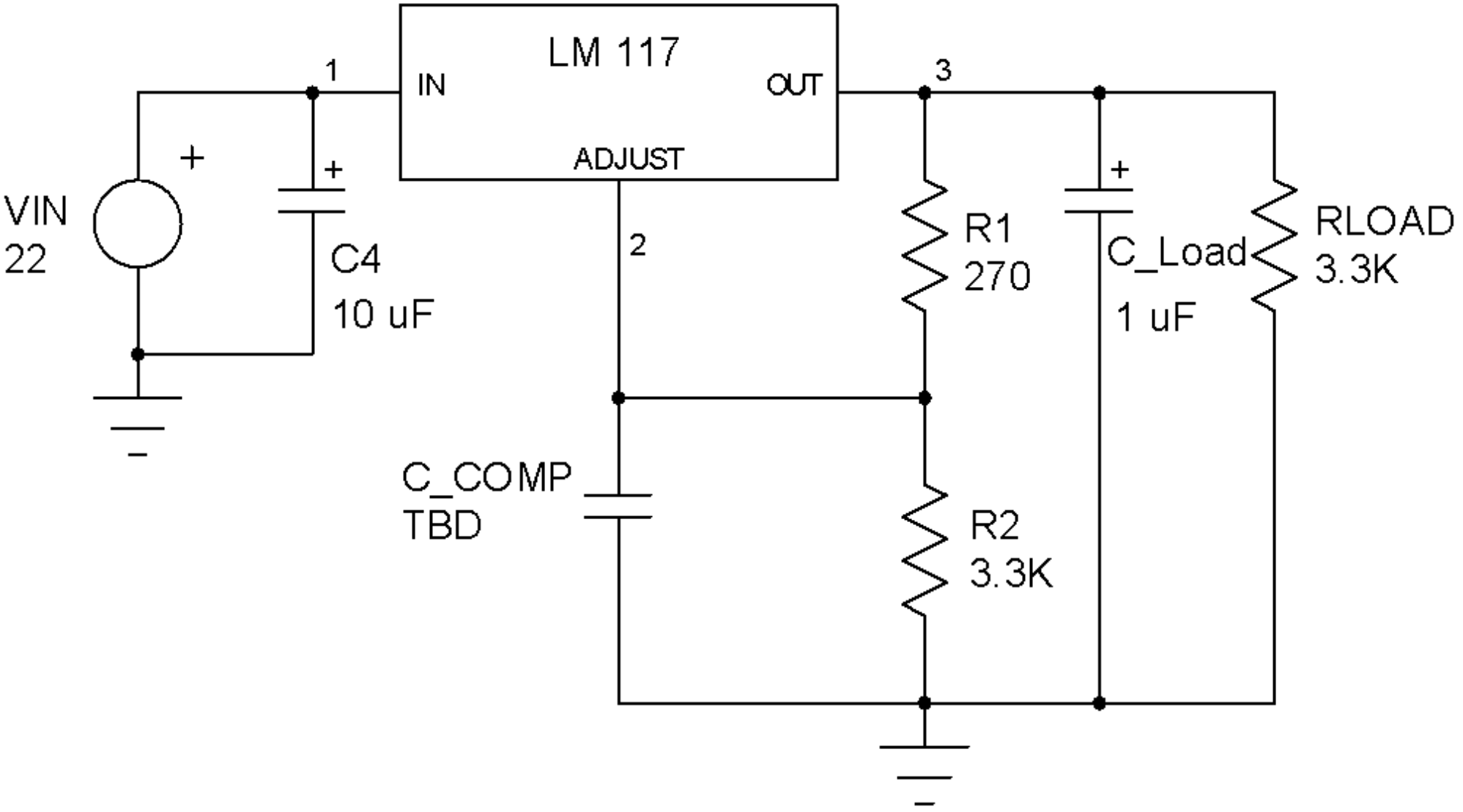


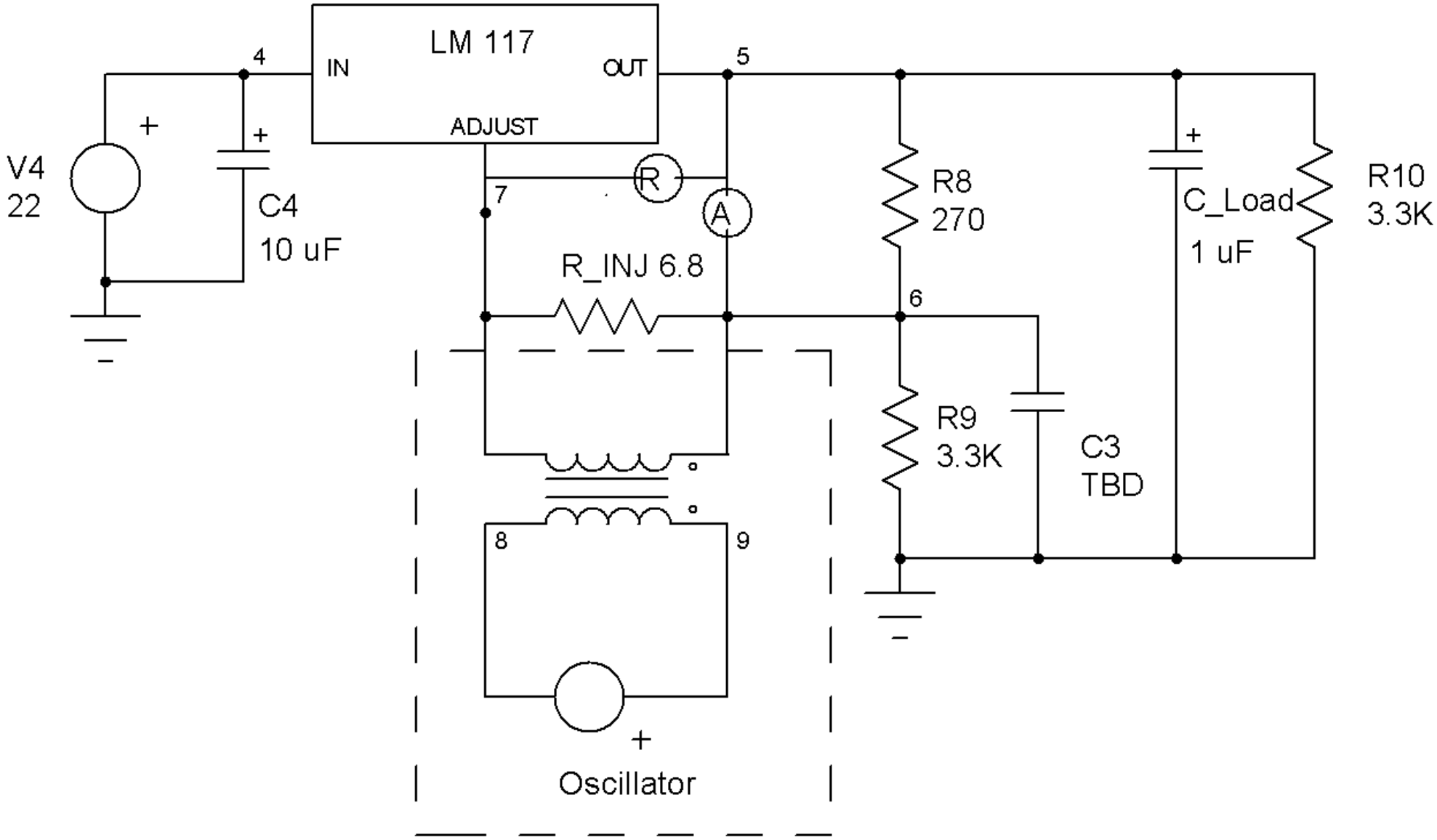
Figure 12-5B: Breadboard LM78S40 waveforms (top - Oscillator voltage, Bottom - inductor voltage)

- SPICE TIP: SPICE models for the LM78S40 were not provided in the Microcap or Pspice evaluation version software packages. This circuit was simulated using IsSpice only.

Run Time Summary		
IsSpice v 7.6	PsPice v 6.3	Micro-Cap V v2
207.3 Sec	xxx Sec	xxx Sec
Advantages: medium parts count, good output voltage line and load regulation, versatile, can provide step up or step down voltages		
Disadvantages: No isolation from input to output		

Filenames: 7840_1 (IsSpice)


LM 117
IN
OUT
ADJUST
1
2
3
VIN
22
+
C4
10 uF
R1
270
C_Load
1 uF
RLOAD
3.3K
C_COMP
TBD
R2
3.3K


LM 117
IN
OUT
ADJUST
4
5
7
6
8
9
V4
22
C4
10 uF
R
A
R_INJ 6.8
R8
270
R9
3.3K
C3
TBD
C_Load
1 uF
R10
3.3K
Oscillator

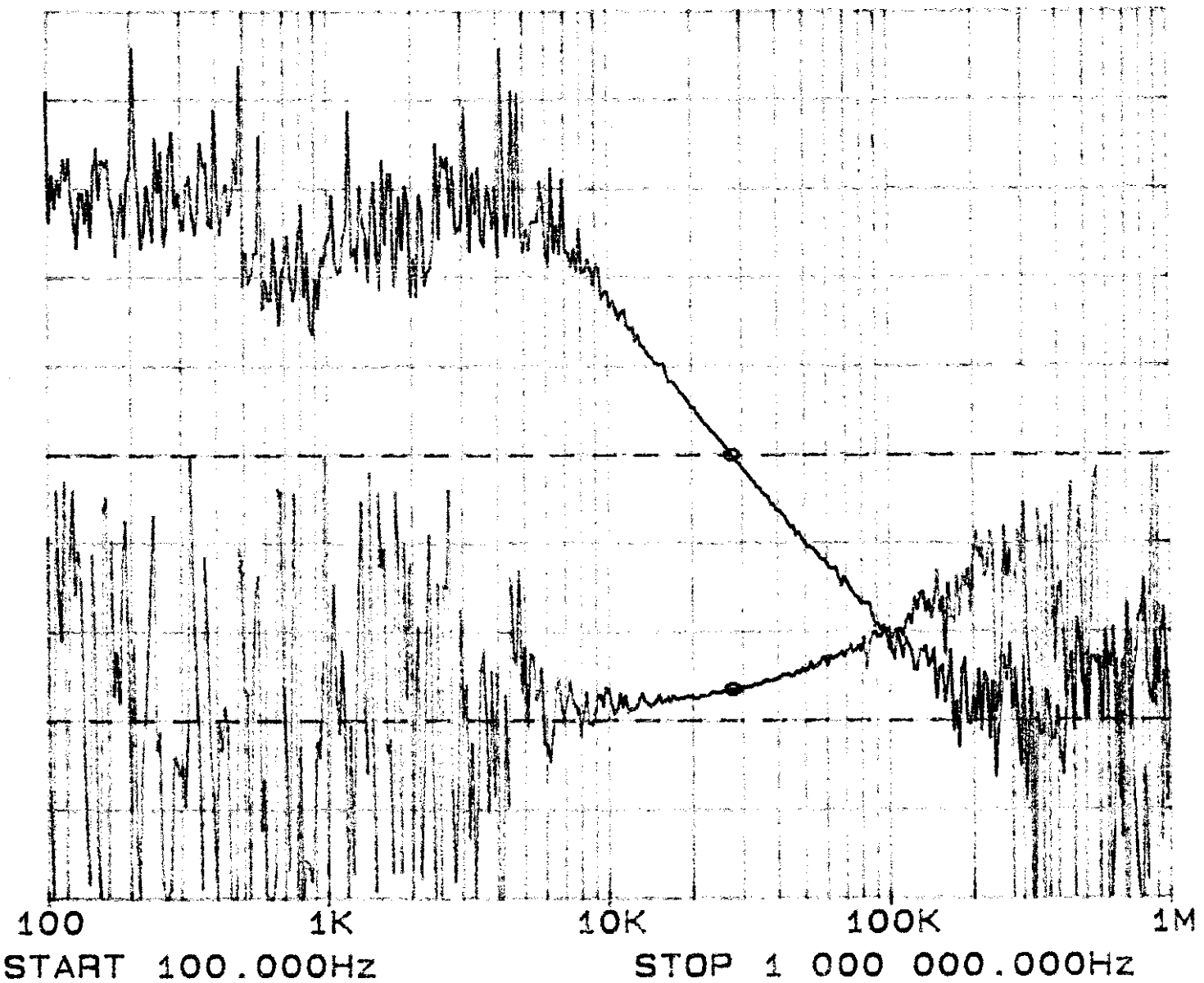
1-28-98

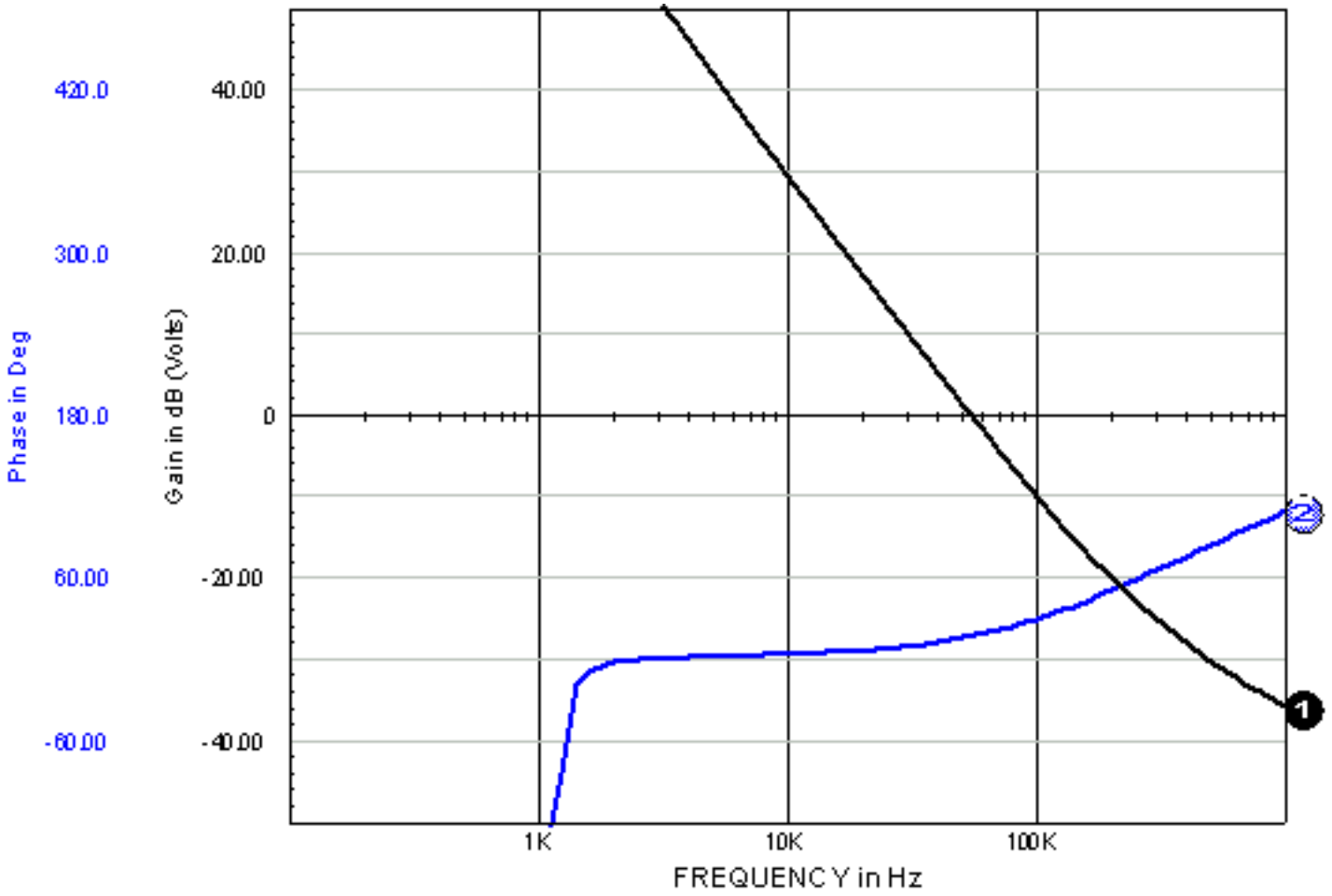
V_{IN} = 22.1V

V_o = 16.67V

C_{LOAD} = 1uF MAX

C_{COMP} = 10.0F MAX




420.0
300.0
180.0
60.00
-60.00
Phase in Deg
40.00
20.00
0
-20.00
-40.00
Gain in dB (Volts)
1K
10K
100K
FREQUENCY in Hz
1
2

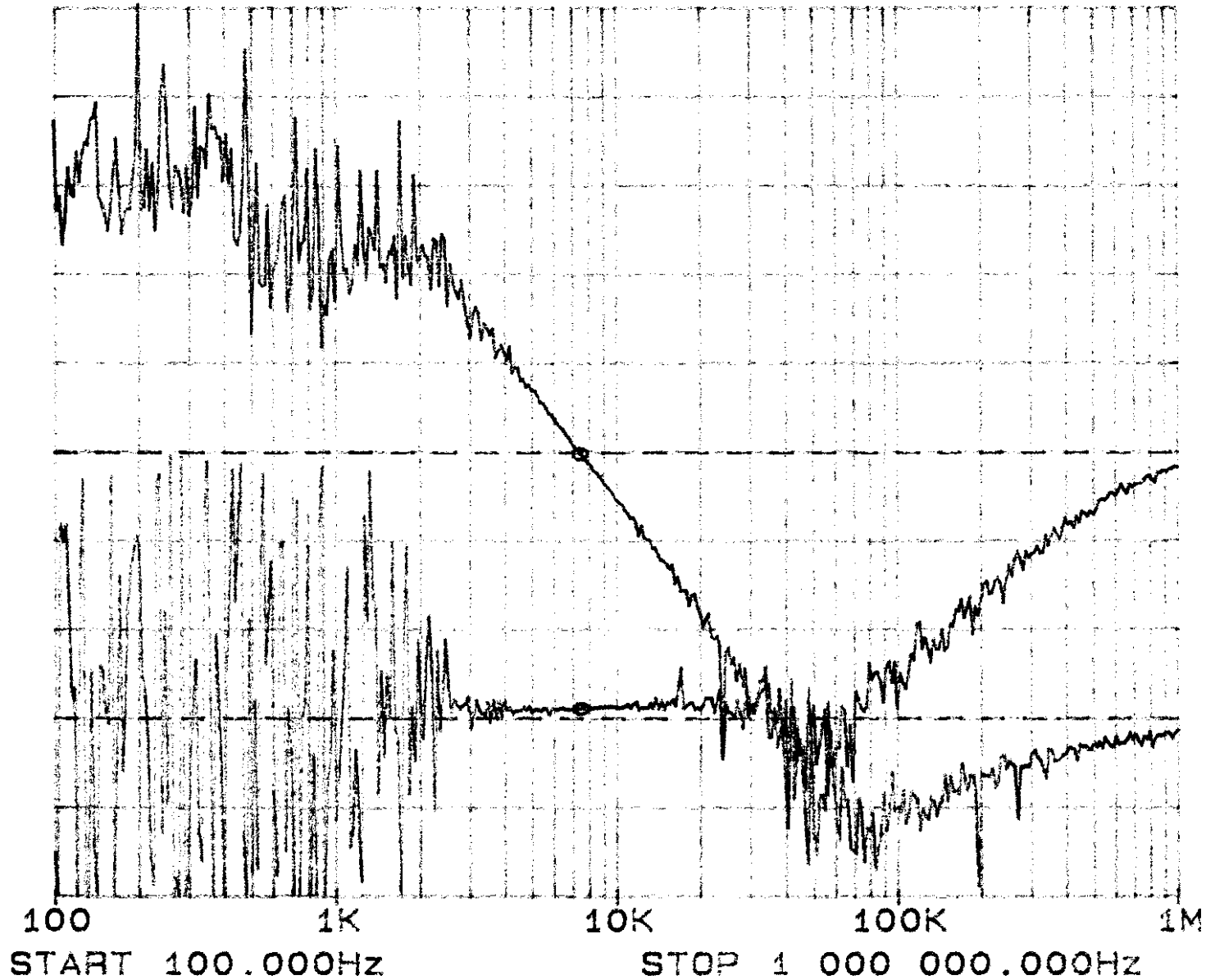
1-28-98

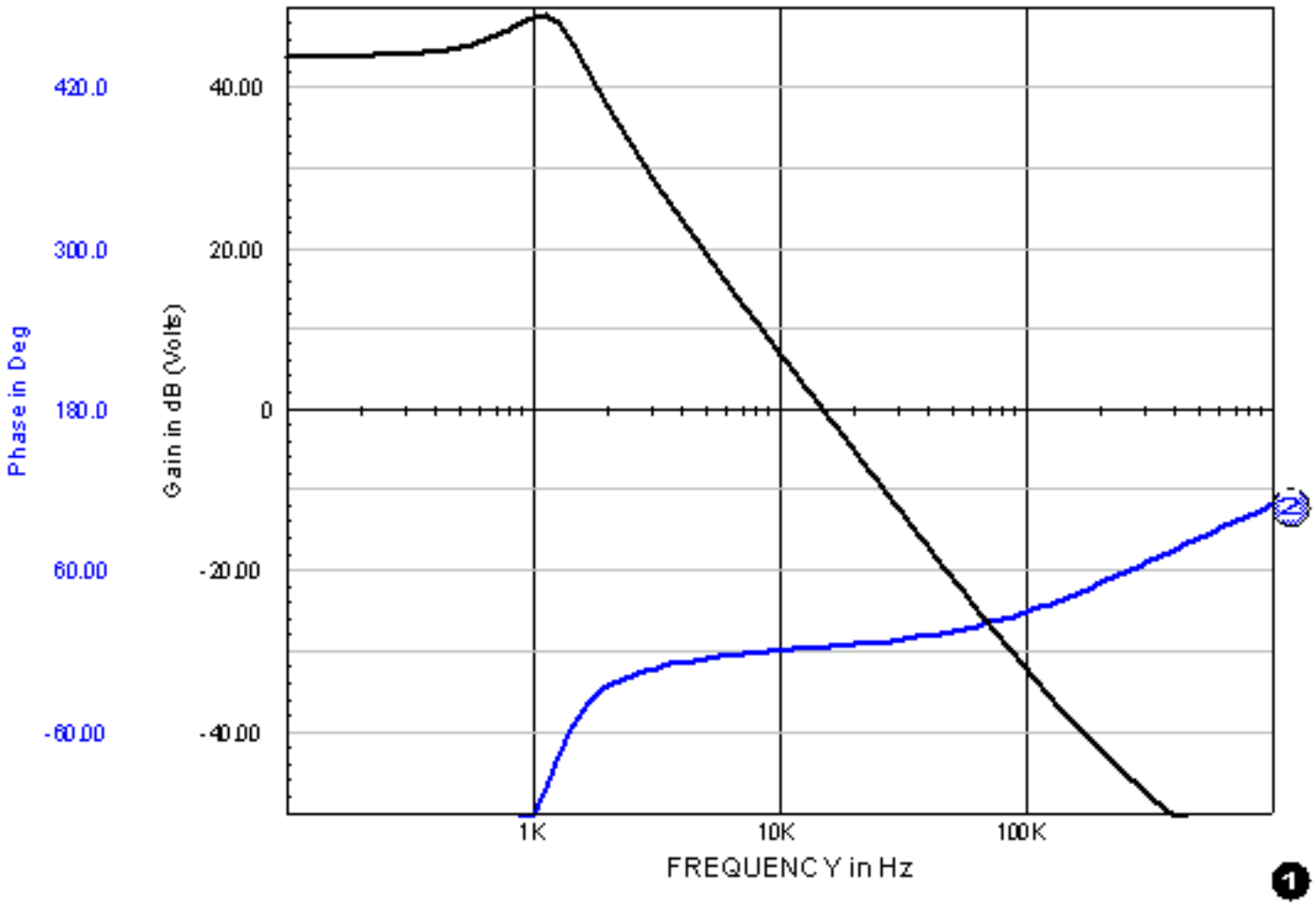
V_{IN} = 22.1v

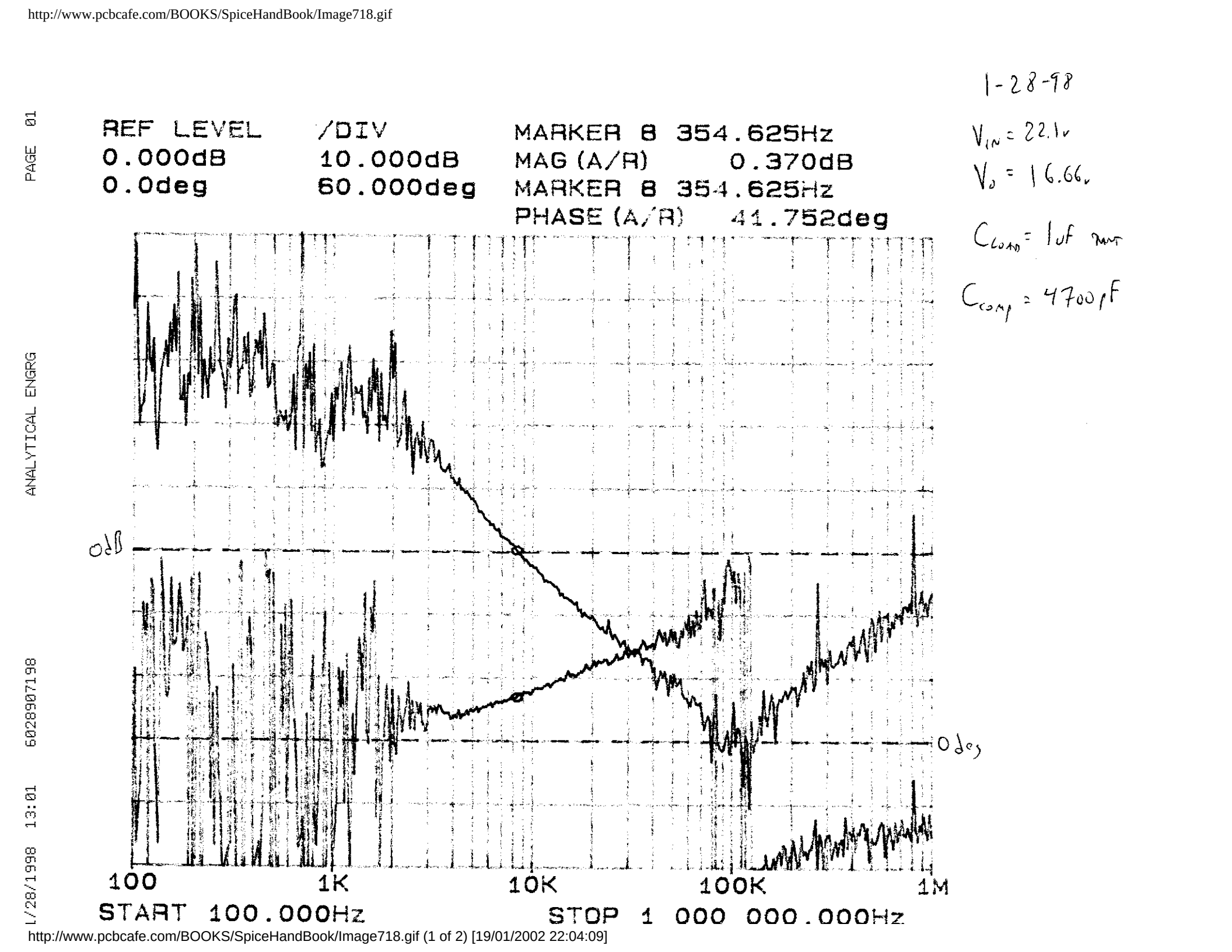
V_o = 16.67v

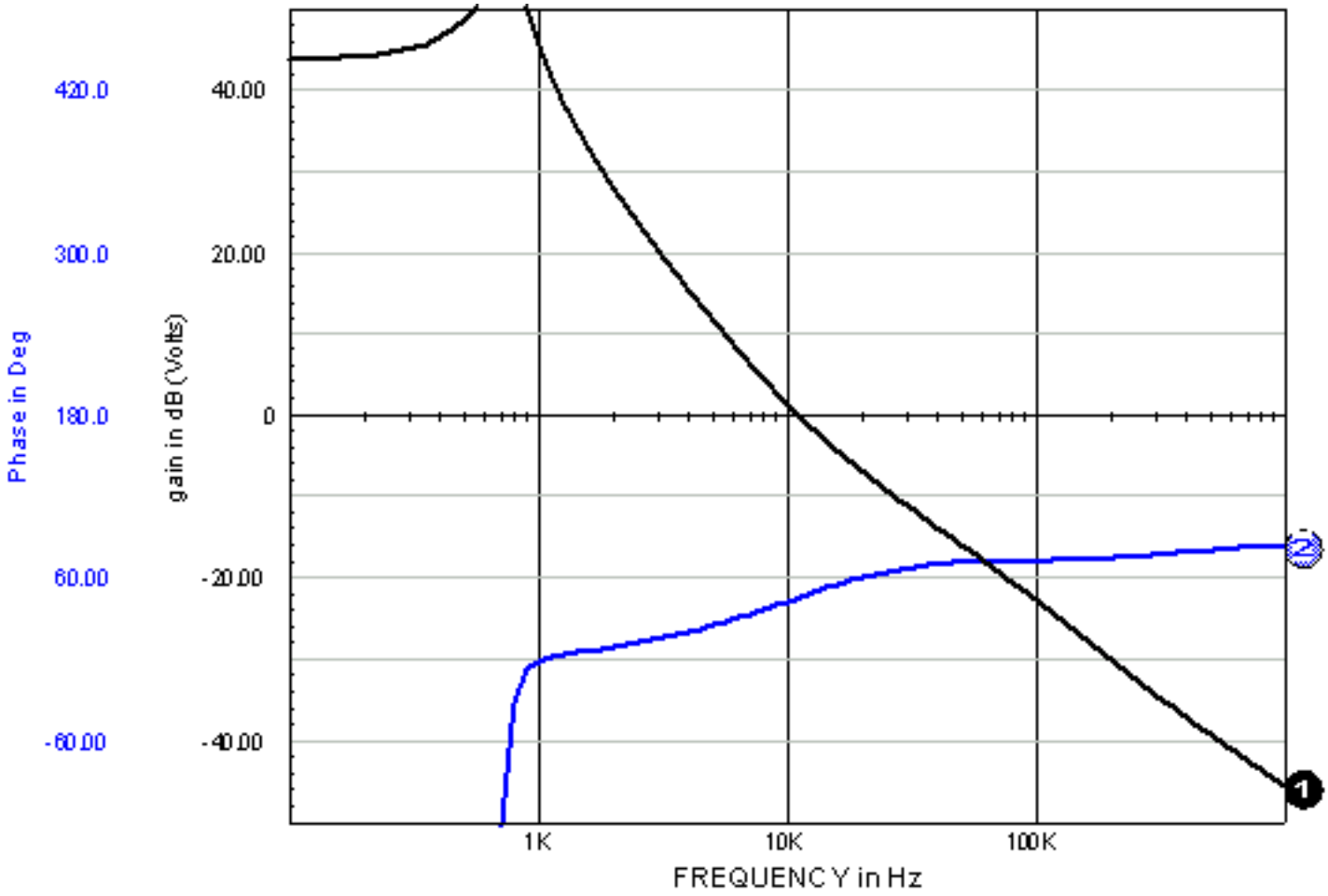
C_{LOAD} = 1uF TANT

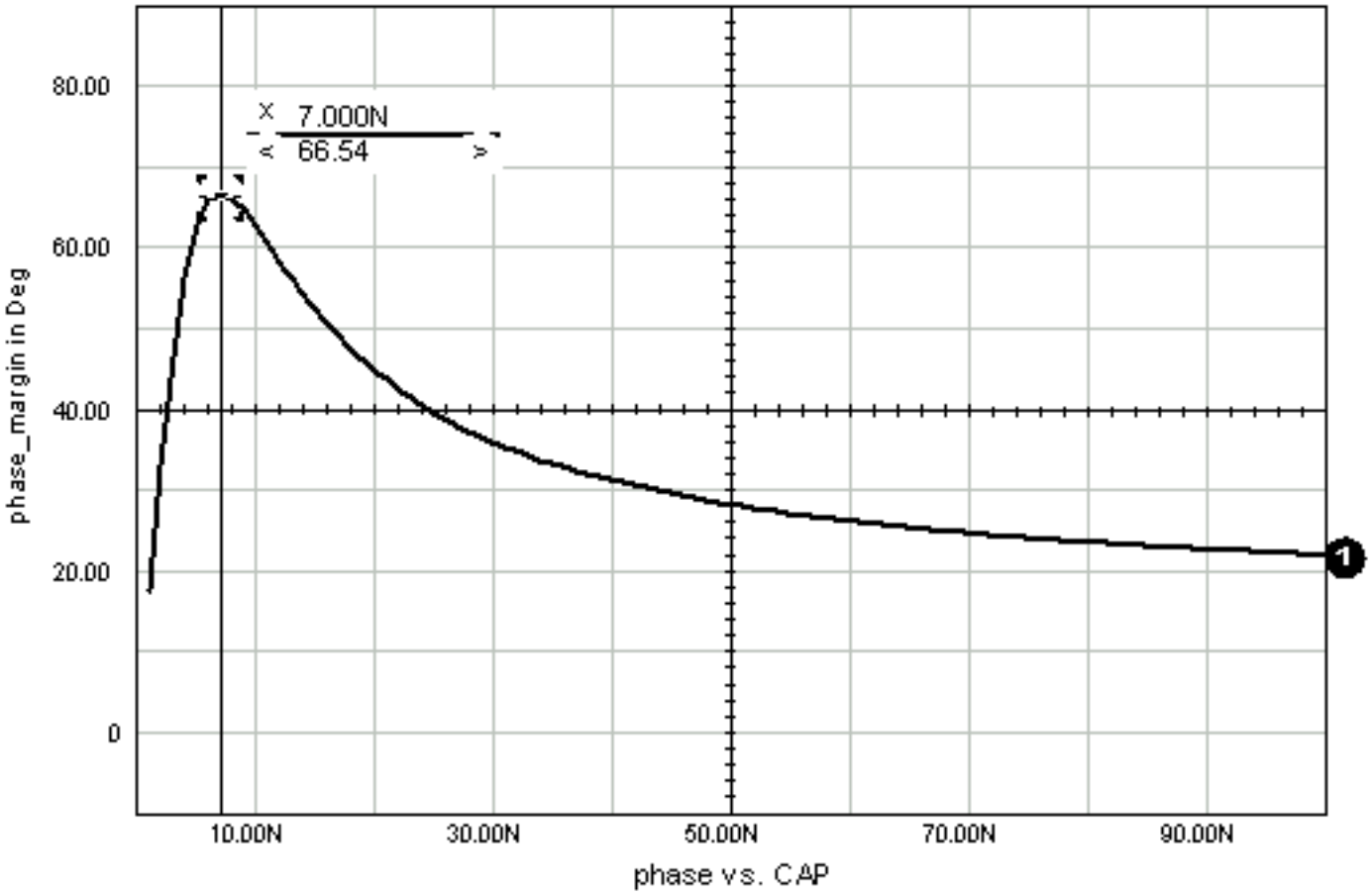
C_{COMP} = OPEN

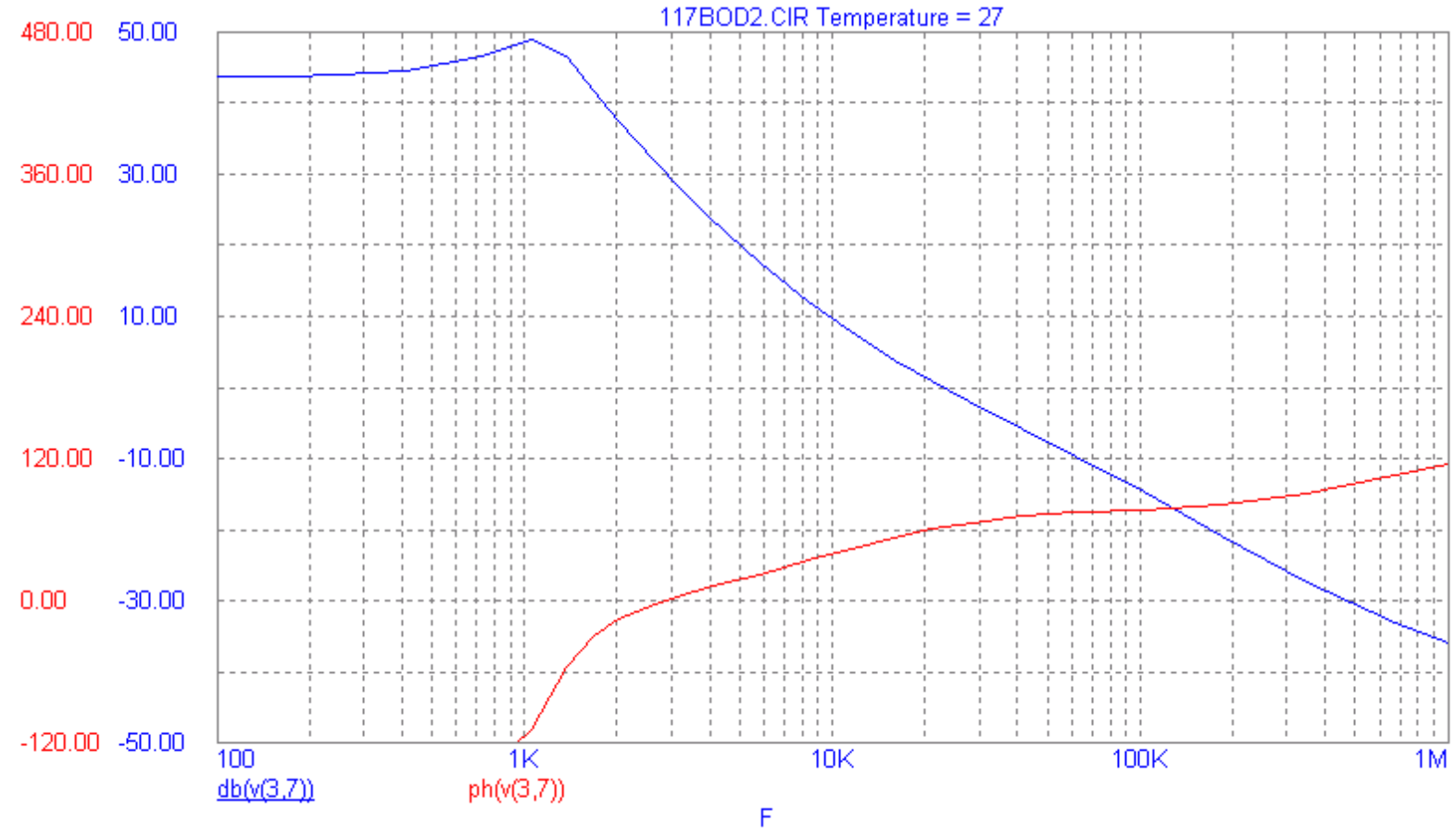



420.0
300.0
180.0
60.00
-60.00
Phase in Deg
40.00
20.00
0
-20.00
-40.00
Gain in dB (Volts)
1K
10K
100K
FREQUENCY in Hz
2
1


1-28-98
REF LEVEL
0.000dB
0.0deg
/DIV
10.000dB
60.000deg
MARKER 8 354.625Hz
MAG (A/R) 0.370dB
MARKER 8 354.625Hz
PHASE (A/R) -41.752deg
V_{IN} = 22.1v
V_o = 16.66v
C_{LOAD} = 1uF MKT
C_{COMP} = 4700pF
0dB
0deg
100
1K
10K
100K
1M
START 100.000Hz
STOP 1 000 000.000Hz
PAGE 01
ANALYTICAL ENGRG
1/28/1998 13:01 6028907198


420.0
300.0
180.0
60.00
-60.00
Phase in Deg
40.00
20.00
0
-20.00
-40.00
gain in dB (Volts)
1K
10K
100K
FREQUENCY in Hz
1
2


80.00
60.00
40.00
20.00
0
X 7.000N
< 66.54 >
phase_margin in Deg
10.00N
30.00N
50.00N
70.00N
90.00N
phase vs. CAP
1


117BOD2.CIR Temperature = 27
480.00
360.00
240.00
120.00
0.00
-120.00
50.00
30.00
10.00
-10.00
-30.00
-50.00
100
1K
10K
100K
1M
db(v(3,7))
ph(v(3,7))
F

#13: UA723 Hysteretic Buck Regulator

The UA723 can be configured to form a simple, low parts count Buck regulator. The UA723 is designed for use in positive or negative power supplies. This type of regulator is popular because it has excellent dynamic response. It can be configured as a series, switching, shunt, or floating regulator. The circuit has variable frequency, because it essentially an uncompensated oscillator. The output ripple is a function of the hysteresis. This comes at a cost, which is a decrease in the ability to maintain regulation. The schematic is shown in Figure 13-1. The breadboard data is shown in Figure 13-2 and Figure 13-3. The Ispice simulated data is shown in Figure 13-4 and Figure 13-5.

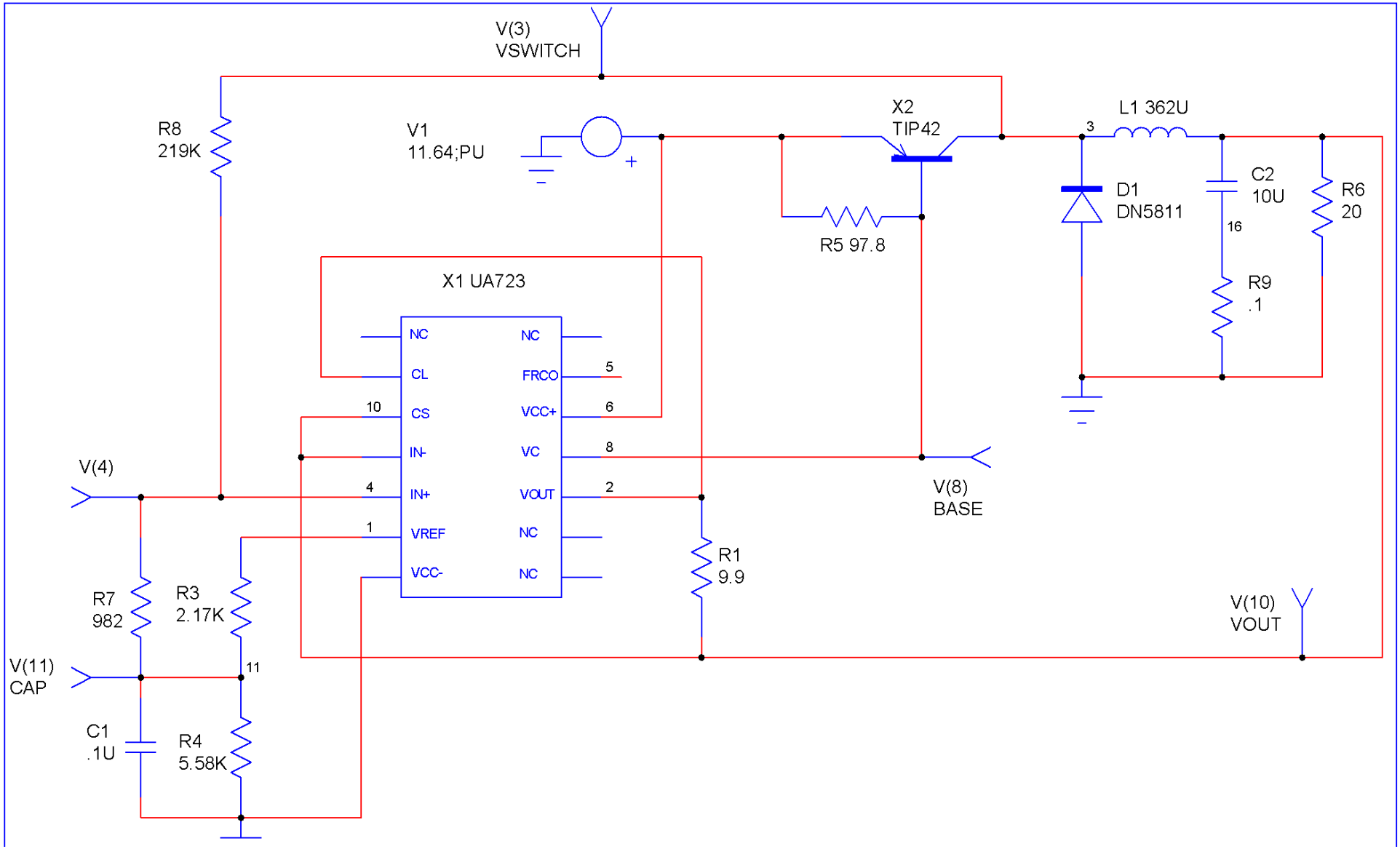


Figure 13-1: Schematic for UA723 Buck Regulator

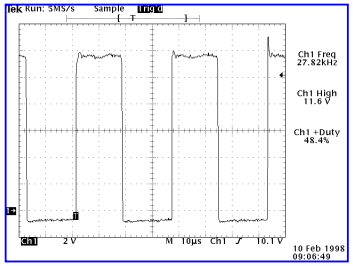


Figure 13-2: Breadboard Collector Voltage of UA723 Buck Regulator

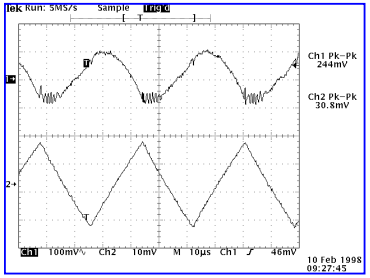


Figure 13-3: Breadboard UA723 waveforms (top - output ripple, Bottom - inductor voltage)

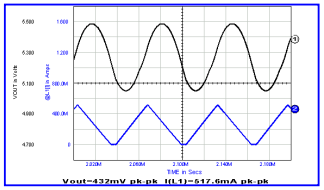


Figure 13-4: Ispice UA723 waveforms (top - output ripple, Bottom - inductor voltage)

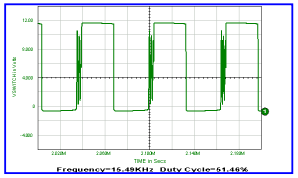


Figure 13-5: Ispice Collector Voltage of UA723 Buck Regulator

Transient domain models of a switching power supplies are extremely sensitive to the transistor model, as well as the edit controls used to govern the simulation. The turn on and turn off characteristics of the transistor model must be accurate to gain any useful information from a simulation, especially at higher frequencies. Convergence can be a major factor in the simulation of a transient domain model. By loosening the restraints on the numeric integration process (RELTOL, VNTOL, ABSTOL), convergence may be achieved, as well as a faster simulation times, at the expense of accuracy. Once convergence and proper simulation results has been established, simulation accuracy can be increased over a shorter run time to obtain accurate results, which was done in the previous simulation results. The simulation was performed substituting transistor TIP-42, with a QSB1071A. The results of this simulation, which is shown in Figure 13-6 and Figure 13-7 correlate better to the measured data. The only difference is the transistor model. To illustrate the importance of the .OPTIONS statement, the original simulation of circuit shown in Figure 13-1 was simulated with the following .OPTIONS statement:

.OPTIONS METHOD=GEAR RELTOL=.01 GMIN=1N

This was changed from the previous .OPTIONS statement of :

.OPTIONS METHOD=GEAR RELTOL=.001

The results of this simulation are shown in Figure 13-8. Notice the shape of the TIP-42 collector wave form.

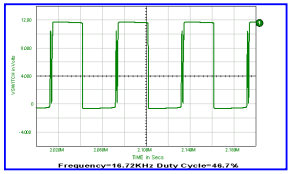


Figure 13-6: Ispice Collector Voltage of UA723 Buck Regulator With QSB1071A

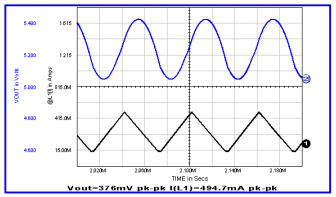


Figure 13-7: Ispice UA723 waveforms (top - output ripple, Bottom - inductor voltage) With QSB1071A

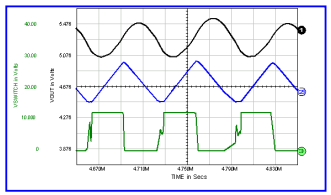


Figure 13-8: Ispice UA723 waveforms (top - output ripple, Bottom - inductor voltage) With TIP-42

Condition	Breadboard	TIP-42	TIP-42*	QSB1071A
Frequency	27.82KHz	15.49KHz	14.29KHz	16.72KHz
Vout pk-pk	244mV	422mV	626mV	376mV
Vout	5.22 V	5.27 V	5.28 V	5.24 V
Inductor Current	308mA	517.6mA	550.8mA	494.7mA
Run Time	NA	82.93 Sec	27.31 Sec	68.42 Sec

Table 13-1:Summary of Results

*.OPTIONS METHOD=GEAR RELTOL=.01 GMIN=1N

The results indicate a trade off between simulation run time and simulation accuracy. Also, the selection on the transistor can have dramatic effects on the results of the simulation.

The simulation results do not correlate well to the hardware. A possible cause is the ESR of a Mallory TDC106K505WSG 10uF capacitor, C2. The feedback loop is originated at the collector of the PNP transistor to avoid sensitivity to the ESR of the output capacitor. However, investigation into the poor correlation indicates that the circuit is sensitive to the ESR of capacitor C2. A measurement of the ESR was made using a HP 3577A network analyzer, which is shown in Figure 13-10.

The setup to make the measurement of capacitor C2, inverted the signal, which is why the ESR measurement is inverted. The ESR of capacitor C2 is dependant on frequency. The hardware frequency is approximately 27KHz. The ESR at this frequency is approximately 386 mOhms.

Another schematic, which reflects the appropriate ESR of C2 and the DCR of inductor L1, is shown below in Figure 13-9. The schematic includes the circuitry that was used to measure the transient response of the hardware.

The measured and simulated data is shown in Figure 13-10 through Figure 13-15.

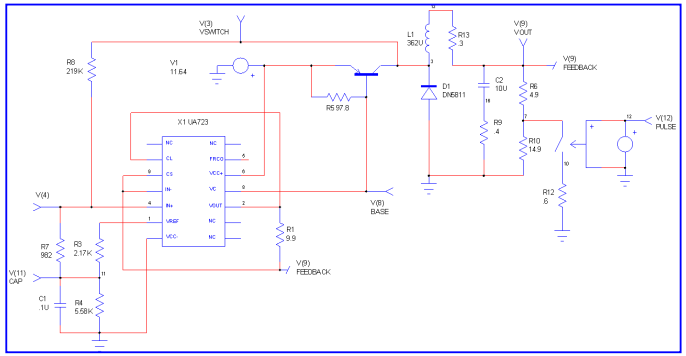


Figure 13-9: UA723 Buck Regulator with Measured ESR and DCR.

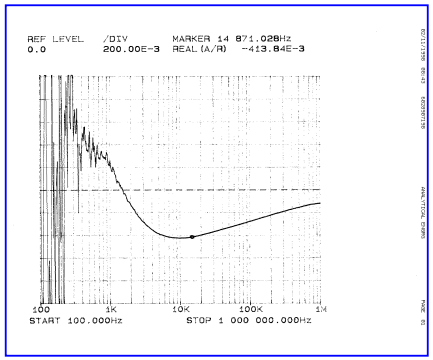


Figure 13-10: Measured ESR of C2

A precarious dilemma results when creating a model that can accurately depict a transient response of the converter as well as the output ripple. The ESR of capacitor C2 is a function of frequency. When simulating the output ripple of the converter, the frequency is essentially constant, approximately 25KHz. However, when the converter encounters a transient, the response is at a much lower frequency, approximately 5KHz. ESR for the transient response simulation is different from the output ripple simulation. The solution is to either create a capacitor model that has ESR, which varies with frequency, or change the ESR to the appropriate value for each simulation. The ESR of capacitor C2 maintains relatively constant from 5KHz through 20KHz, but varies immensely outside of these frequencies.

In correlating to the transient response, many difficulties arose. The ESR of C2 determines the magnitude of the transient response, as well as the frequency of the output ripple. Varying the ESR of C2, varies where in the period of the output ripple that the transient occurred. A larger magnitude of the transient response corresponds to the transient occurring while the transistor is conducting, which indicates that the simulation results are dependent on when the transient occurs.

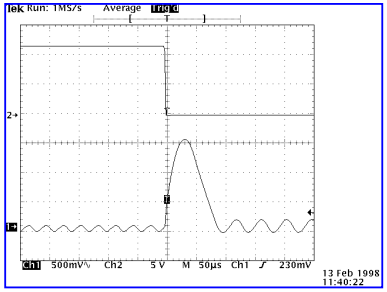


Figure 13-11: Measured UA723 Buck Regulator Transient Response

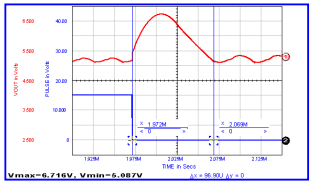


Figure 13-12: Ispice UA723 Buck Regulator Transient Response

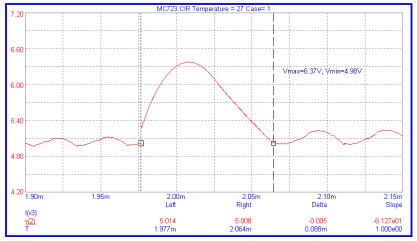


Figure 13-15: Micro-Cap V UA723 Buck Regulator Transient Response

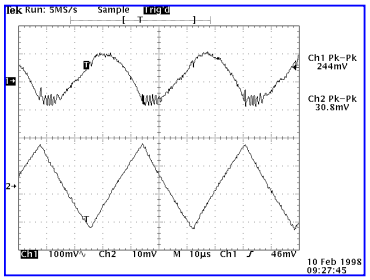


Figure 13-3: Breadboard UA723 waveforms (top - output ripple, Bottom - inductor voltage)

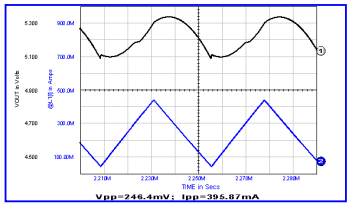


Figure 13-13: Ispice UA723 Buck Regulator Output Ripple

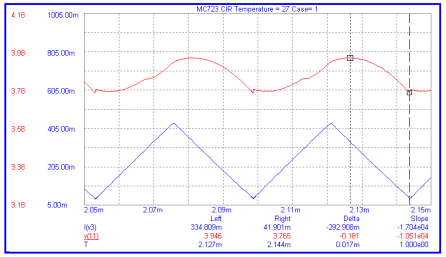


Figure 13-14: Micro-Cap V UA723 Buck Regulator Output Ripple

Condition	Breadboard	Ispice	Micro-Cap V
Frequency	27.82KHz	21.3KHz	22KHz
Vout (pk-pk)	244mV	246mV	292mV
Vout (Avg)	5.22 V	5.21	5.11
Inductor Current	308mA	395.9mA	396mA

Transient Response (pk-pk)	1.6V	1.63V	1.39V
Response Duration	90uS	97uS	88uS
Run Time of Transient Response	NA	147.88 sec	74.56 sec

Table 13-2: Summary of Results

The circuit consisted of too many nodes for the Pspice evaluation version.

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1990 Linear Databook, Linear Technology.

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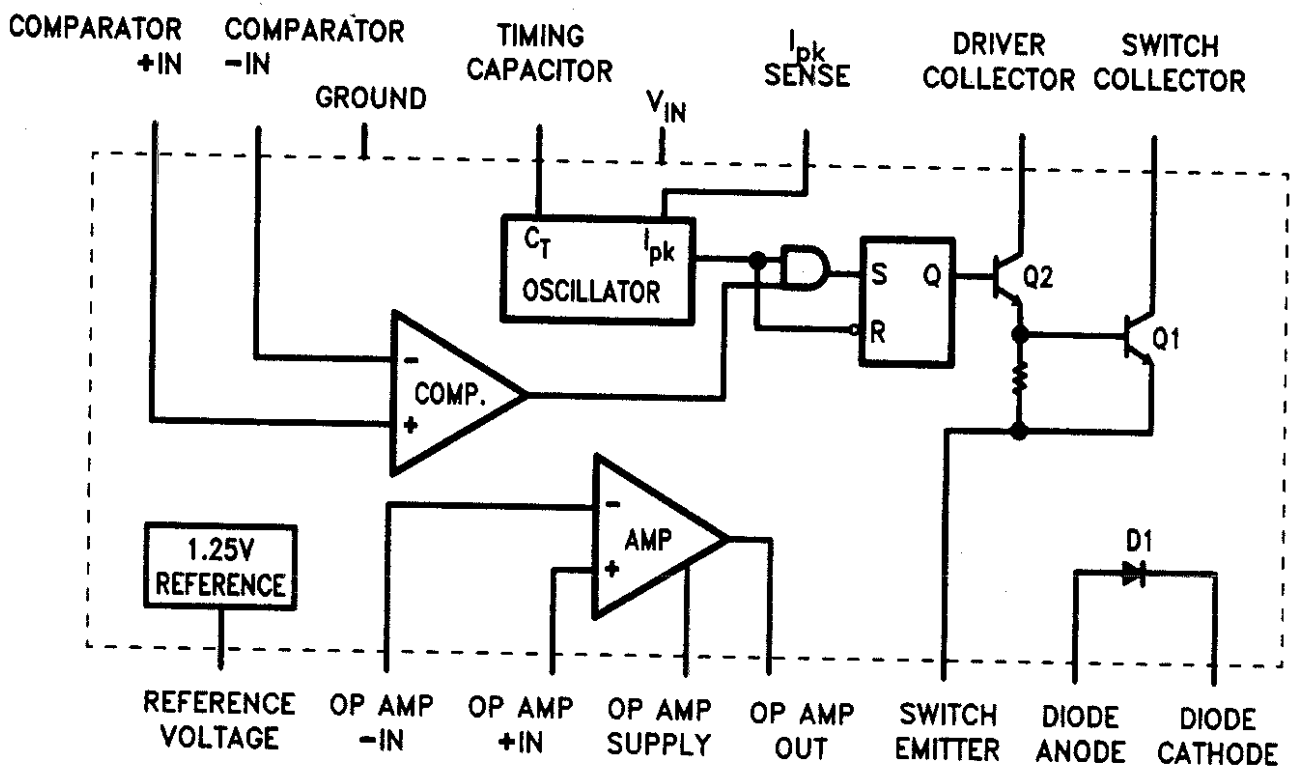
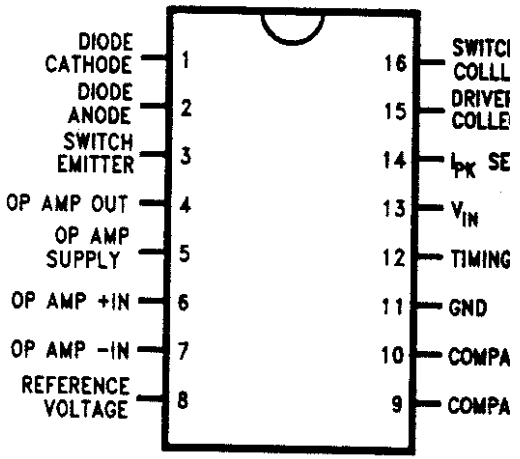


TL/H/10057–2

16-Lead DIP

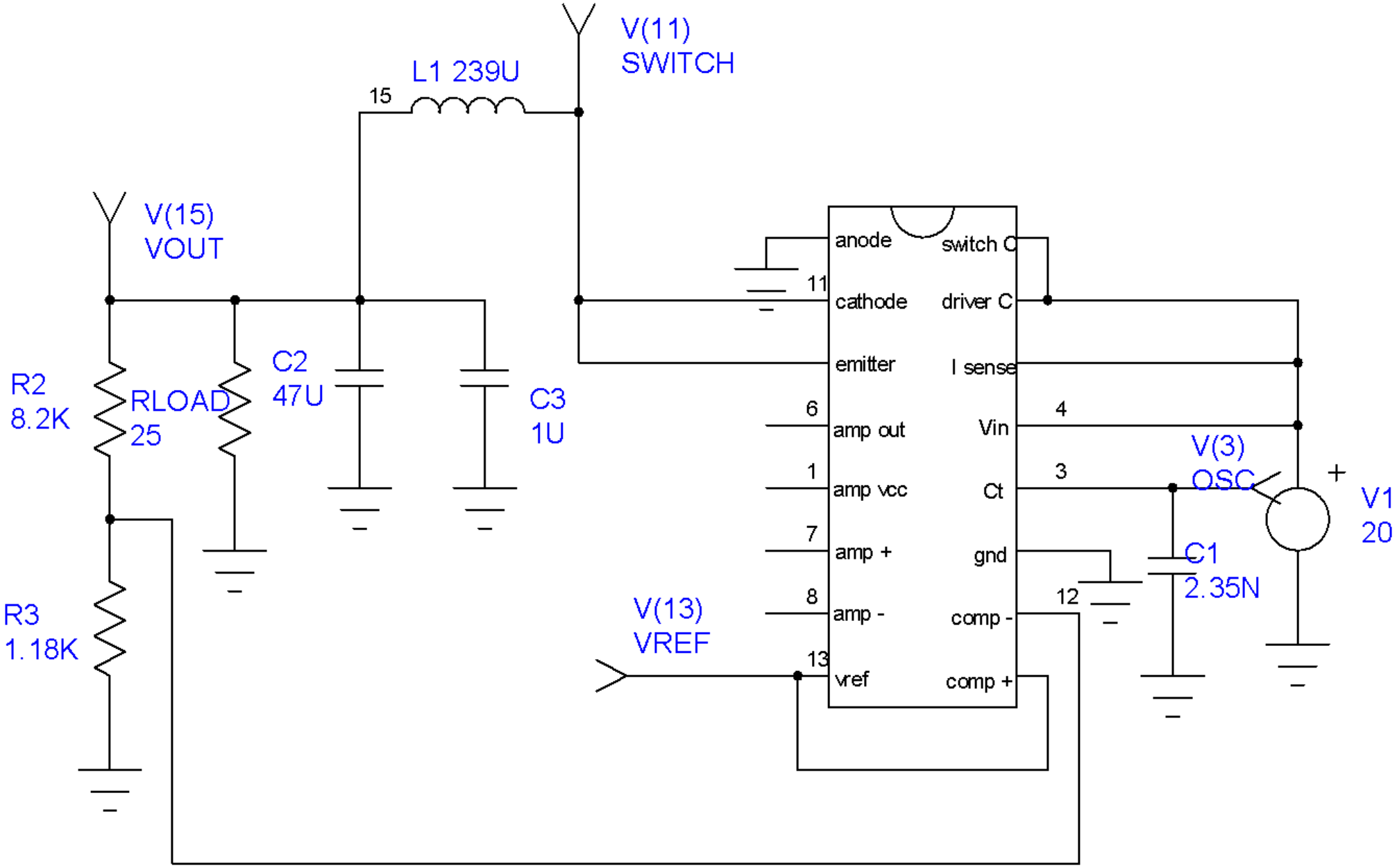


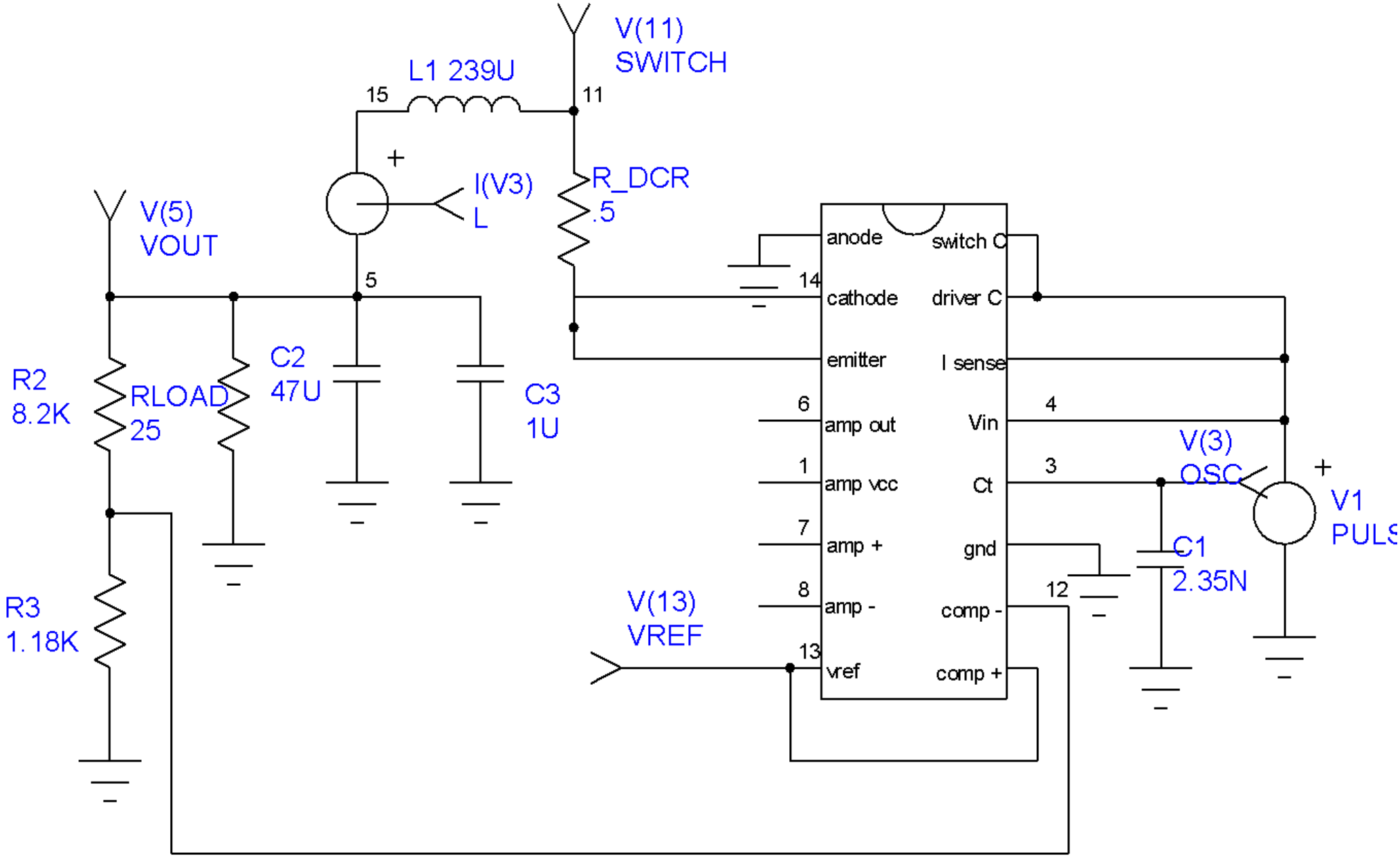
TL/H/

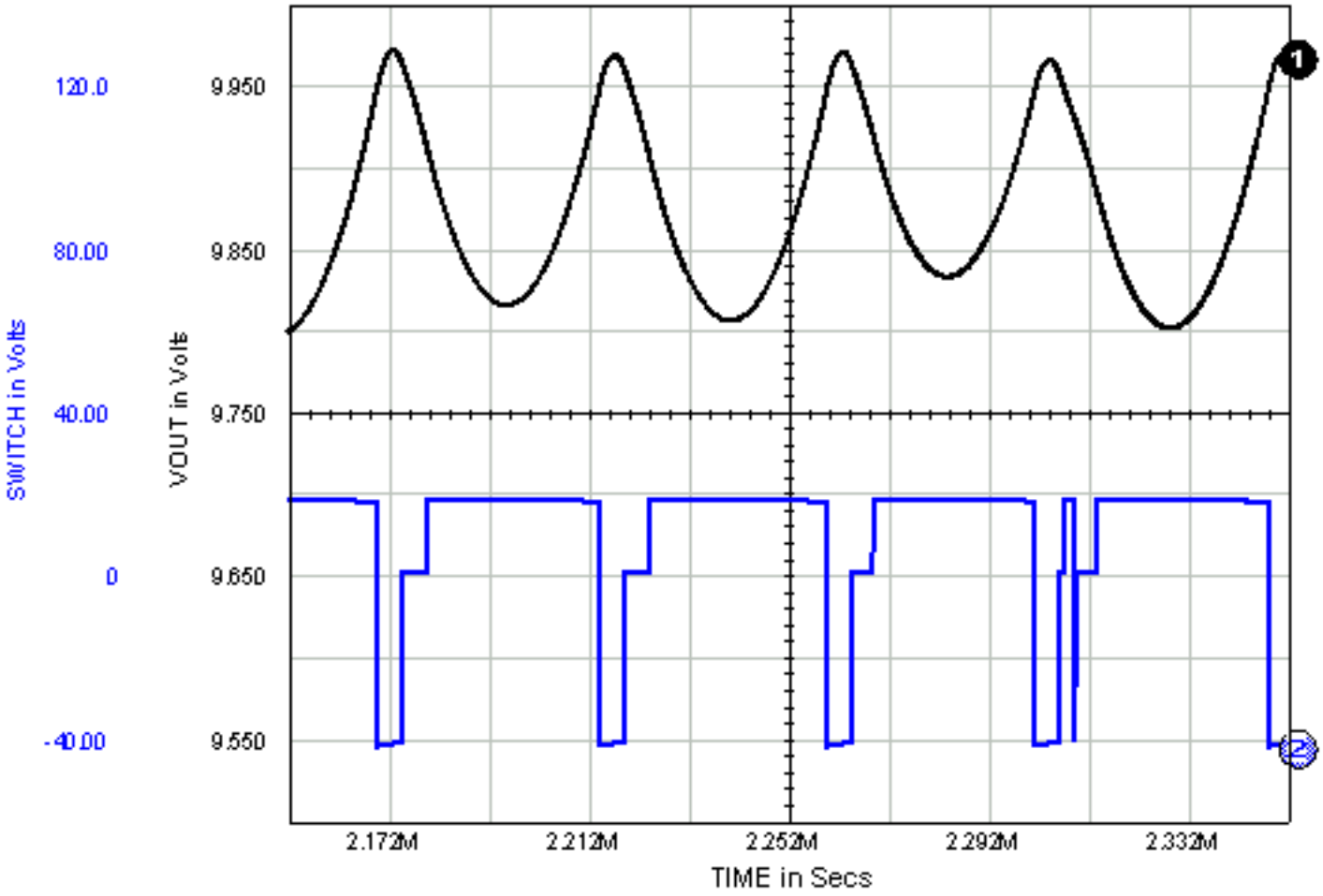
Top View

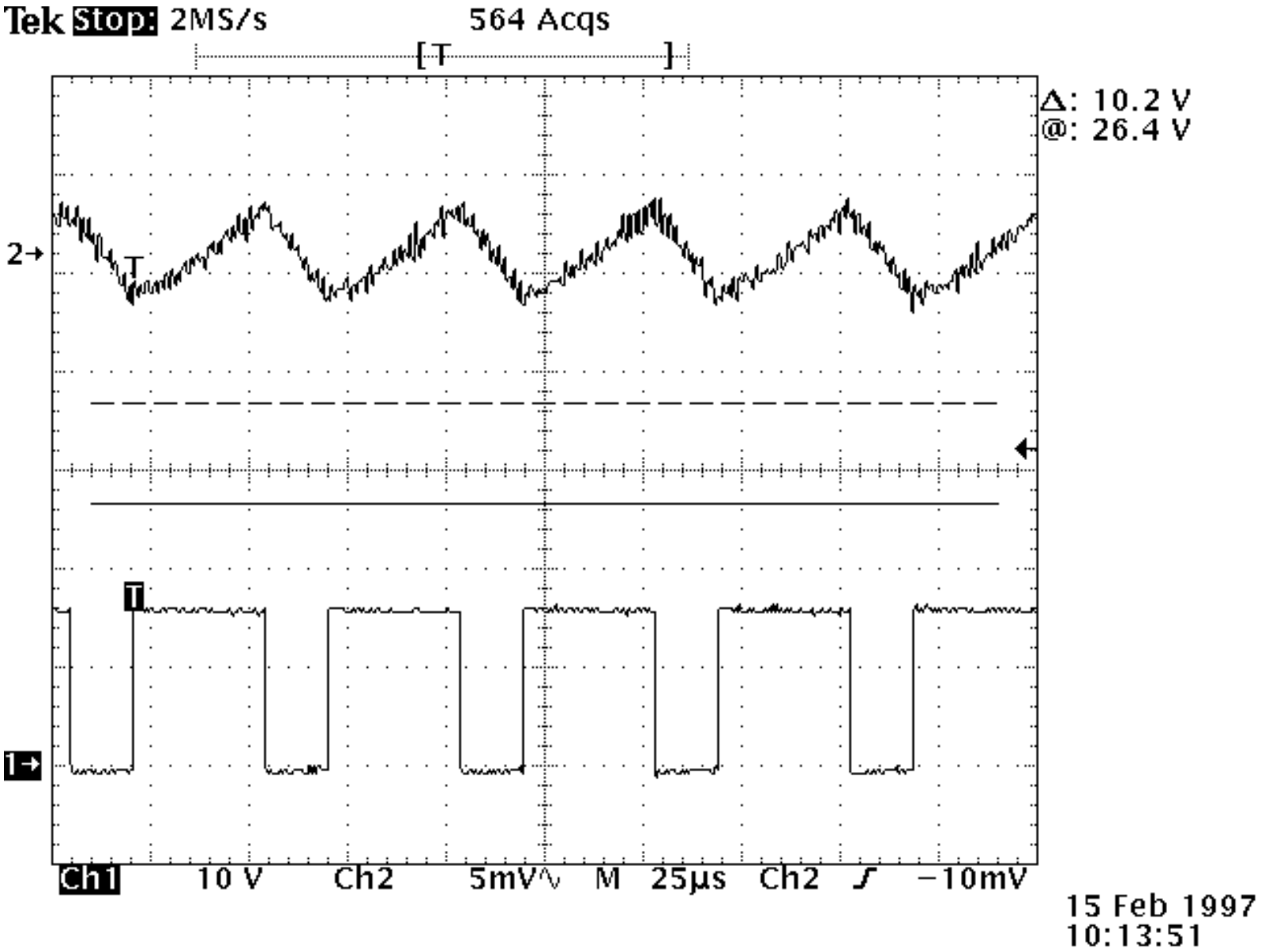
Ordering Information

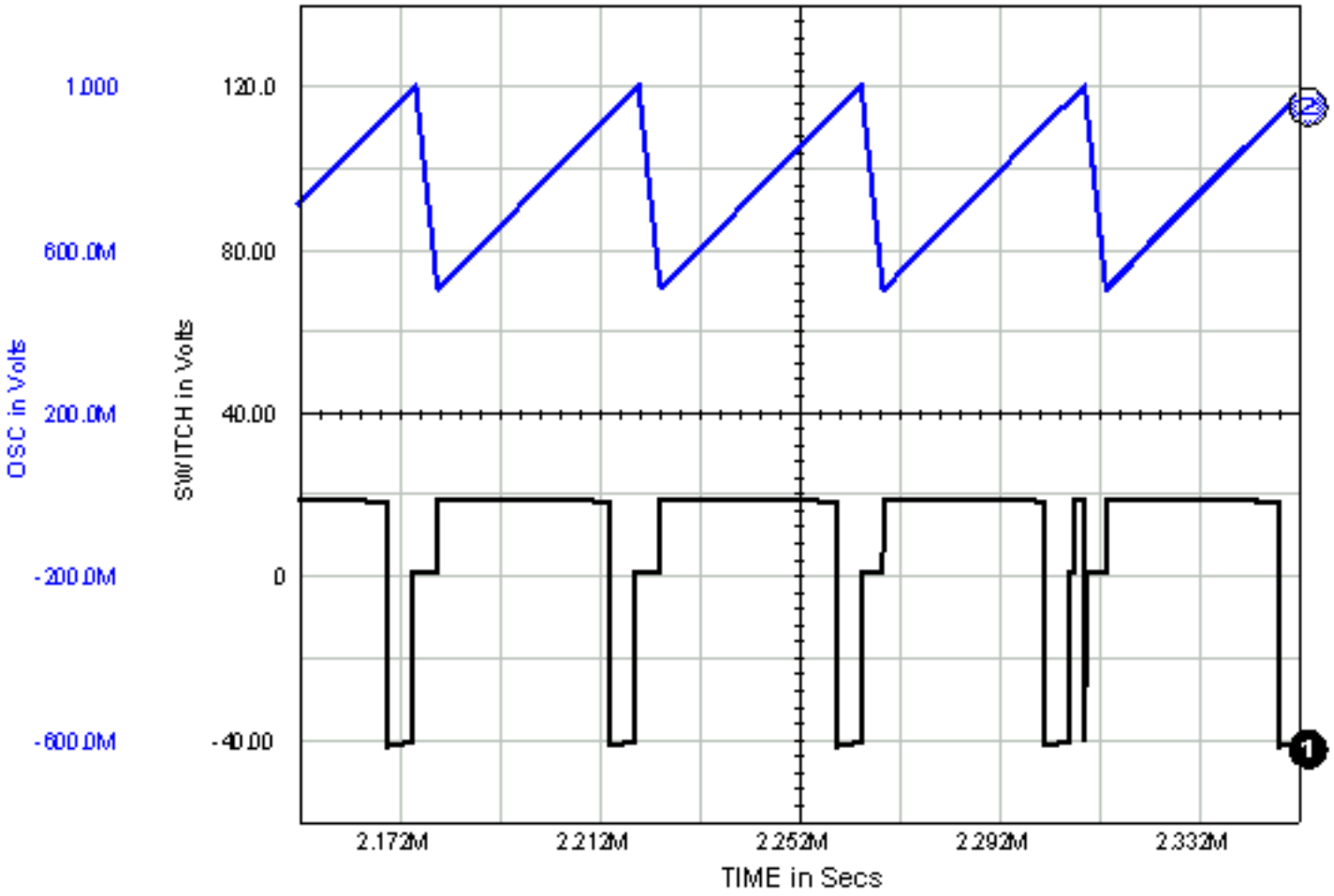
Part Number	NS Package	Temperature Range
LM78S40J LM78S40J/883	J16A Ceramic DIP J16A Ceramic DIP	−55°C to +125°C
LM78S40N	N16E Molded DIP	−40°C to +125°C
LM78S40CJ LM78S40CN	J16A Ceramic DIP N16E Molded DIP	0°C to +70°C

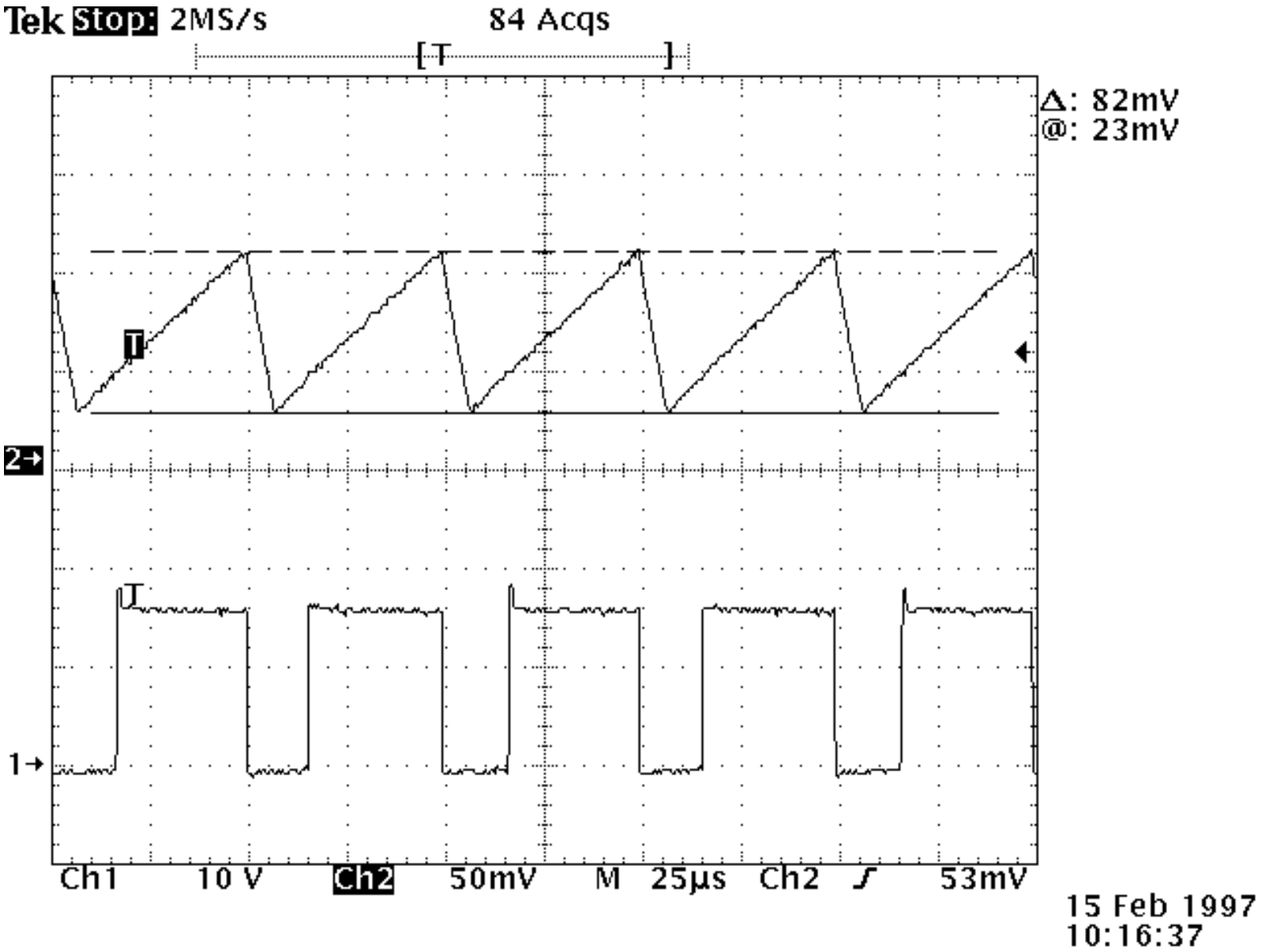

V(11)
SWITCH
L1 239U
15
V(15)
VOUT
R2
8.2K
RLOAD
25
C2
47U
C3
1U
R3
1.18K
anode
switch C
11
cathode
driver C
emitter
I sense
6
amp out
Vin
4
1
amp vcc
Ct
3
V(3)
OSC
7
amp +
gnd
C1
2.35N
12
8
amp -
comp -
V(13)
VREF
13
vref
comp +
V1
20


V(11)
SWITCH
L1 239U
15
11
+
I(V3)
L
R_DCR
.5
V(5)
VOUT
5
R2
8.2K
RLOAD
25
C2
47U
C3
1U
R3
1.18K
anode
switch C
14
cathode
driver C
emitter
I sense
6
amp out
Vin
4
1
amp vcc
Ct
3
7
amp +
gnd
8
amp -
comp -
12
V(13)
VREF
13
vref
comp +
V(3)
OSC
+
V1
PULS
C1
2.35N


120.0
80.00
40.00
0
-40.00
SWITCH in Volts
9.950
9.850
9.750
9.650
9.550
VOUT in Volts
2.172M
2.212M
2.252M
2.292M
2.332M
TIME in Secs
1
2


Tek Stop: 2MS/s
564 Acqs
Δ: 10.2 V
@: 26.4 V
2→
1→
Ch1 10 V Ch2 5mV M 25µs Ch2 −10mV
15 Feb 1997
10:13:51


1.000
600.0M
200.0M
-200.0M
-600.0M
OSC in Volts
120.0
80.00
40.00
0
-40.00
SWITCH in Volts
2.172M
2.212M
2.252M
2.292M
2.332M
TIME in Secs
2
1


Tek Stop: 2MS/s
84 Acqs
Δ: 82mV
@: 23mV
Ch1 10 V
Ch2 50mV
M 25µs
Ch2 53mV
15 Feb 1997
10:16:37

#14: 1524A Buck Regulator

The SG1524A advanced regulating pulse width modulator can be configured to create a voltage mode controlled buck regulator. This type of regulator will produce an output voltage which is proportional to the duty cycle. The duty cycle is a function of input voltage and loading. The switched voltage is averaged by an L-C filter, which produces a DC output voltage.

There are two types of models that can be utilized to analyze switching circuits. The first is an averaged or state space model, which represent the operation of the switching circuit via linear techniques. All linear circuits fall into the category of average models. The benefits of using an average model are, extremely fast simulation times, reasonable accuracy, and they support AC as well as transient domain simulations. Averaged models can be used for predicting phase and gain margins, conducted susceptibility, and input and output impedance.

Transient models represent the actual function of the circuit in the time domain. This type of model is useful in determining the time domain characteristics of a circuit. These models can be very accurate, and display switching spikes, ripple, and propagation delays, and other transient characteristics associated with switching circuits. There are two major disadvantages to using a transient model. Because the simulation accurately models the time domain switching characteristics of the circuit, a simulation run can take a considerable amount of time. Higher frequency circuits require smaller step sizes to accurately predict the time domain characteristics, which increases simulation run times. Transient models cannot be used to determine the AC characteristics of a circuit.

The schematic of the SG1524 Buck Regulator is shown in Figure 24-1. The values of the capacitors and resistors are measured values.

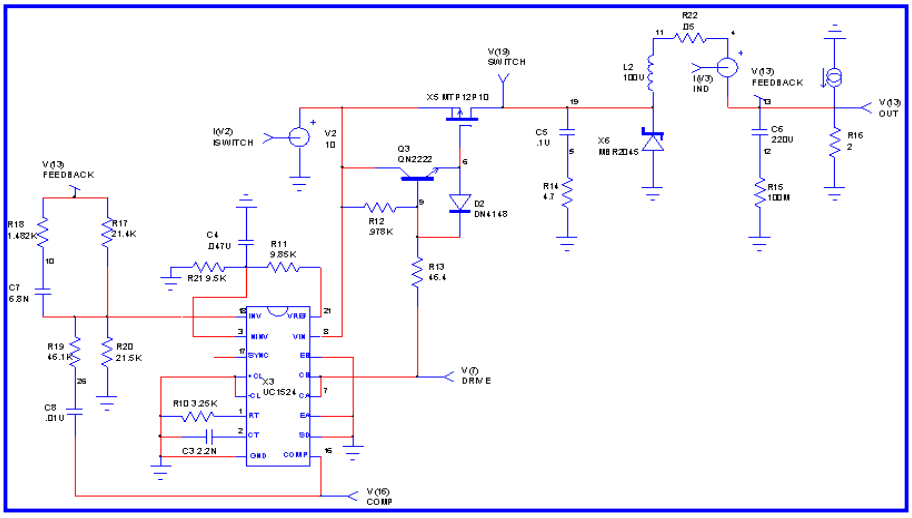


Figure 14-1: Schematic of SG1524 Buck Regulator

The phase and gain margins were measured using an average model of the SG1524 buck regulator. The Schematic of the average model is shown in Figure 14-2.

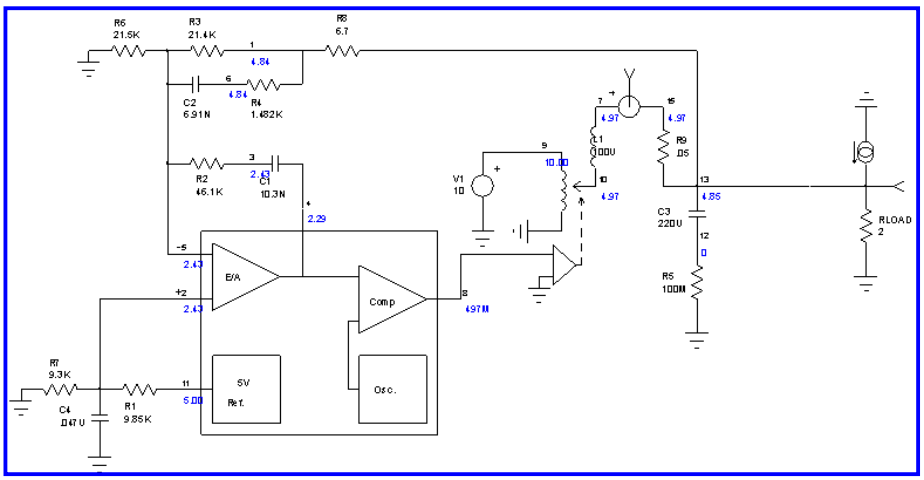


Figure 14-2: SG1524 Buck Regulator Average Model

There are five parameters that must be passed to the average SG1524 model.

T=6.44uSec Switching Period

TO=300nSec Dead Time

TS=100nSec Transistor Storage Time

EP=3.7V Peak Saw Voltage

EO=.85V Minimum Saw Voltage

These values were measured on the breadboard circuit, which is shown in Figure 14-3 and Figure 14-4.

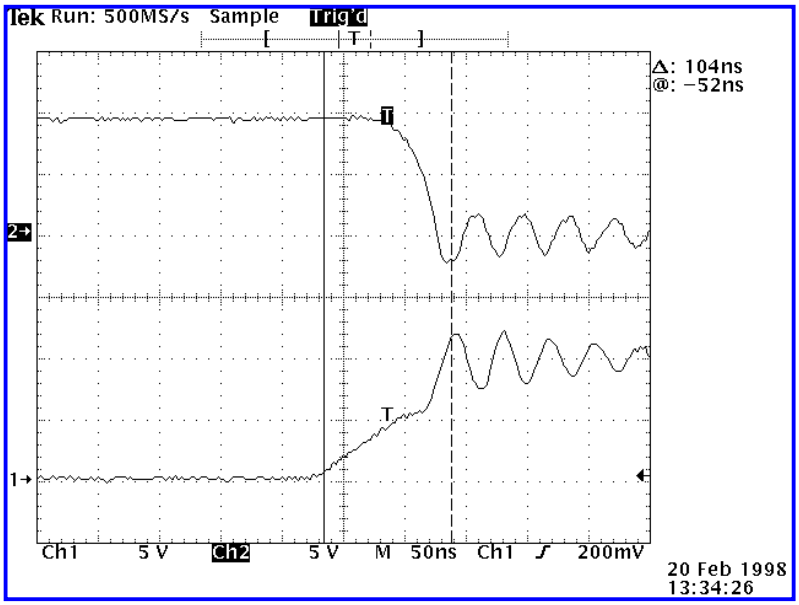


Figure 14-3: Transistor Storage Time

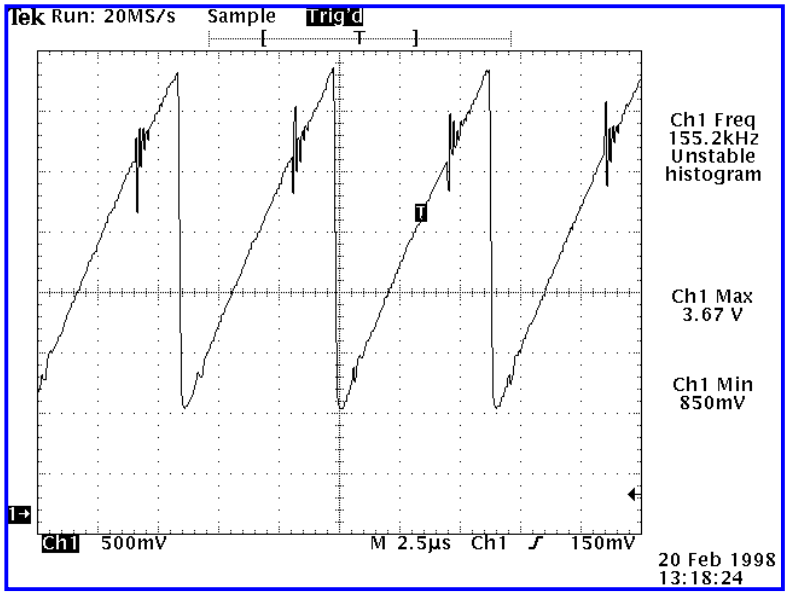


Figure 14-4: Saw Wave Form Resulting from Rt and Ct

The following equations are used to predict the pole and zero locations of the feedback loop. The output filter causes a double pole at:

$$L_2 := 100\,10^{-6}$$

$$C_6 := 220\,10^{-6}$$

$$F_1 := \frac{1}{2\cdot\pi\cdot\sqrt{L_2\cdot C_6}}$$

$$F_1 = 1.073\,10^{3}$$

One of these two poles is canceled by R17 and C7

$$R_{17} := 2140$$

$$C_7 := 6.8\,10^{-9}$$

$$F_2 := \frac{1}{2\cdot\pi\cdot R_{17} C_7}$$

$$F_2 = 1.094\,10^{3}$$

A third pole is created by capacitor C8, and Resistor R19

$$R_{19} := 4610$$

$C_8 := .011 \cdot 10^{-6}$

$$F_3 := \frac{1}{2 \cdot \pi \cdot R_{19} C_8}$$

$F_3 = 345.238$

A zero is caused by the output filter capacitor, and the ESR of the output filter capacitor.

$C_6 := 220 \cdot 10^{-6}$

$R_{15} := 100 \cdot 10^{-3}$

$$F_4 := \frac{1}{2 \cdot \pi \cdot R_{15} C_6}$$

$F_4 = 7.234 \cdot 10^{3}$

This zero gets cancelled by R18, and C7

$C_7 := 6.8 \cdot 10^{-9}$

$R_{18} := 1.428 \cdot 10^{3}$

$$F_5 := \frac{1}{2 \cdot \pi \cdot R_{18} C_7}$$

$F_5 = 1.639 \cdot 10^{4}$

Because the ESR of the output filter capacitor creates a zero, it is essential to measure this term. The ESR measurement of output filter capacitor C6 is shown below in Figure 14-3. The ESR is approximately equal to 100mOhms at the bandwidth of the converter.

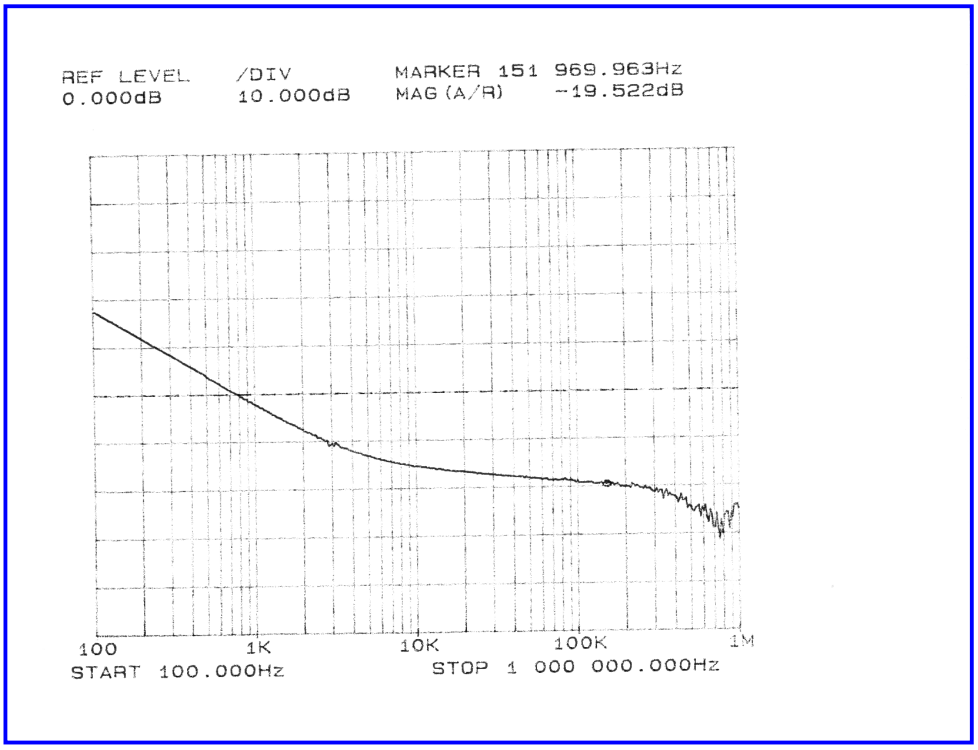


Figure 14-5: ESR of Output Filter Capacitor C6

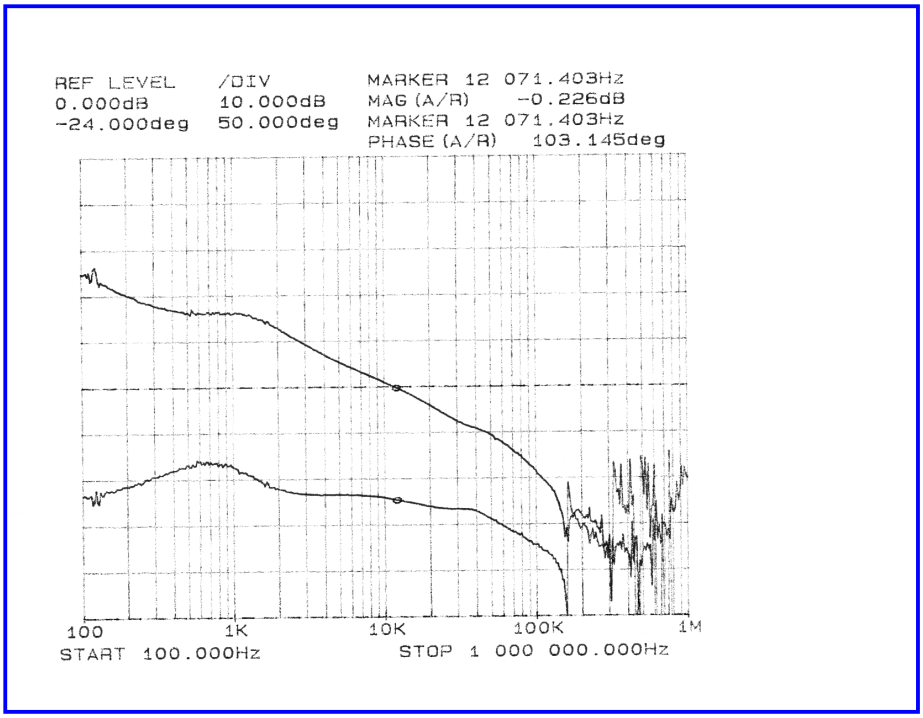


Figure 14-6: Measured Phase and Gain Margins

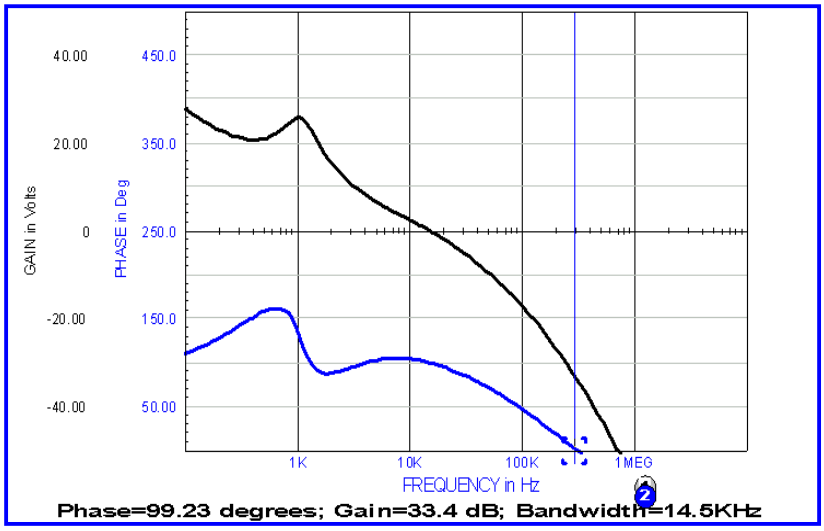


Figure 14-7: Simulated Phase and Gain Margins

The transient domain model shown in Figure 14-1 was used to measure output ripple voltage, transient response, gate voltage and inductor current. This model properly predicts the cycle by cycle switching effects of the regulator.

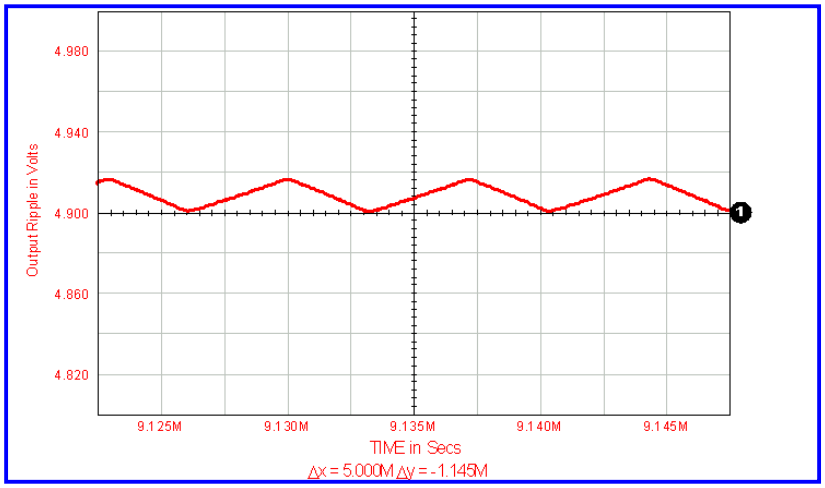


Figure 14-8: Simulated Output Ripple

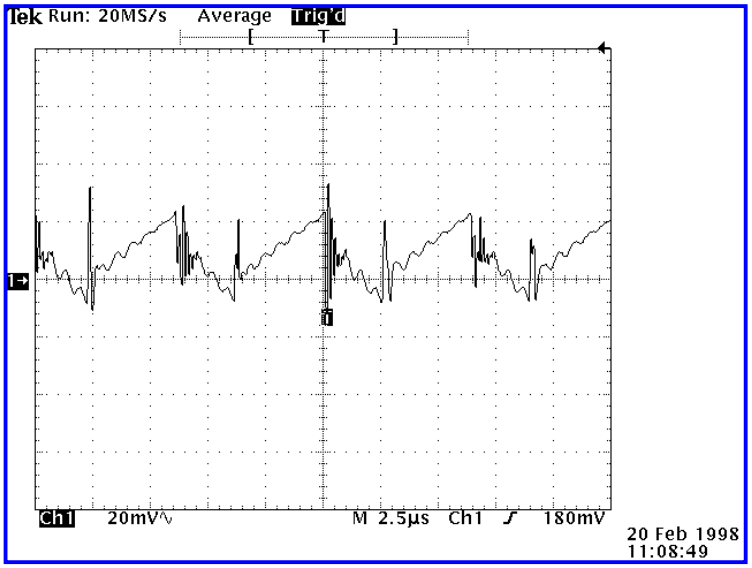


Figure 14-9: Measured Output Ripple

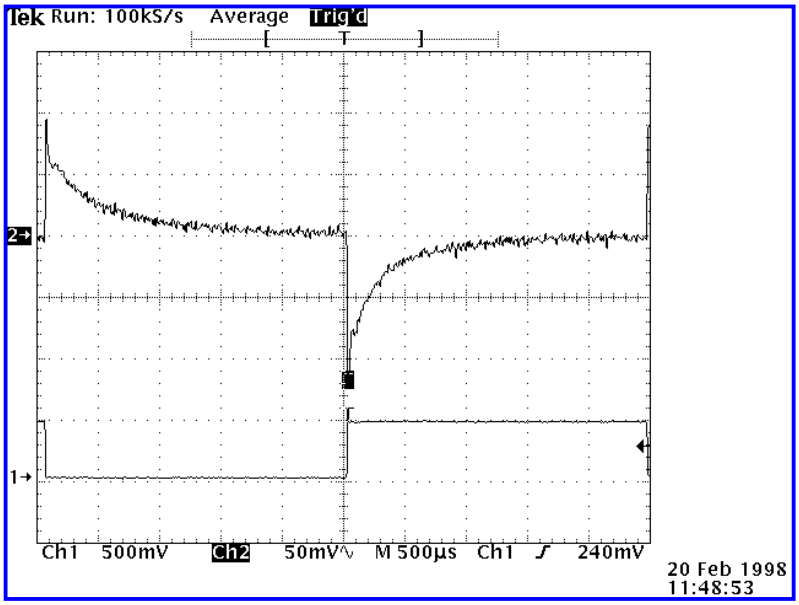


Figure 14-10: Measured Transient Response

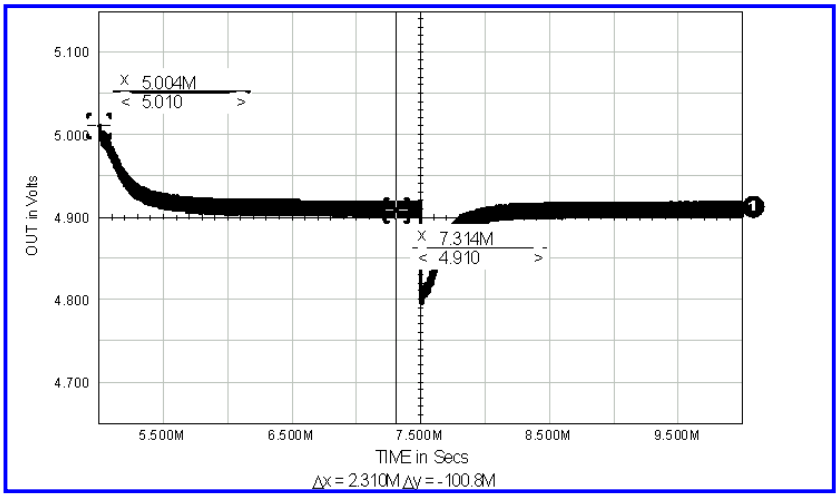


Figure 14-11: Simulated Transient Response

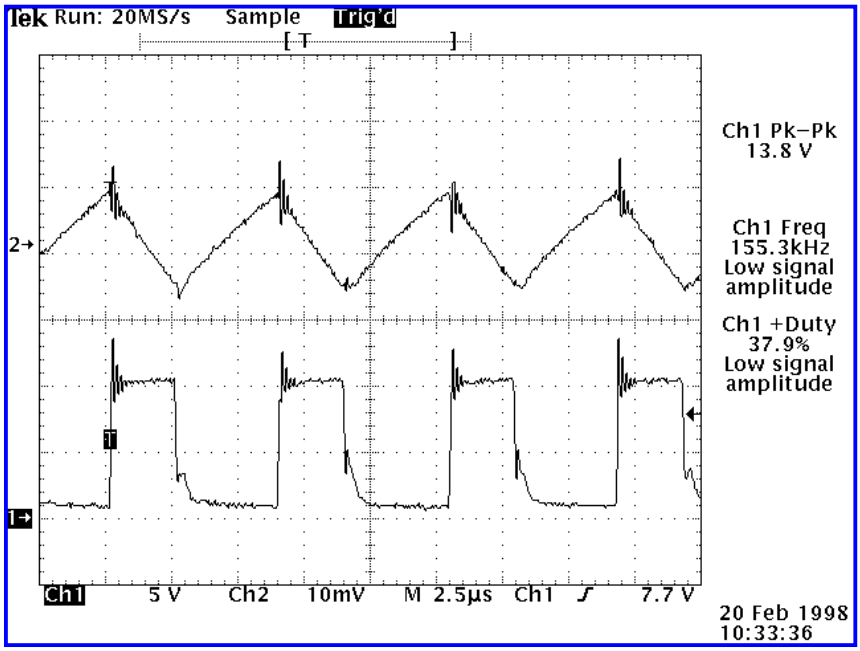


Figure 14-12: Measured Output Inductor Current and Gate Drive Voltage

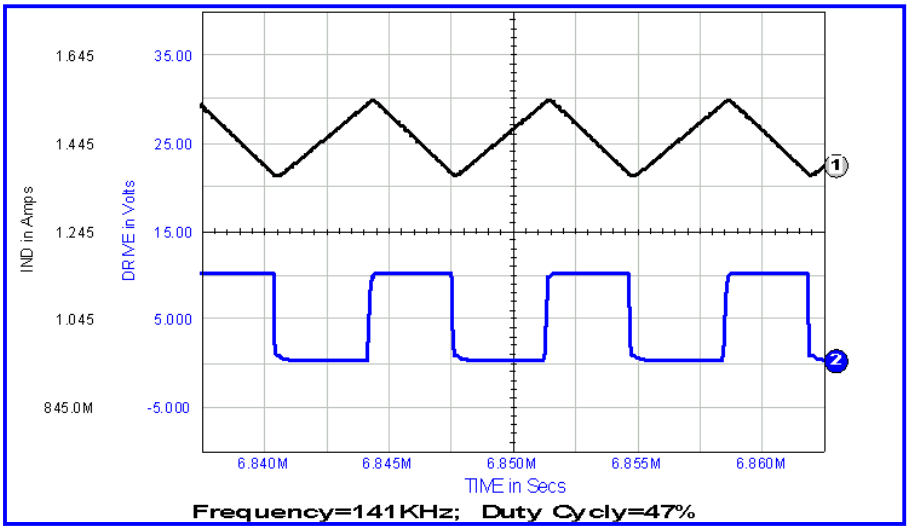


Figure 14-13: Output Inductor Current and Gate Drive Voltage

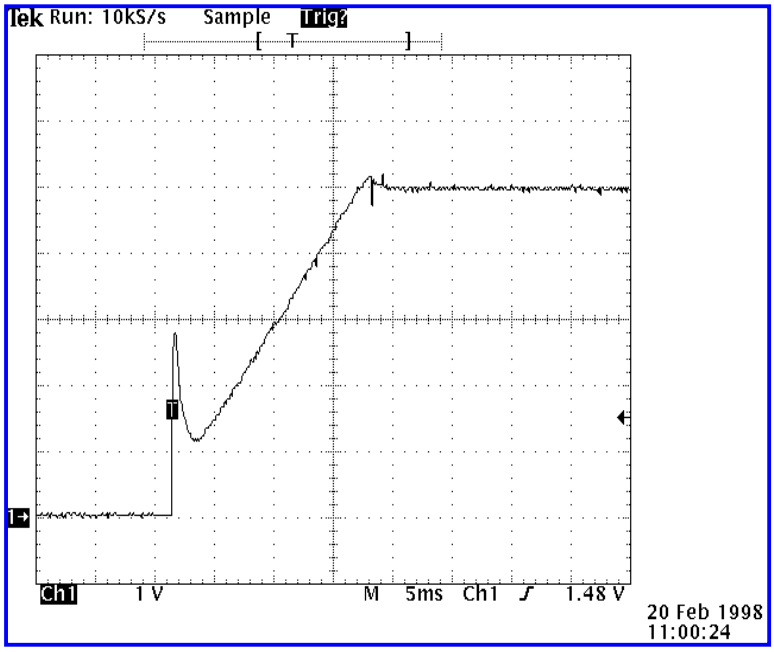


Figure 14-14: Measured Turn On of SG1524 Buck Regulator

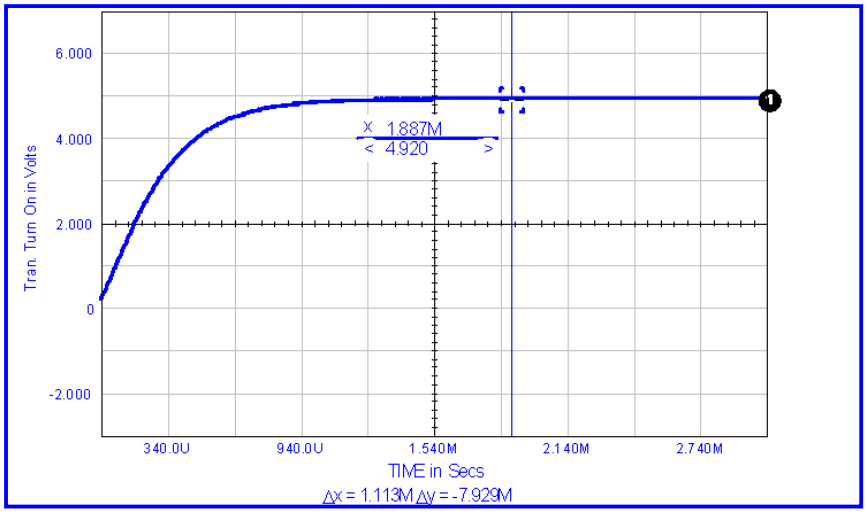


Figure 14-15: Simulated Turn On of SG1524 Buck Regulator Using Transient Model

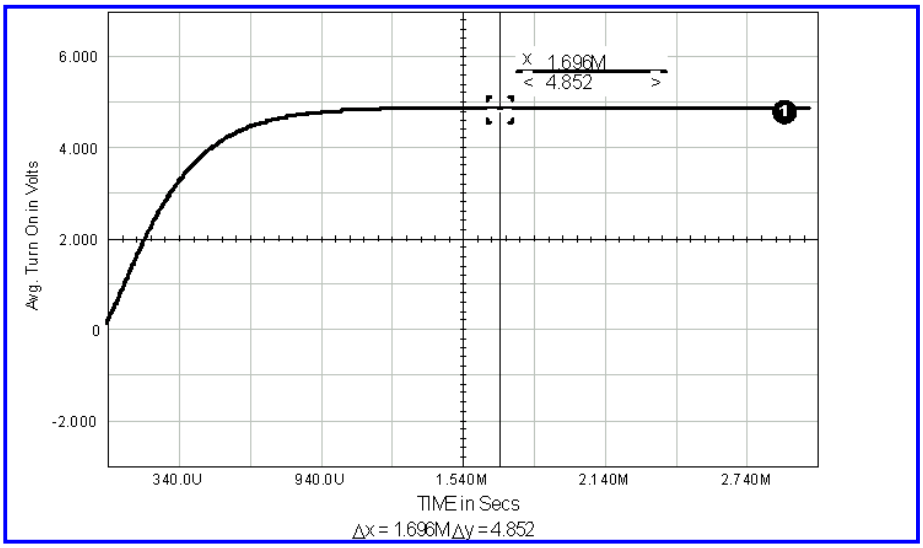


Figure 14-16: Simulated Turn On of SG1524 Buck Regulator Using Average Model

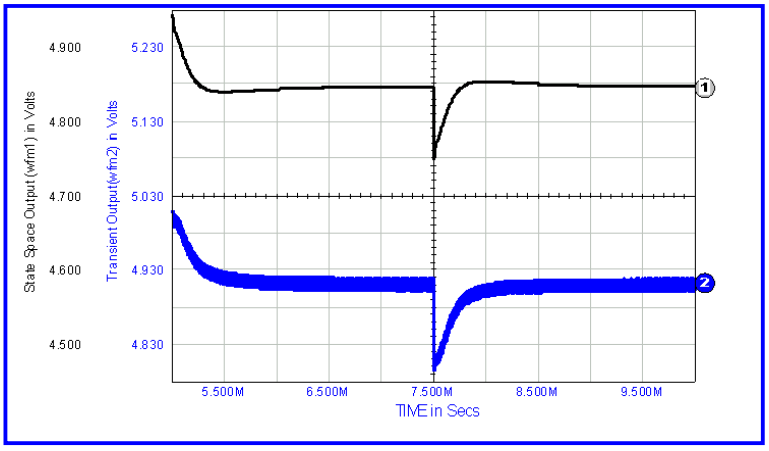


Figure 14-17: Average -Vs- Transient Model Step Load Response

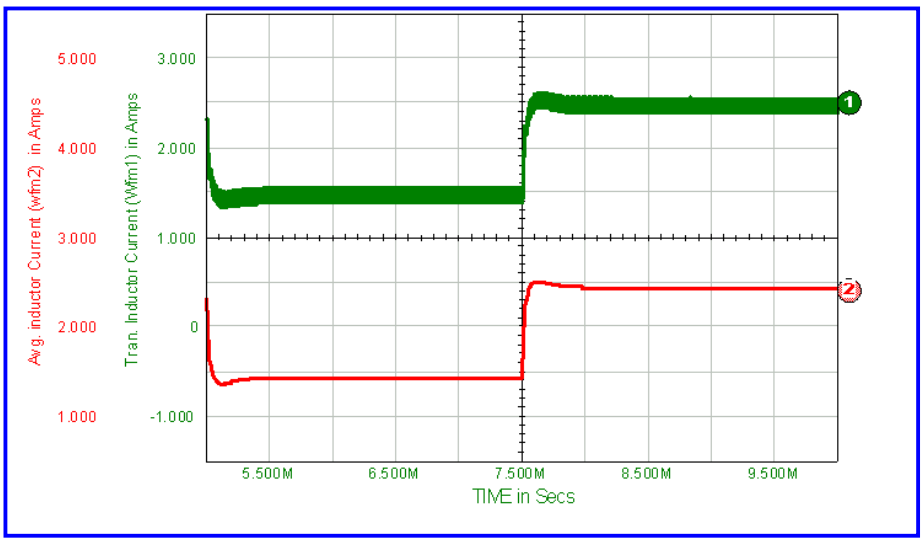
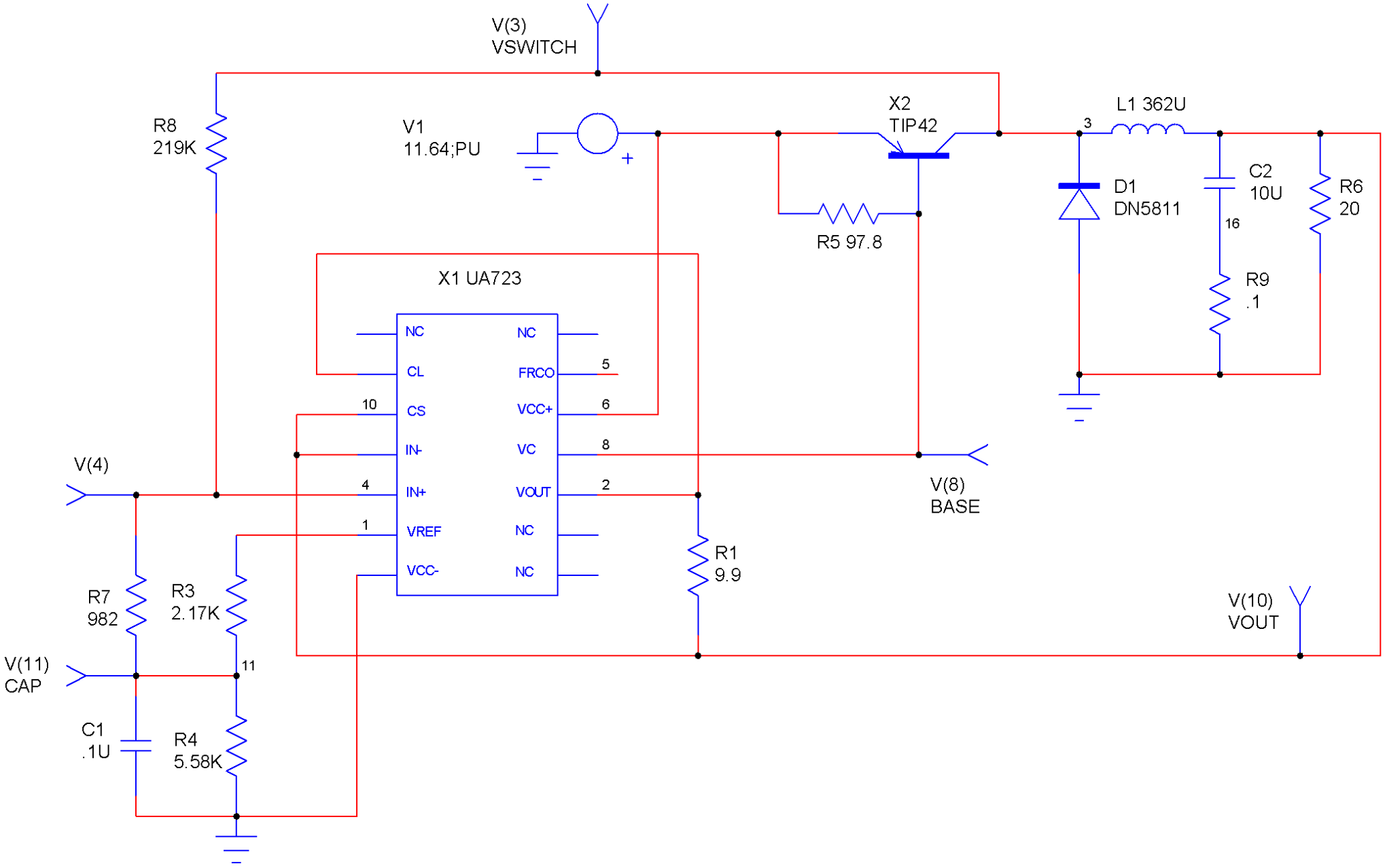
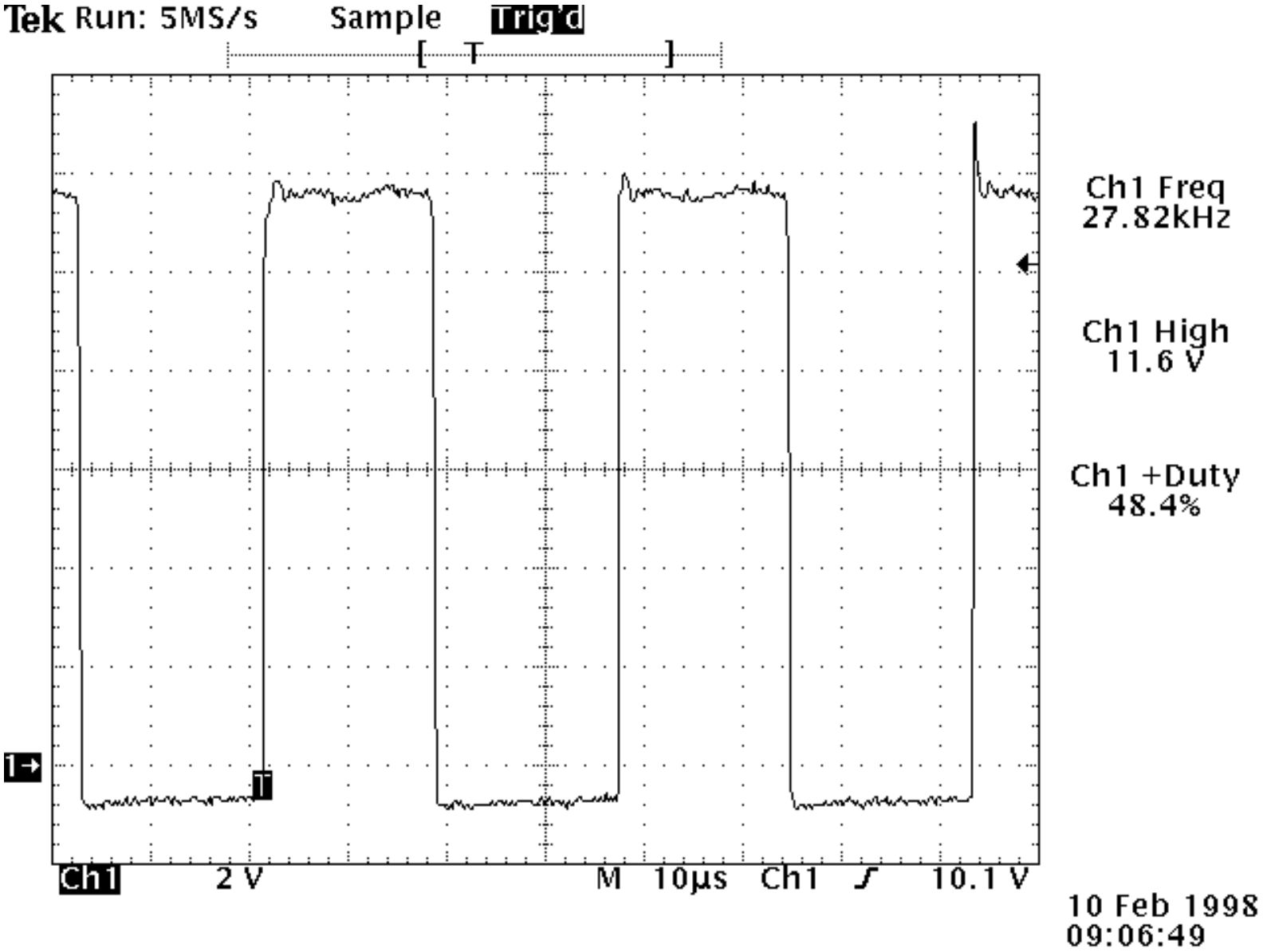


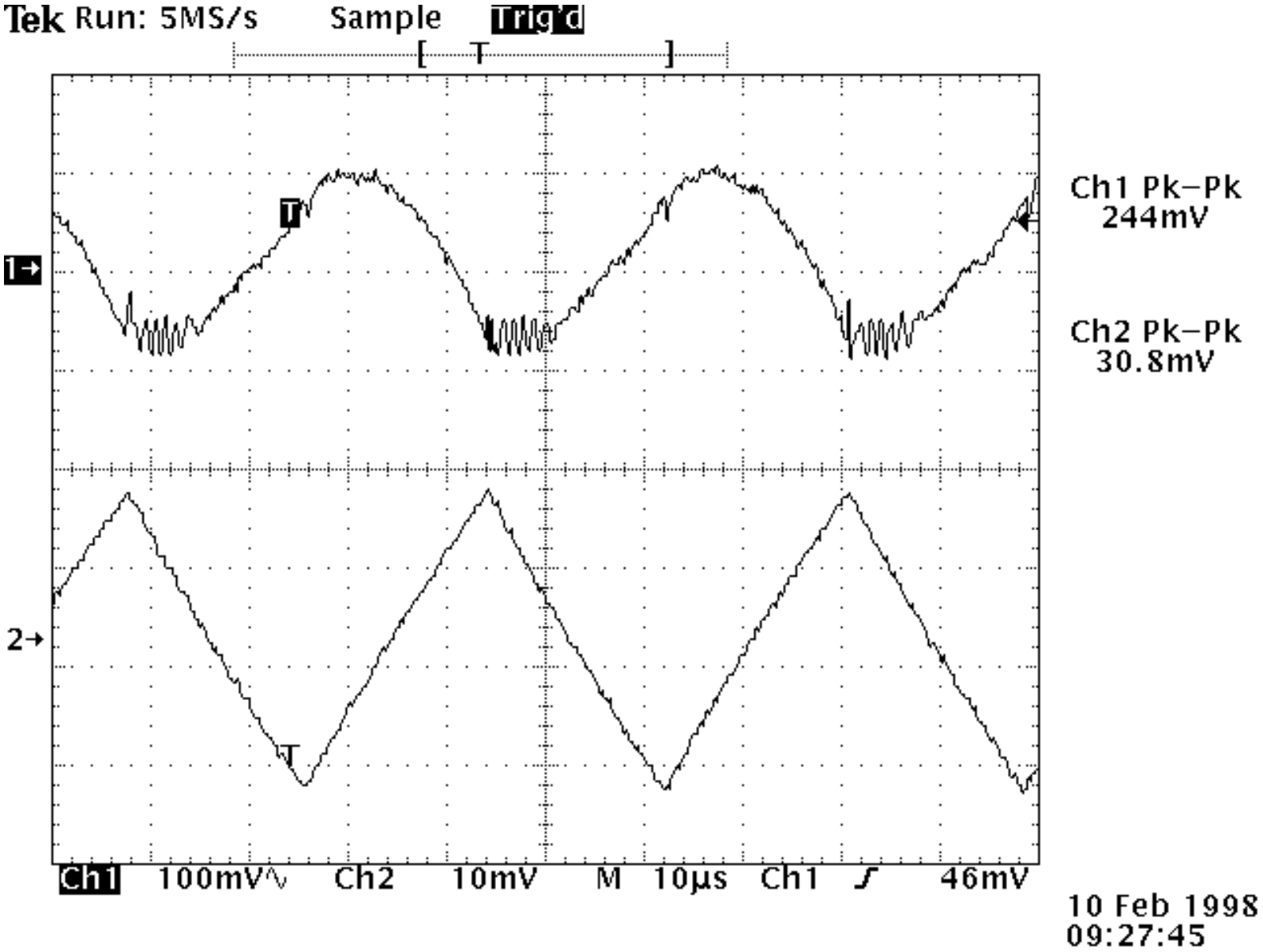
Figure 14-17: Average -Vs- Transient Model Step Load Response of Inductor Current

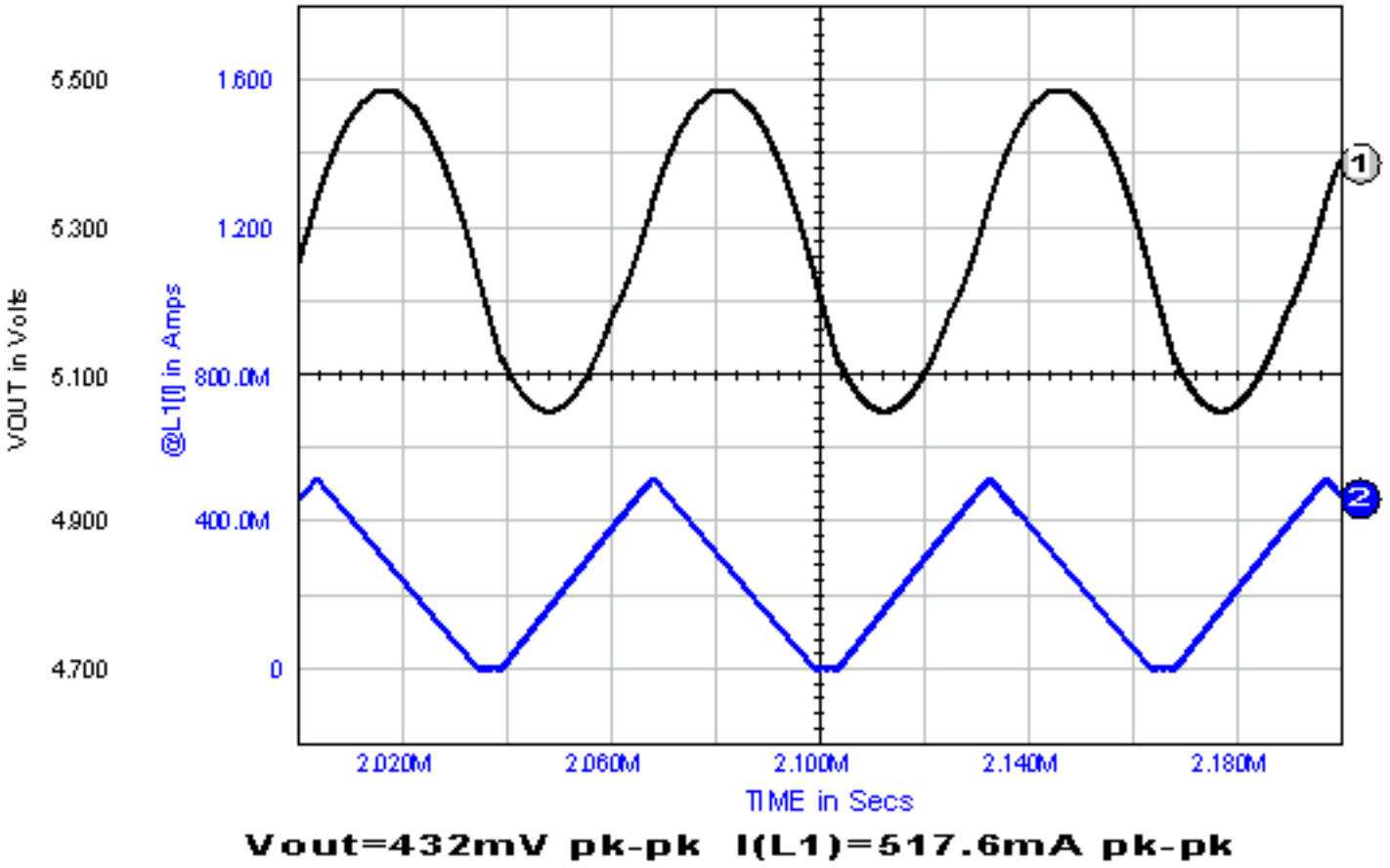
Table 14-1: Spice Statistics (The SG1524 model is only available in Ispice)

File Name	Type of Simulation	Type of Model	Run Time
AVG_TON	Transient	Average	2.98 Sec
1524_TON	Transient	Transient	514.73 Sec
AVG_TRAN	Transient	Average	3.08 Sec
SG1524	Transient	Transient	1713.58 Sec
AVG1524	AC	Average	1.02 Sec

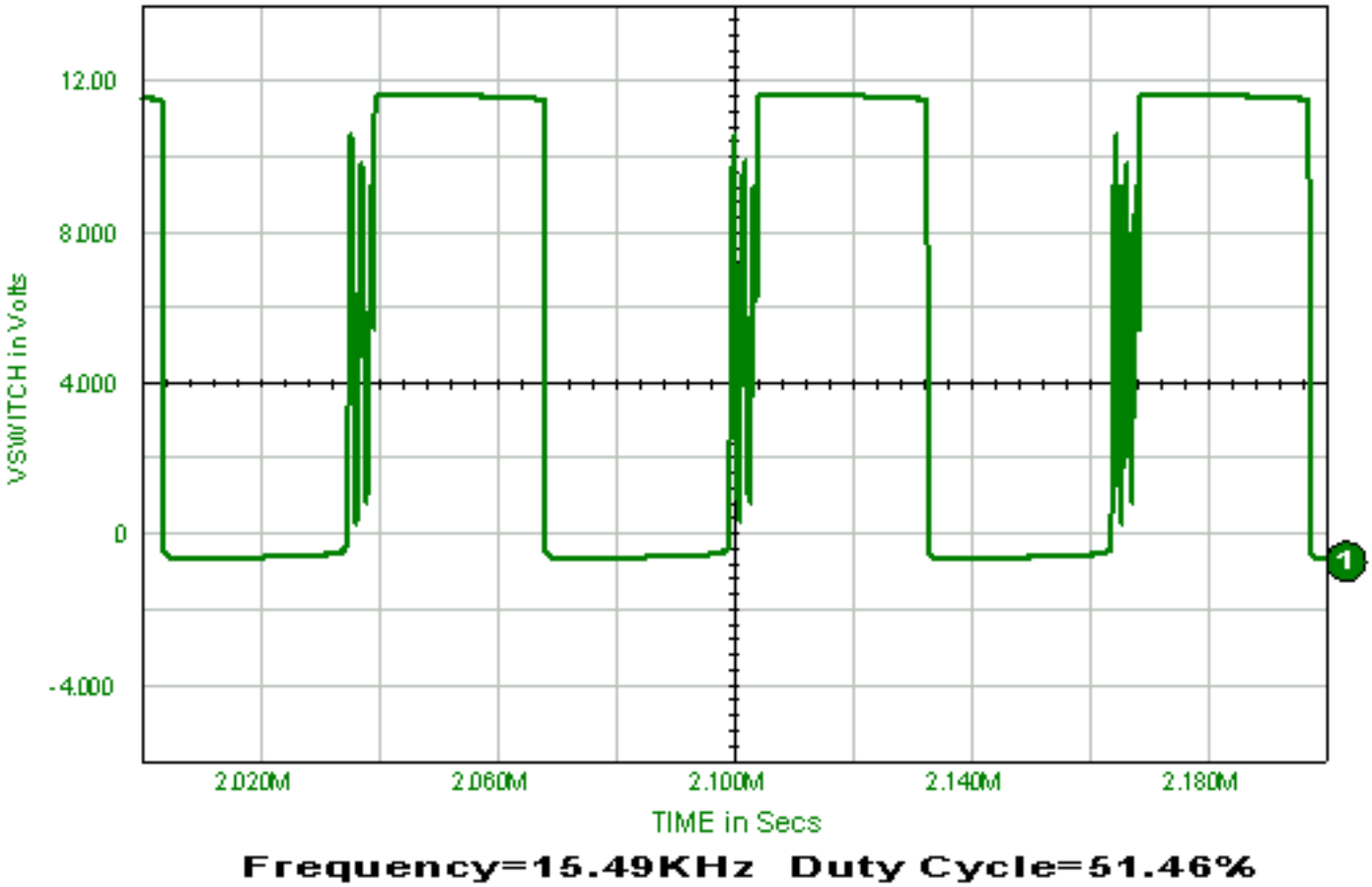

V(3)
VSWITCH
R8
219K
V1
11.64;PU
X2
TIP42
L1 362U
3
D1
DN5811
C2
10U
16
R6
20
R5 97.8
R9
.1
X1 UA723
NC
NC
CL
FRCO
5
10
CS
VCC+
6
IN-
VC
8
V(4)
4
IN+
VOUT
2
V(8)
BASE
1
VREF
NC
R1
9.9
VCC-
NC
V(10)
VOUT
R7
982
R3
2.17K
V(11)
CAP
11
C1
.1U
R4
5.58K


Tek Run: 5MS/s Sample Trig'd
Ch1 Freq
27.82kHz
Ch1 High
11.6 V
Ch1 +Duty
48.4%
Ch1 2 V
M 10µs Ch1 ∫ 10.1 V
10 Feb 1998
09:06:49

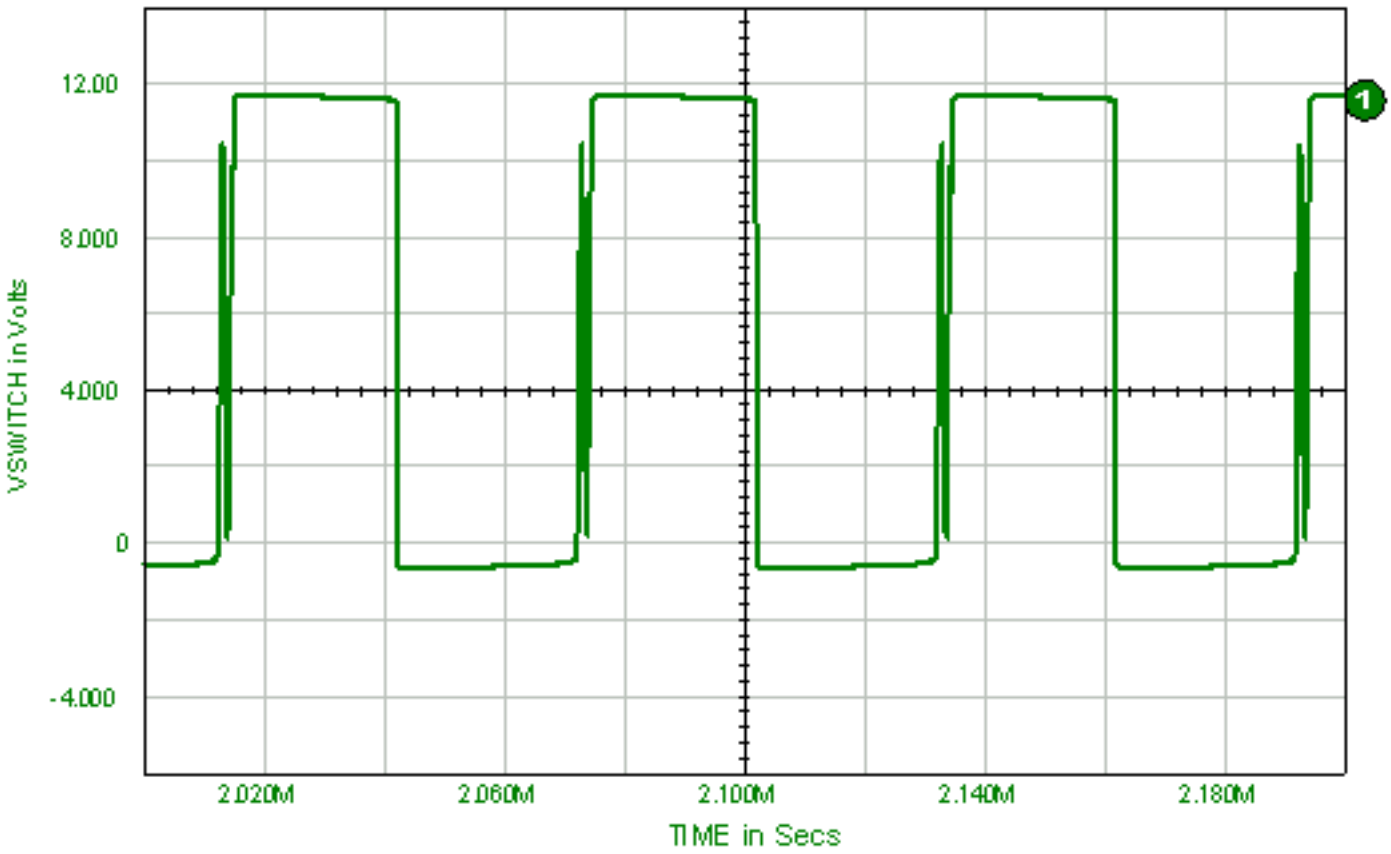

Tek Run: 5MS/s Sample Trig'd
Ch1 Pk-Pk
244mV
Ch2 Pk-Pk
30.8mV
Ch1 100mV Ch2 10mV M 10µs Ch1 46mV
10 Feb 1998
09:27:45



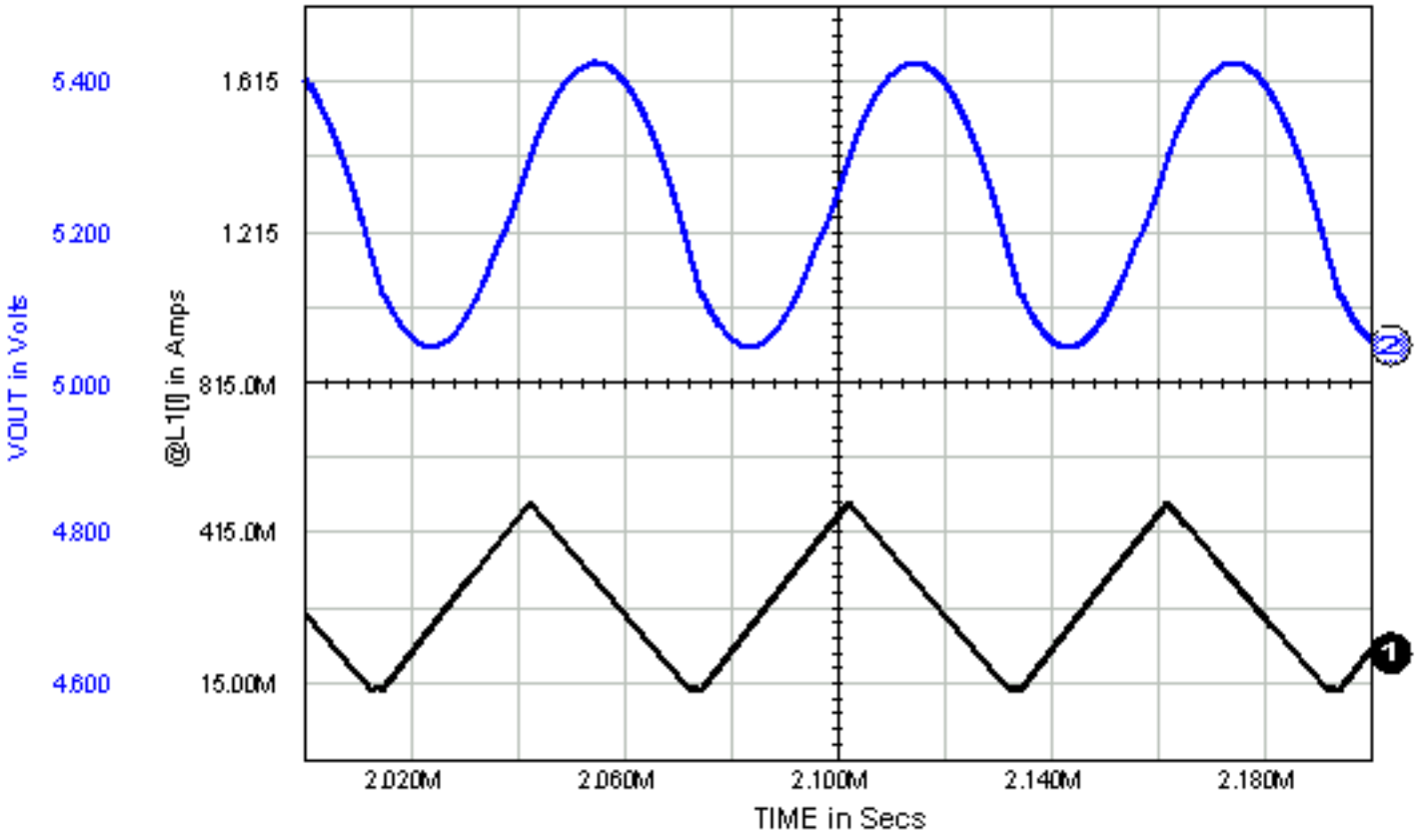
Vout=432mV pk-pk I(L1)=517.6mA pk-pk



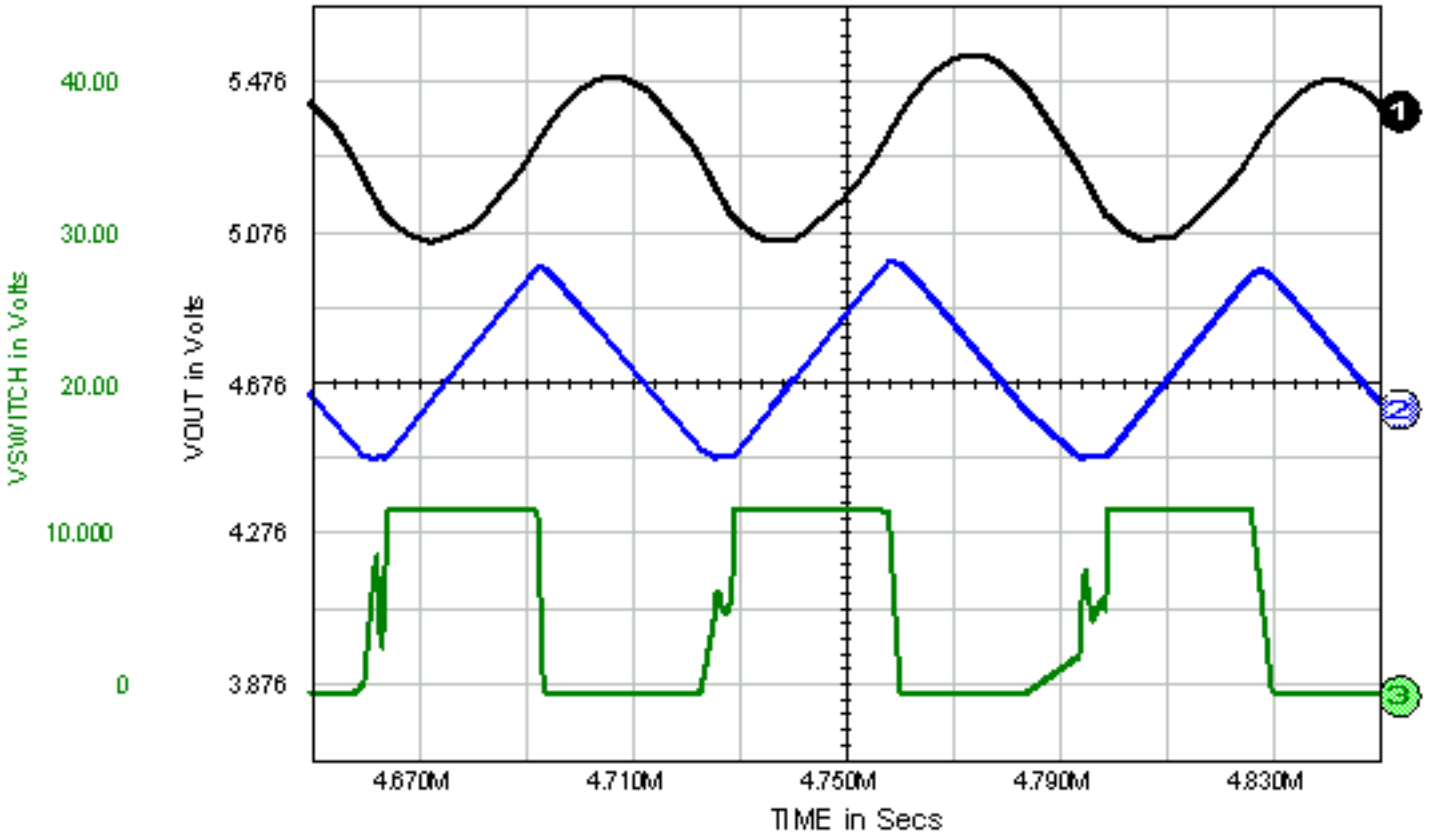
Frequency=15.49KHz Duty Cycle=51.46%

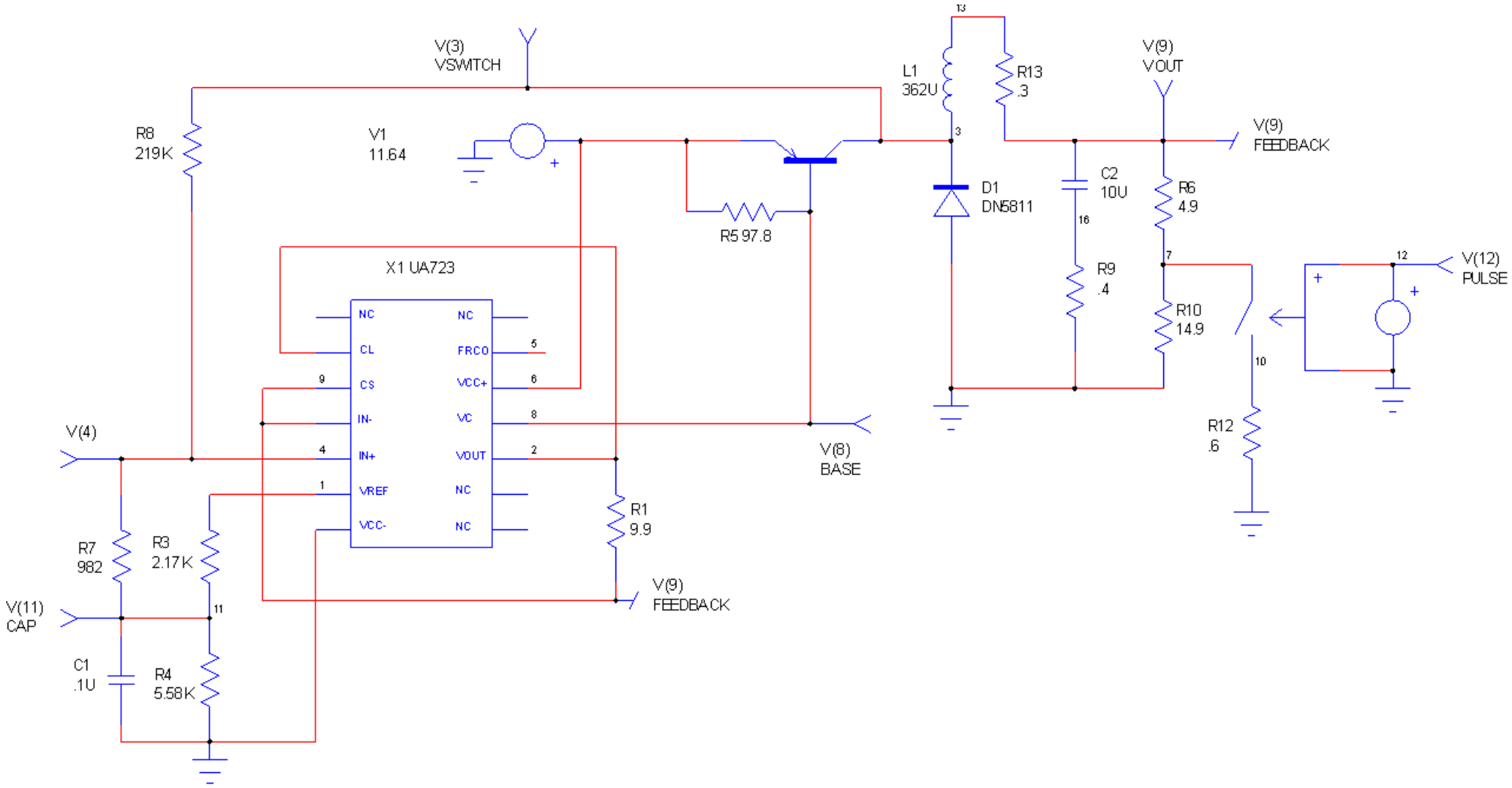


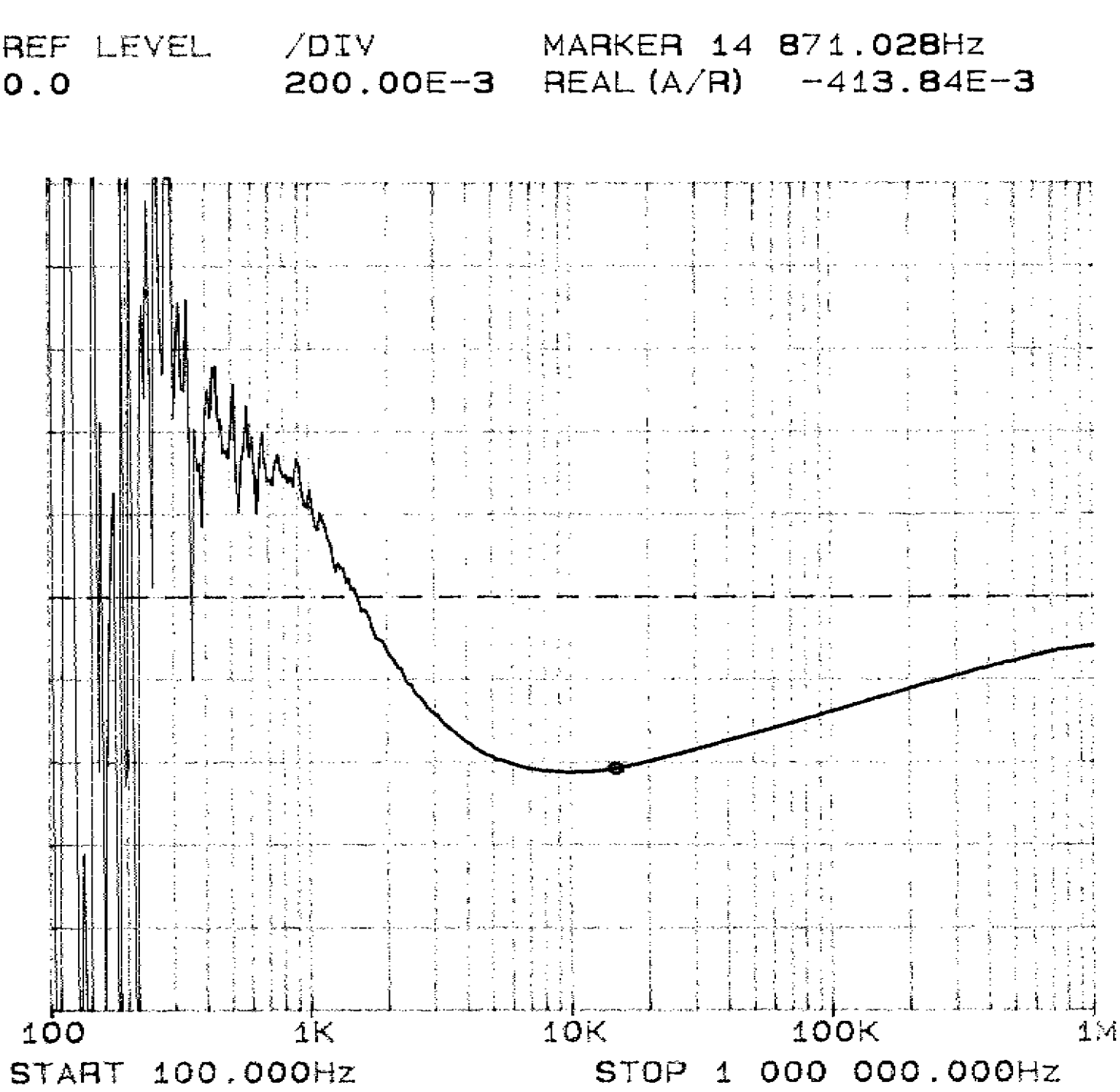
Frequency=16.72KHz Duty Cycle=46.7%

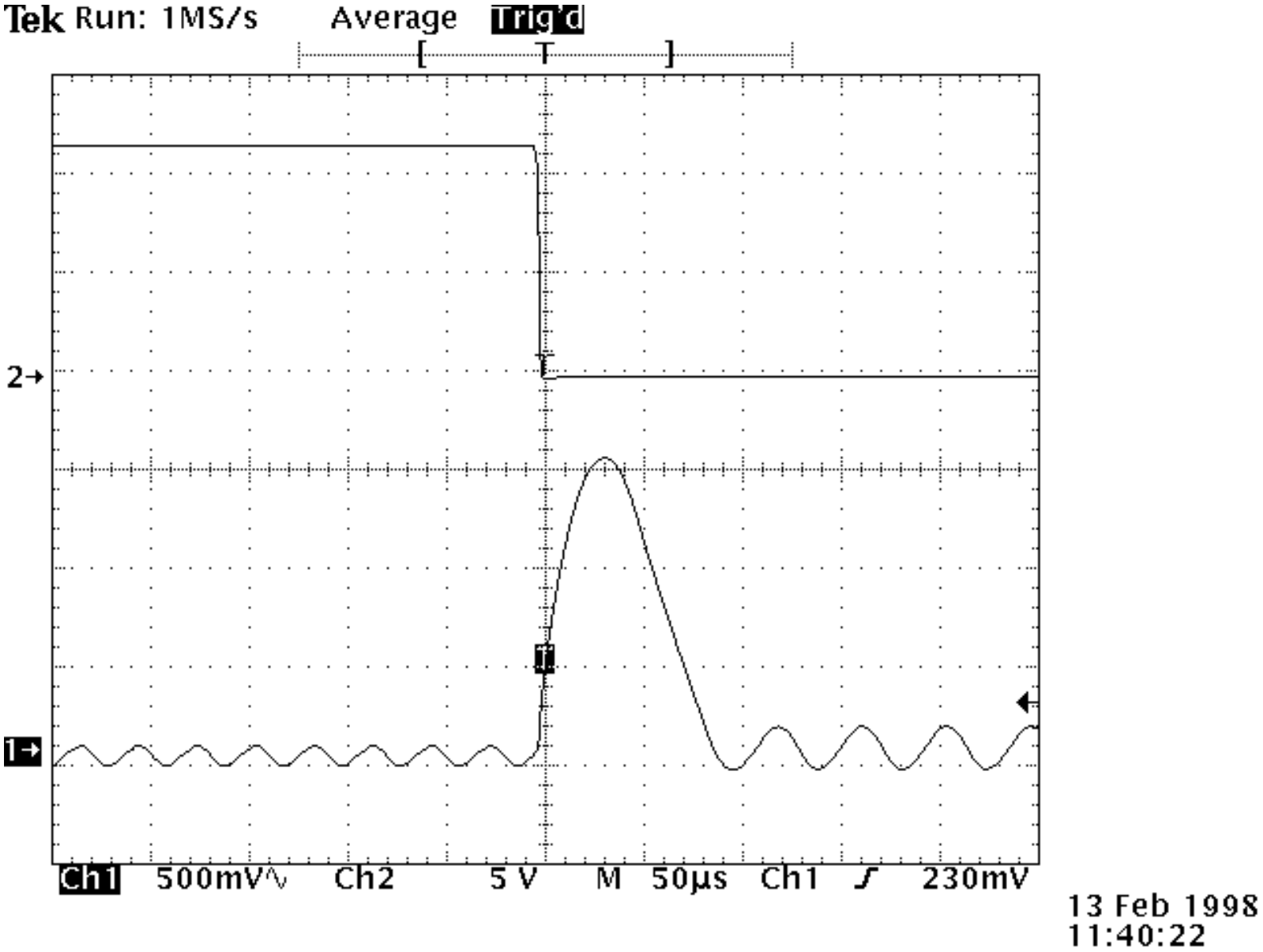


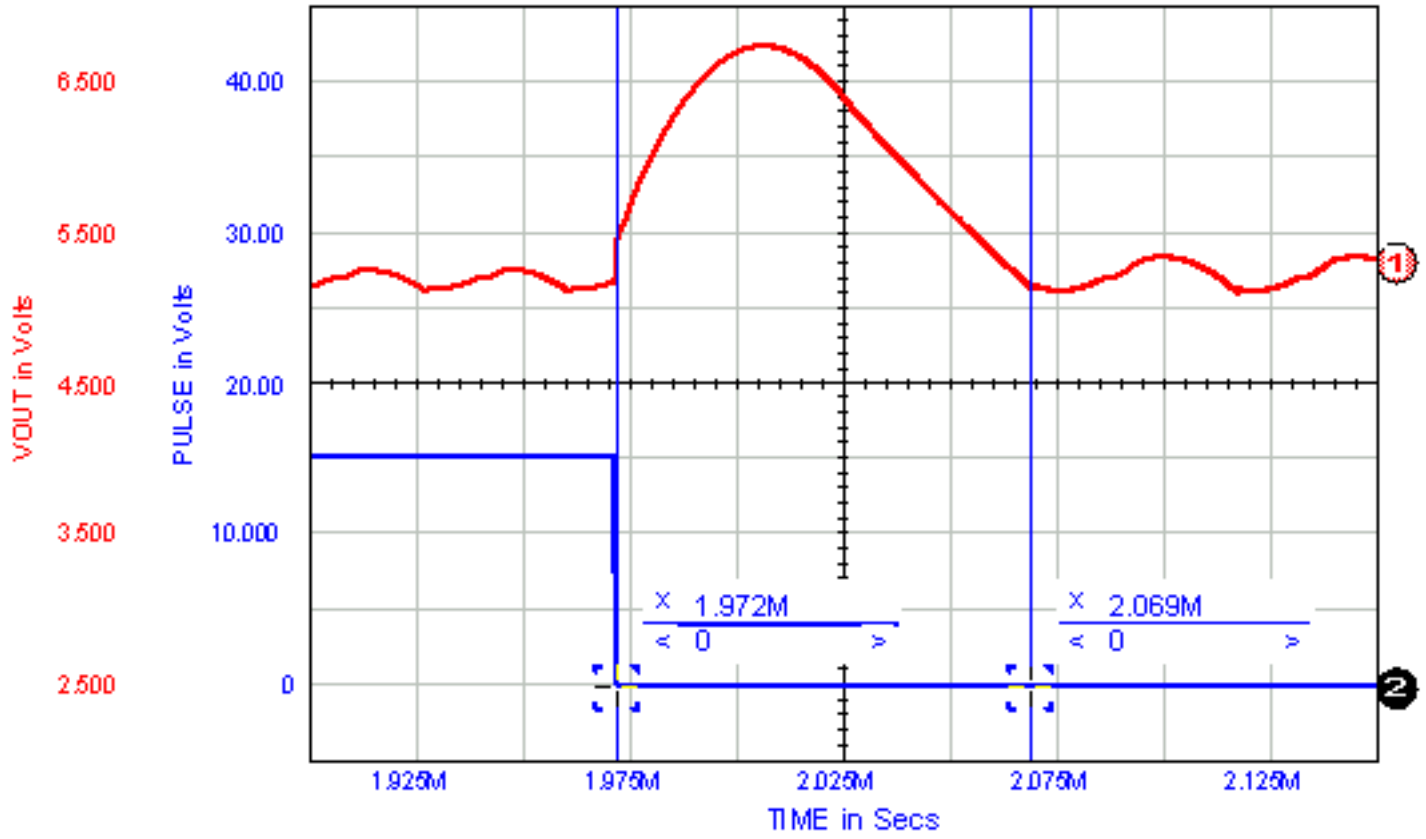
Vout=376mV pk-pk I(L1)=494.7mA pk-pk


40.00
30.00
20.00
10.000
0
VSWITCH in Volts
5.476
5.076
4.676
4.276
3.876
VOUT in Volts
4.670M
4.710M
4.750M
4.790M
4.830M
TIME in Secs
1
2
3


V(3)
VSWITCH
R8
219K
V1
11.64
L1
362U
R13
.3
V(9)
VOUT
V(9)
FEEDBACK
D1
DN5811
C2
10U
R6
4.9
R5 97.8
X1 UA723
R9
.4
R10
14.9
V(12)
PULSE
R12
.6
NC
CL
CS
IN-
IN+
VREF
VCC-
FRCO
VCC+
VC
VOUT
V(4)
V(8)
BASE
R1
9.9
R7
982
R3
2.17K
V(11)
CAP
C1
.1U
R4
5.58K
V(9)
FEEDBACK

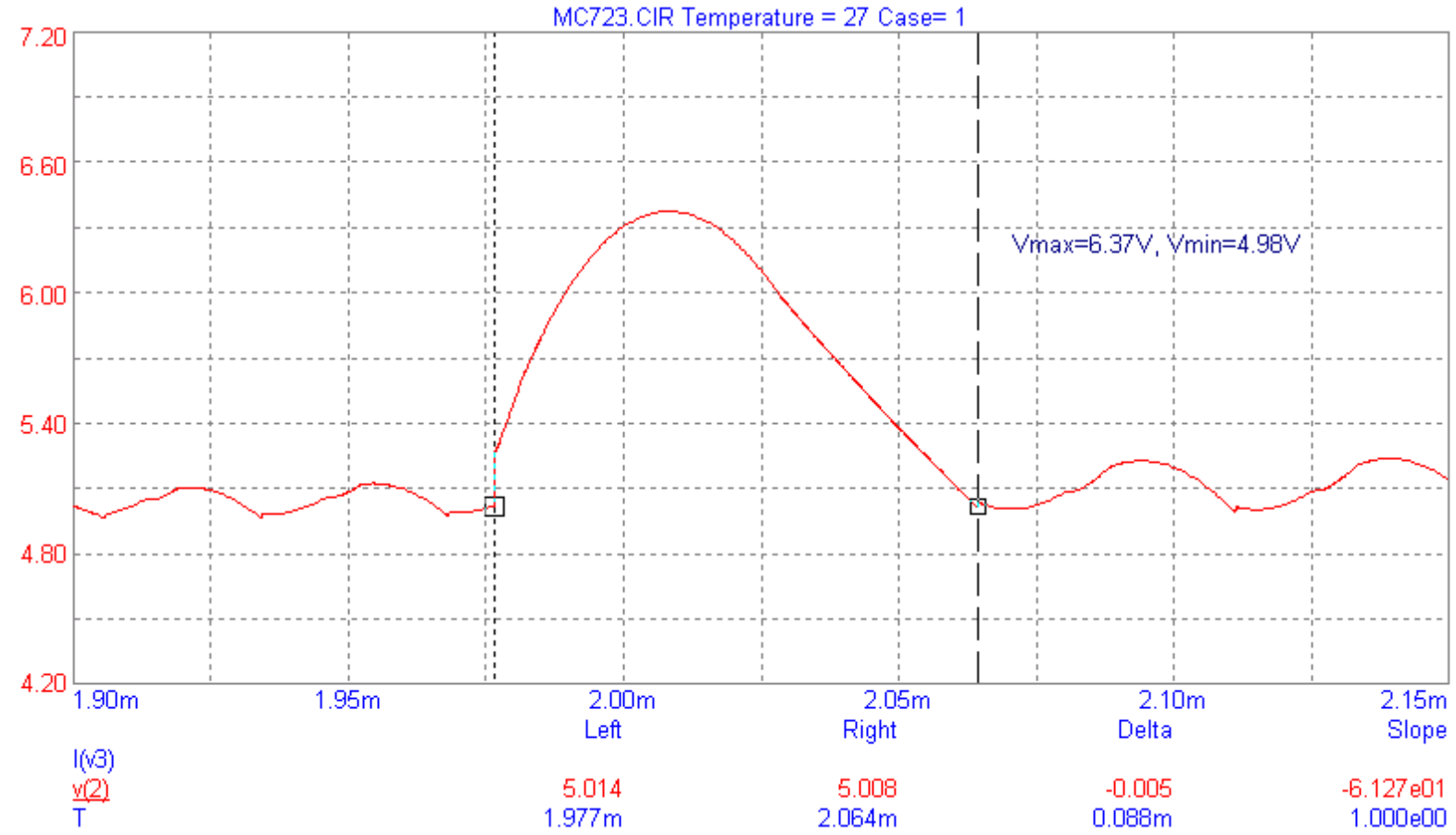


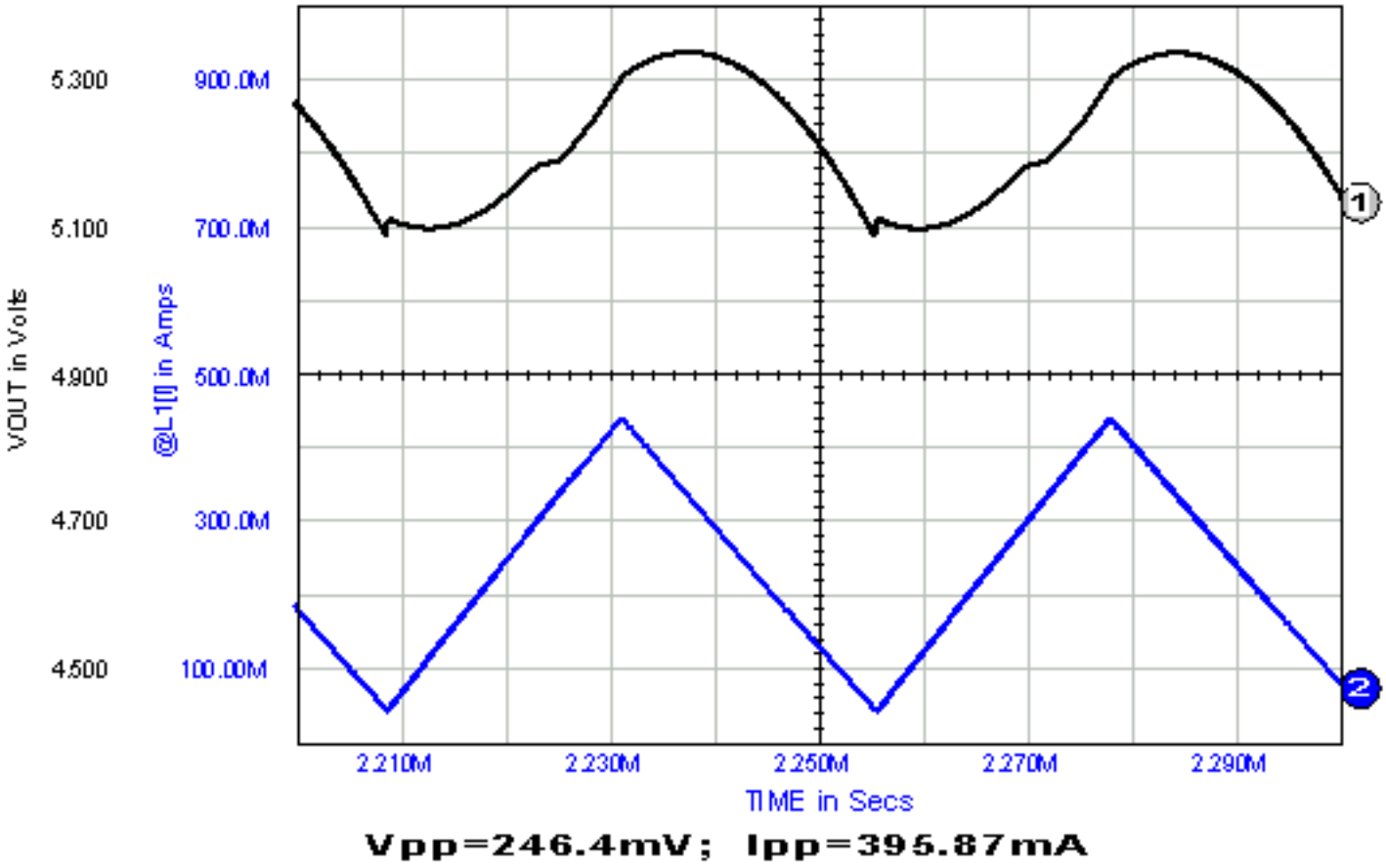

Tek Run: 1MS/s Average Trig'd
2→
1→
Ch1 500mV Ch2 5 V M 50µs Ch1 ƒ 230mV
13 Feb 1998
11:40:22



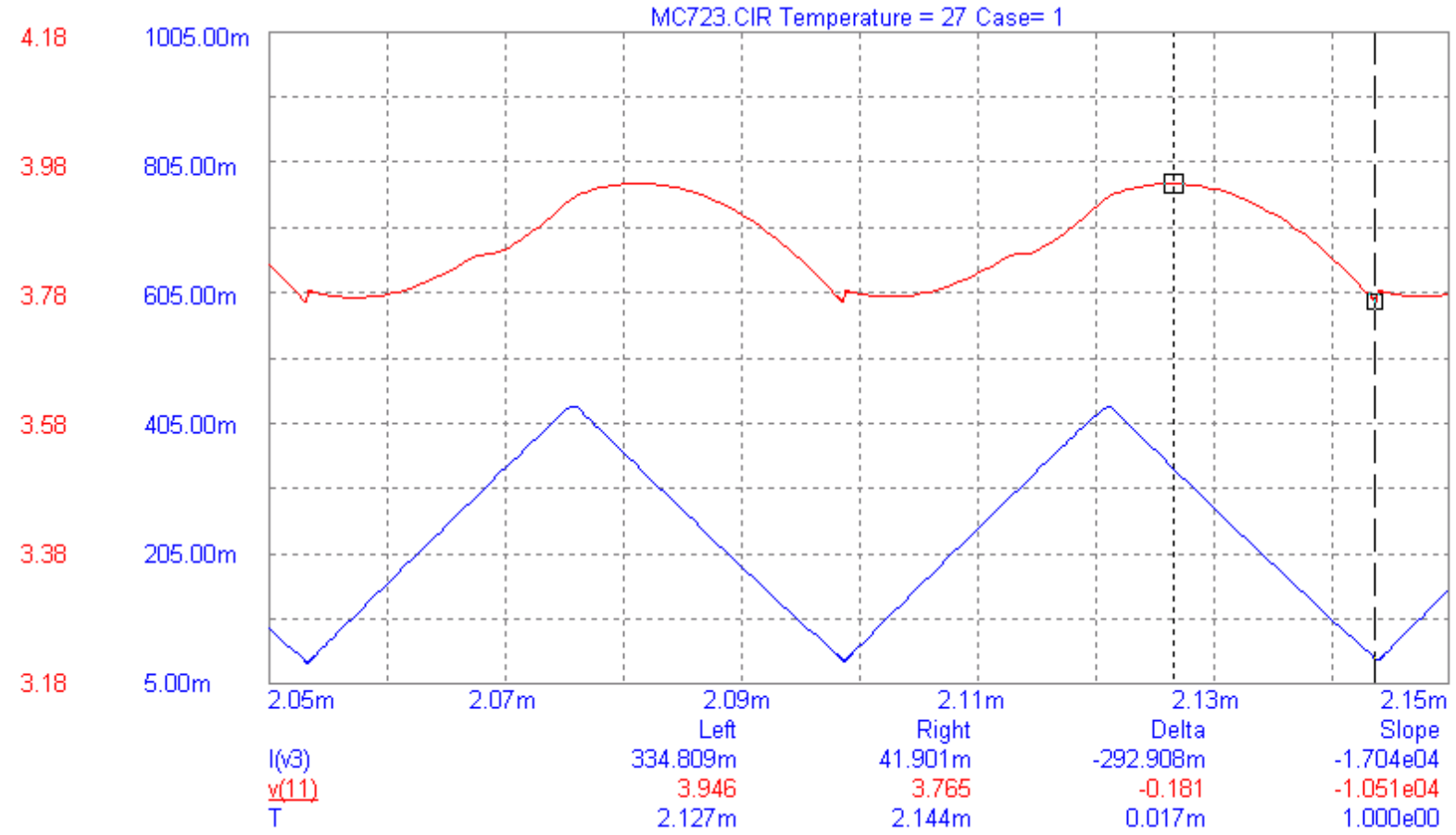
Vmax=6.716V, Vmin=5.087V

Δx = 96.90U Δy = 0


MC723.CIR Temperature = 27 Case= 1
7.20
6.60
6.00
5.40
4.80
4.20
Vmax=6.37V, Vmin=4.98V
1.90m
1.95m
2.00m
2.05m
2.10m
2.15m
Left
Right
Delta
Slope
I(v3)
v(2)
5.014
5.008
-0.005
-6.127e01
T
1.977m
2.064m
0.088m
1.000e00



Vpp=246.4mV; Ipp=395.87mA


MC723.CIR Temperature = 27 Case= 1
4.18
3.98
3.78
3.58
3.38
3.18
1005.00m
805.00m
605.00m
405.00m
205.00m
5.00m
2.05m
2.07m
2.09m
2.11m
2.13m
2.15m
Left
Right
Delta
Slope
I(v3) 334.809m 41.901m -292.908m -1.704e04
v(11) 3.946 3.765 -0.181 -1.051e04
T 2.127m 2.144m 0.017m 1.000e00

#15: Low Drop Out Regulator

Multiple output power converters may not provide regulation that is good enough to meet the requirements of every output. The regulation of a single output of the converter may require some type of post regulation to meet the regulation requirements of that output. In many applications a simple three terminal regulator may be used. However, some applications may be sensitive to efficiency. In these applications the use of a low drop out linear regulator, which is shown in Figure 15-1, may be used to meet the specific regulation requirements of a particular output.

This circuit utilizes a Mosfet as a source follower. The Mosfet is controlled by a TL431 shunt regulator integrated circuit. The Mosfet reduces the minimum input-to-output differential or headroom of 1.5V to 2V of a typical three terminal regulator, down to the product of the output current and the ON resistance on the Mosfet. The lower the on resistance of the Mosfet used in the circuit, the lower the headroom of the regulator. This circuit requires a bias voltage for the Mosfet gate, which must be several volts greater than the output voltage. If a large enough voltage is not available in the power convert, then a CMOS charge pump can be used to generate it.

The dominant pole is created by the source impedance of the Mosfet, and the output capacitor. A second pole is created by the Mosfet's Ciss and its driving impedance. Therefore, the Mosfet is the major contributor to the accuracy of the phase and gain margin measurements. A zero is contributed by the compensation of the TL431, R2 and C1, which has a corner frequency of approximately 12.8KHz.

In order measure the control loop stability of the regulator, a simple modification to the circuit was made. L1 and C3 were added to the circuit to effectively open the control loop of the regulator. This allows AC phase and gain measurements to be made. A simple ICL script can be implemented to reduce the computations that must be made in the post processor. The ESR of capacitor C2 is shown in Figure 15-2. The simulated and measured results are shown in Figure 15-3 through Figure 15-8.

```
.CONTROL

SAVE ALL

ALIAS GAIN VDB(9)

ALIAS PHASE VP(9)
```

```
AC DEC 40 100 1MEG

PRINT GAIN PHASE

.ENDC

.PRINT AC GAIN PHASE
```

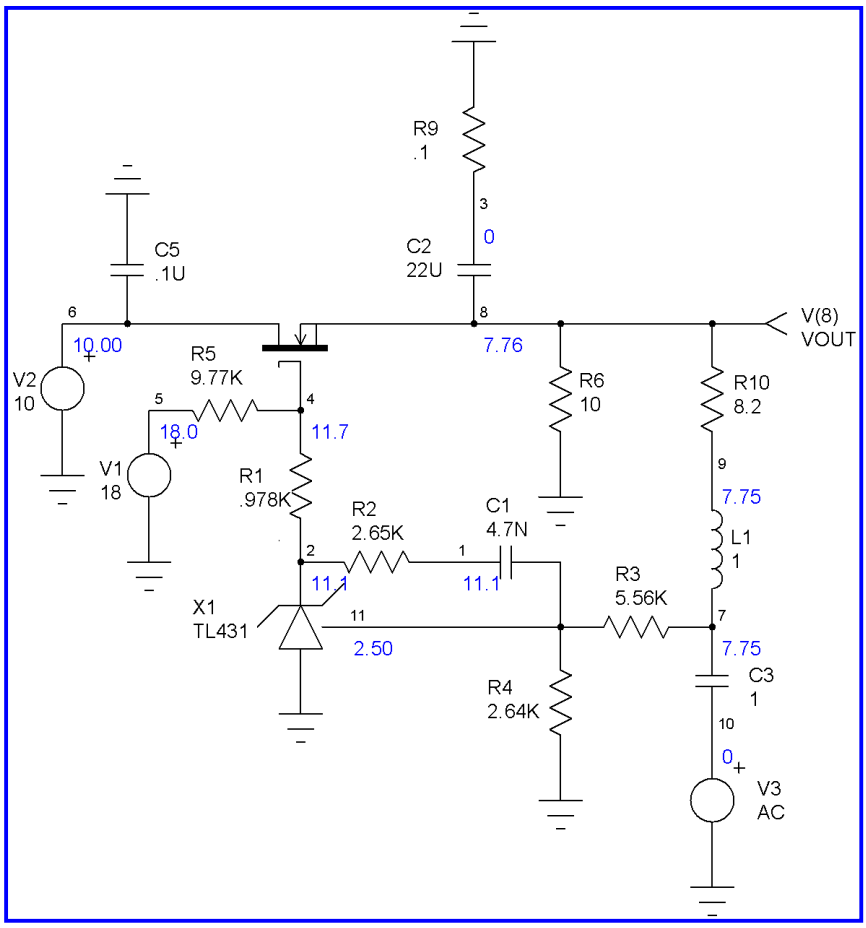


Figure 15-1: TL431 Low Drop Out Linear Regulator Circuit

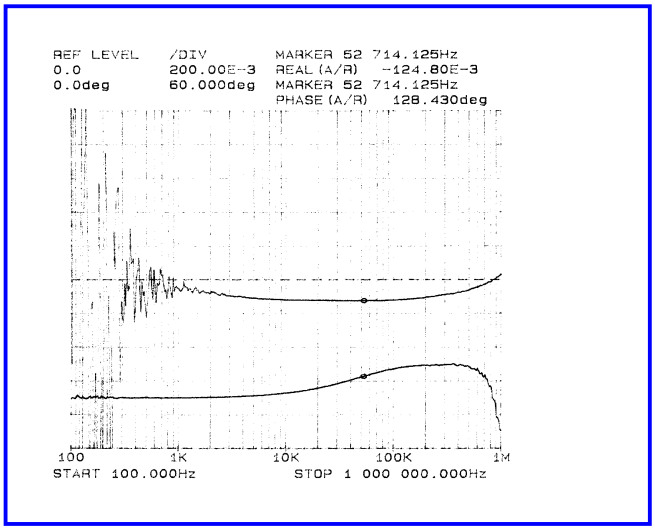


Figure 15-2: 22uF (TDC226K050WSG) ESR

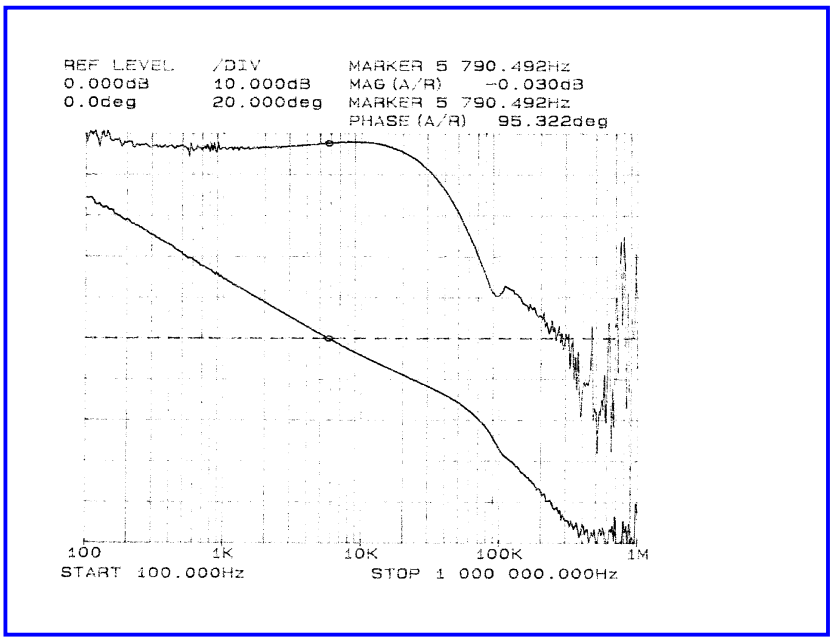


Figure 15-3: Measured Low Drop Out Regulator Phase and Gain Margins

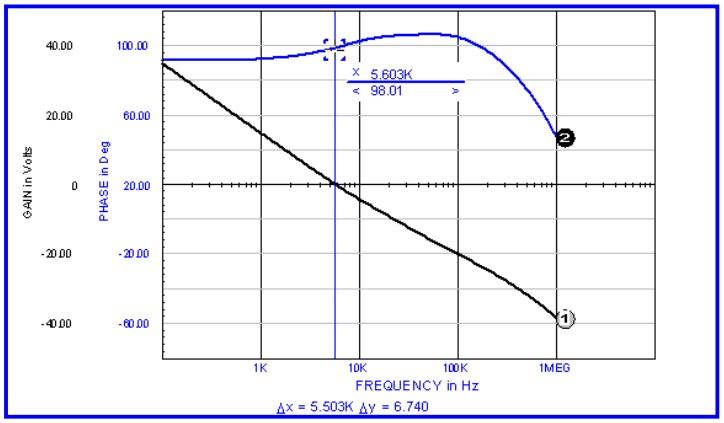


Figure 15-4: Simulated Low Drop Out Regulator Phase and Gain Margins

Note: Poor Phase margin correlation. Role off occurs at100KHz, rather than 10KHz.

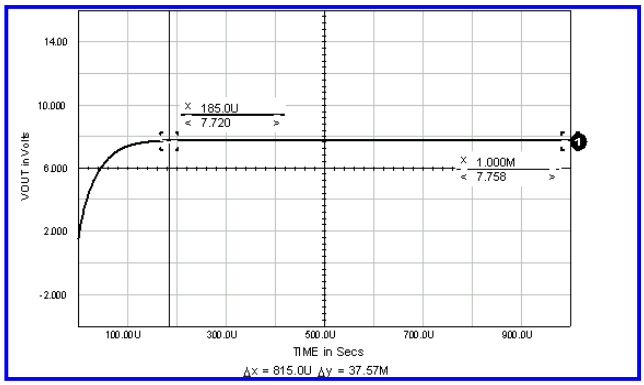


Figure 15-5: Simulated Low Drop Out Regulator Turn On

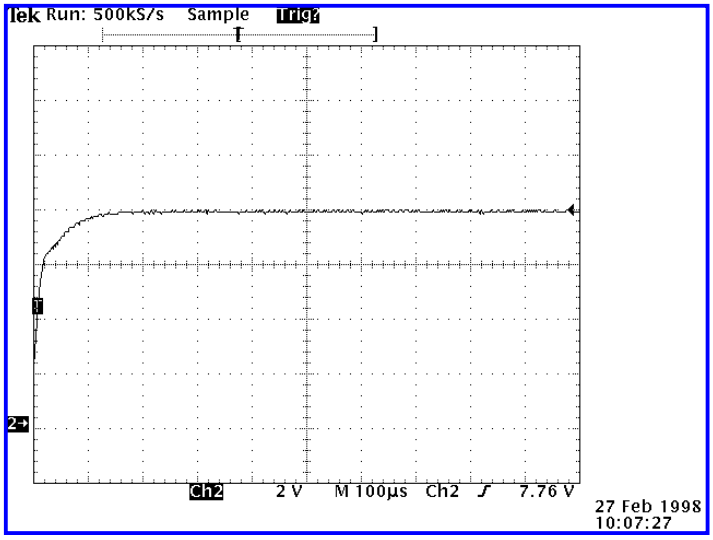


Figure 15-6: Measured Low Drop Out Regulator Turn On

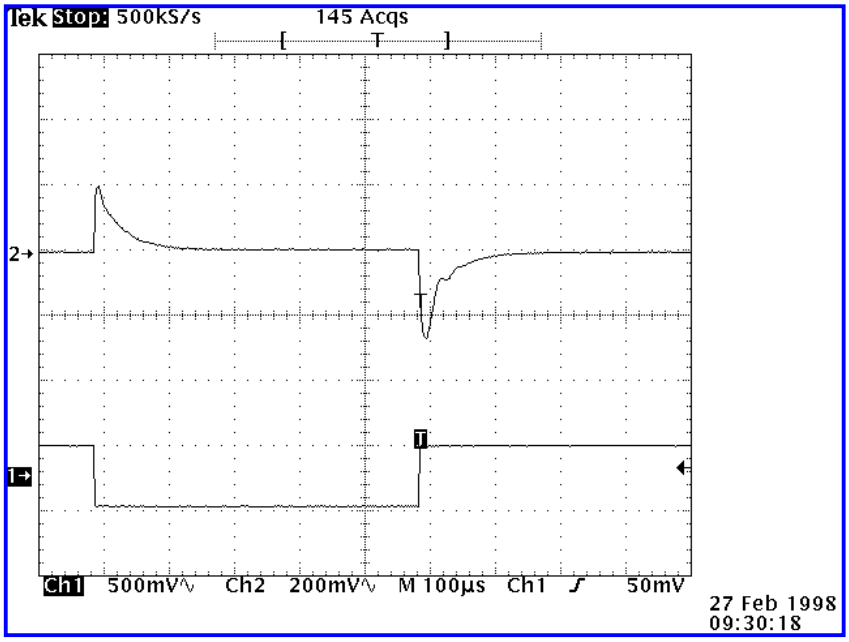


Figure 15-7: Measured Low Drop Out Regulator Transient Response

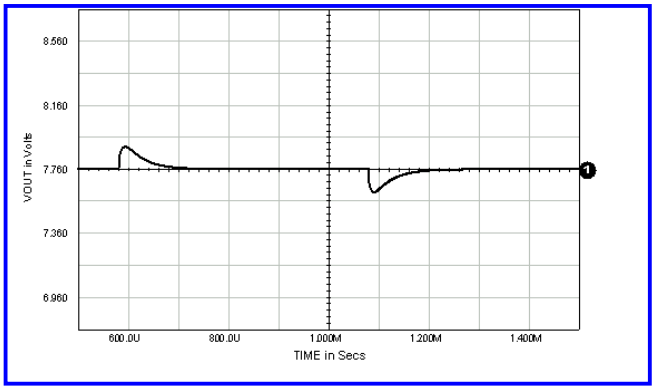


Figure 15-8: Simulateded Low Drop Out Regulator Transient Response

The poor correlation of the phase and gain margins can be addressed and corrected. The major player in the phase and gain margins is the Mosfet. The Mosfet used in the hardware, is a IRF641, which is not available in the Ispice libraries. To select a Mosfet which is an appropriate match, the data sheet needs to be evaluated as well as correlation to the phase and gain margins of the regulator. Because the dominant poles are determined by the characteristics of the Mosfet model, selection of a substitute model requires verification of the phase and gain characteristics dictated by the use of a particular model. Mosfets can be difficult to model, and they are notorious for being inaccurate. Rather that building a Mosfet model of the IRF641, an alternate solution was chosen to obtain correlation to the TL431 regulator circuit. To correlate to this model, the correct capacitance of the mosfet needs to be accounted for. This can be achieved by manipulating the values of the output filter capacitor to values which create the proper phase and gain margins. The modified schematic of this model is shown below in Figure 15-9. The measured and simulated results are shown in Figure 15-10 through Figure 15-15.

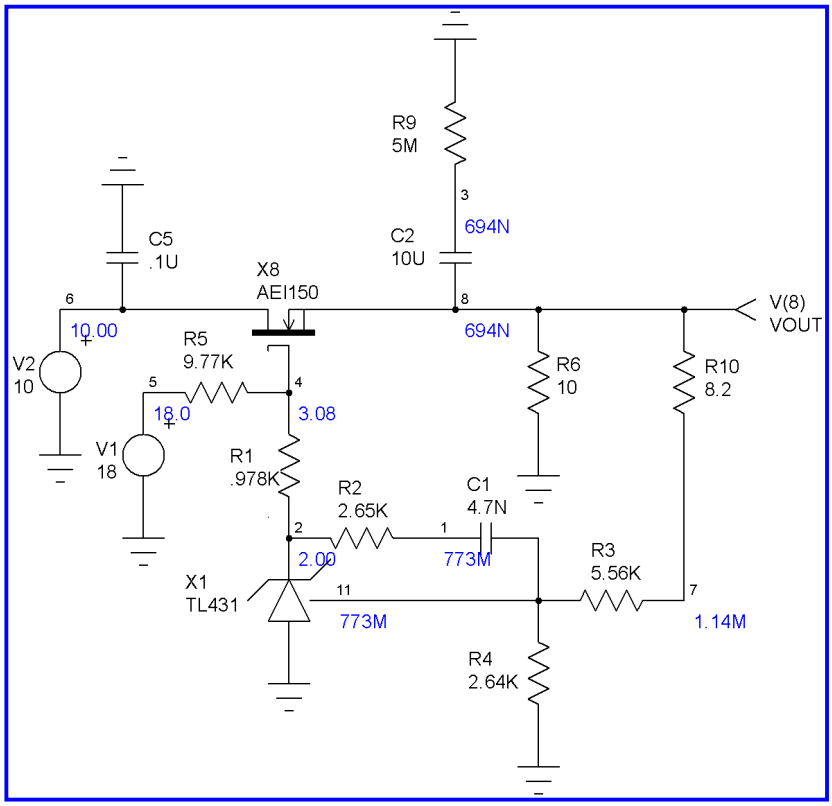


Figure 15-9: TL431 Modified Low Drop Out Linear Regulator Circuit

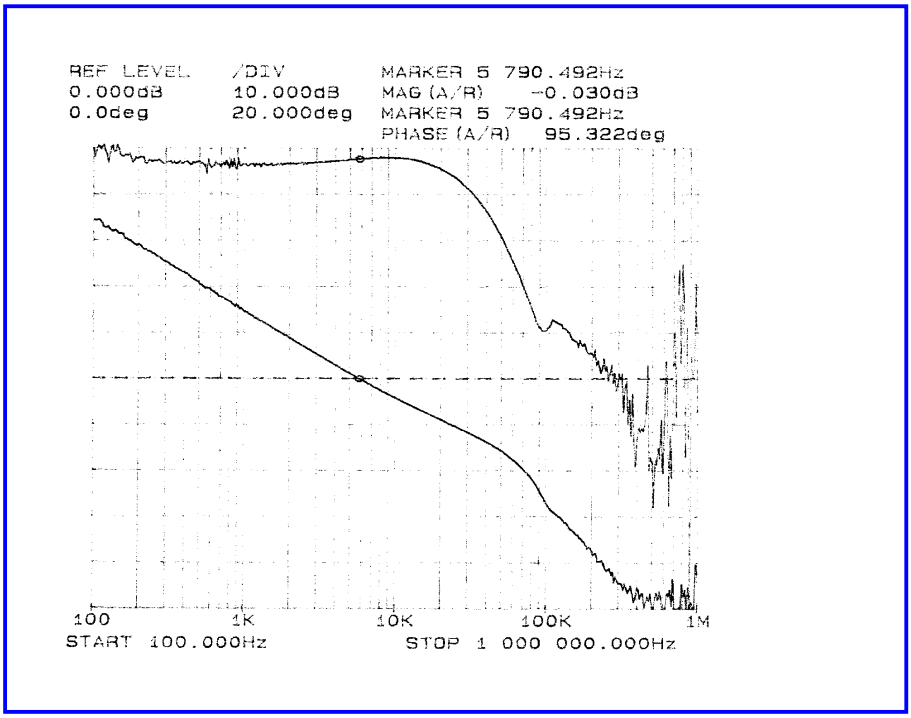


Figure 15-10: Measured Modified Low Drop Out Regulator Phase and Gain Margins

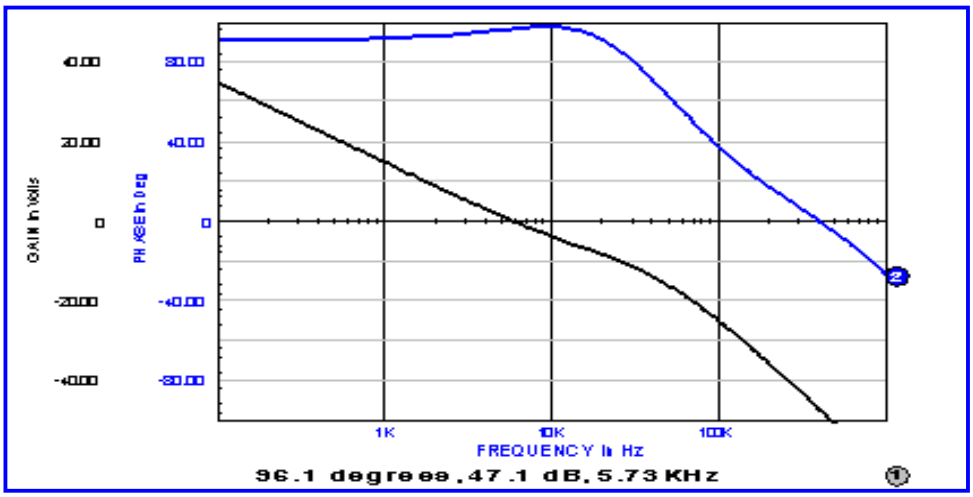


Figure 15-11: Measured Modified Low Drop Out Regulator Phase and Gain Margins

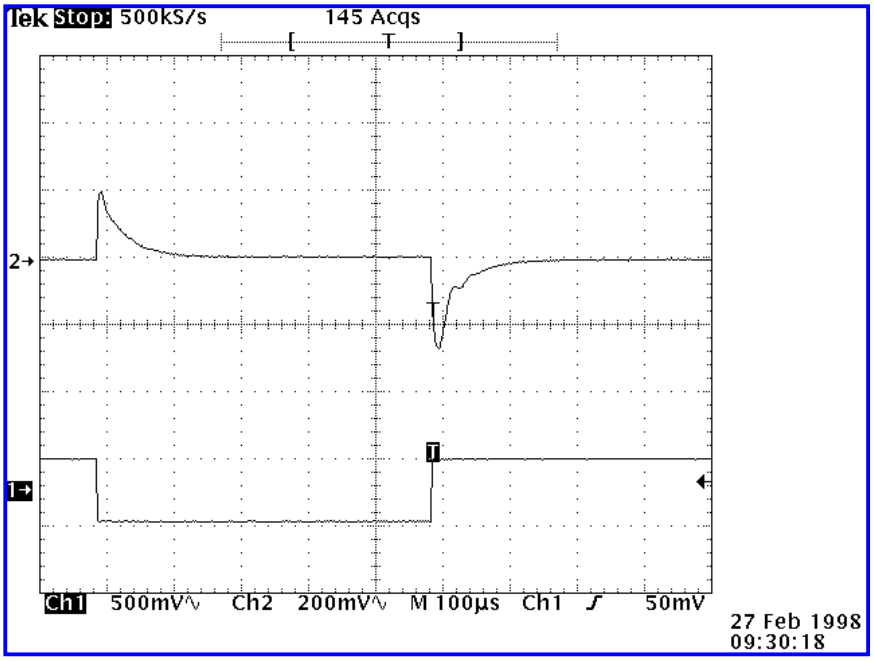


Figure 15-12: Measured Modified Low Drop Out Regulator Transient Response

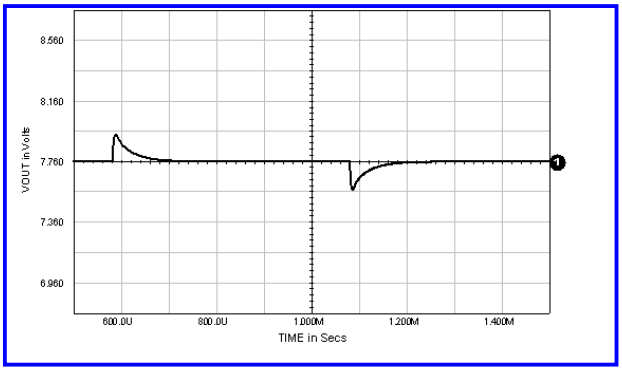


Figure 15-13: Simulated Modified Low Drop Out Regulator Transient Response

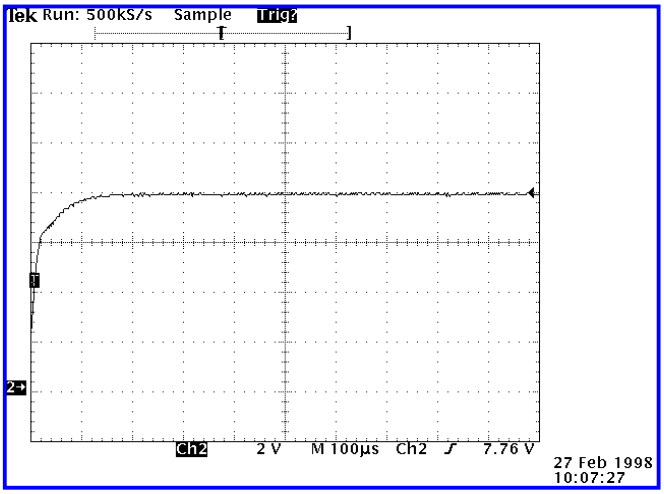


Figure 15-14: Measured Modified Low Drop Out Regulator Turn On

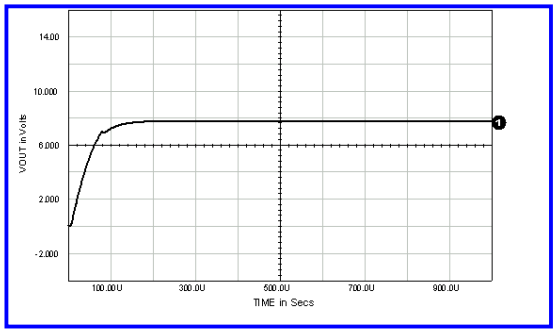
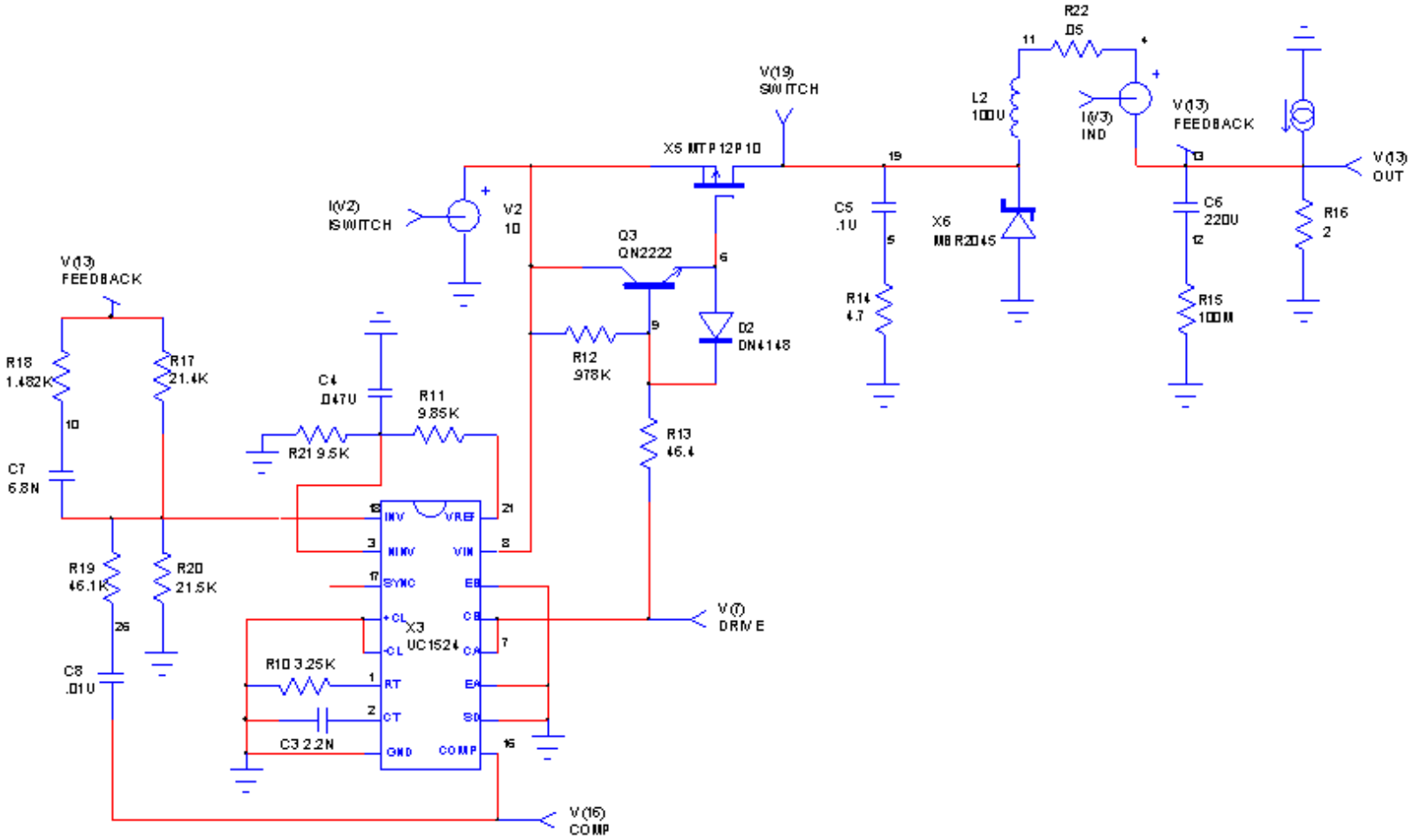
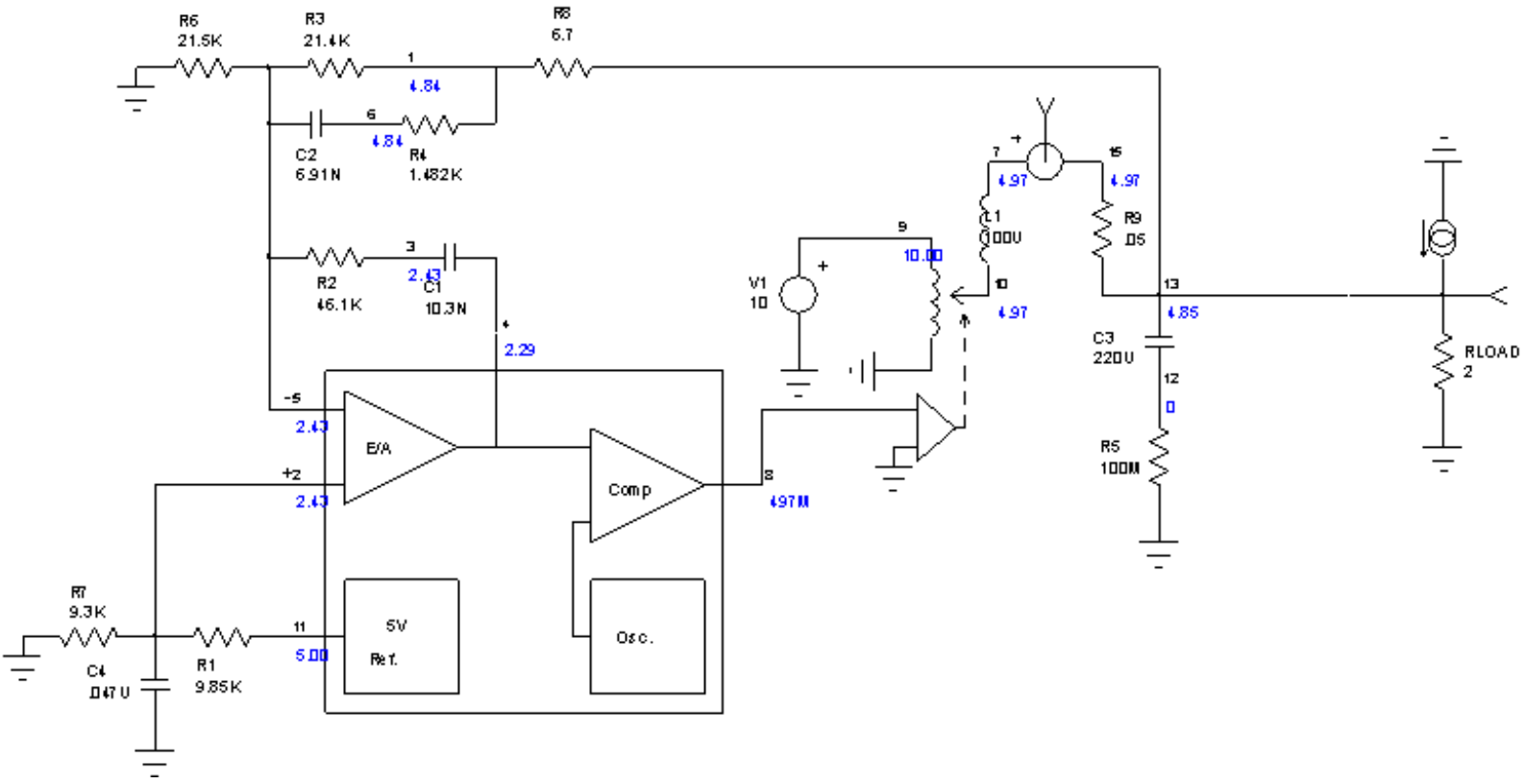
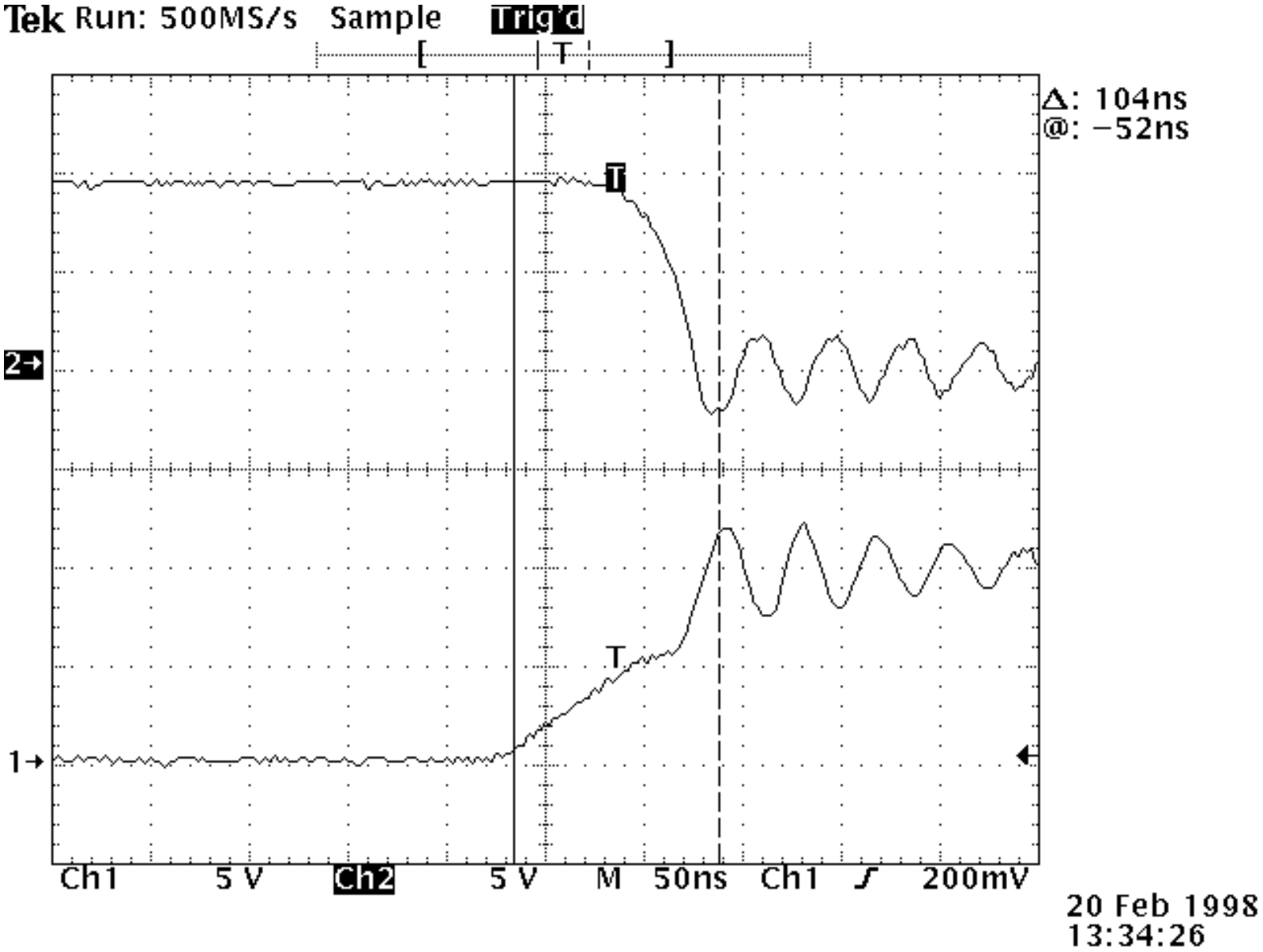
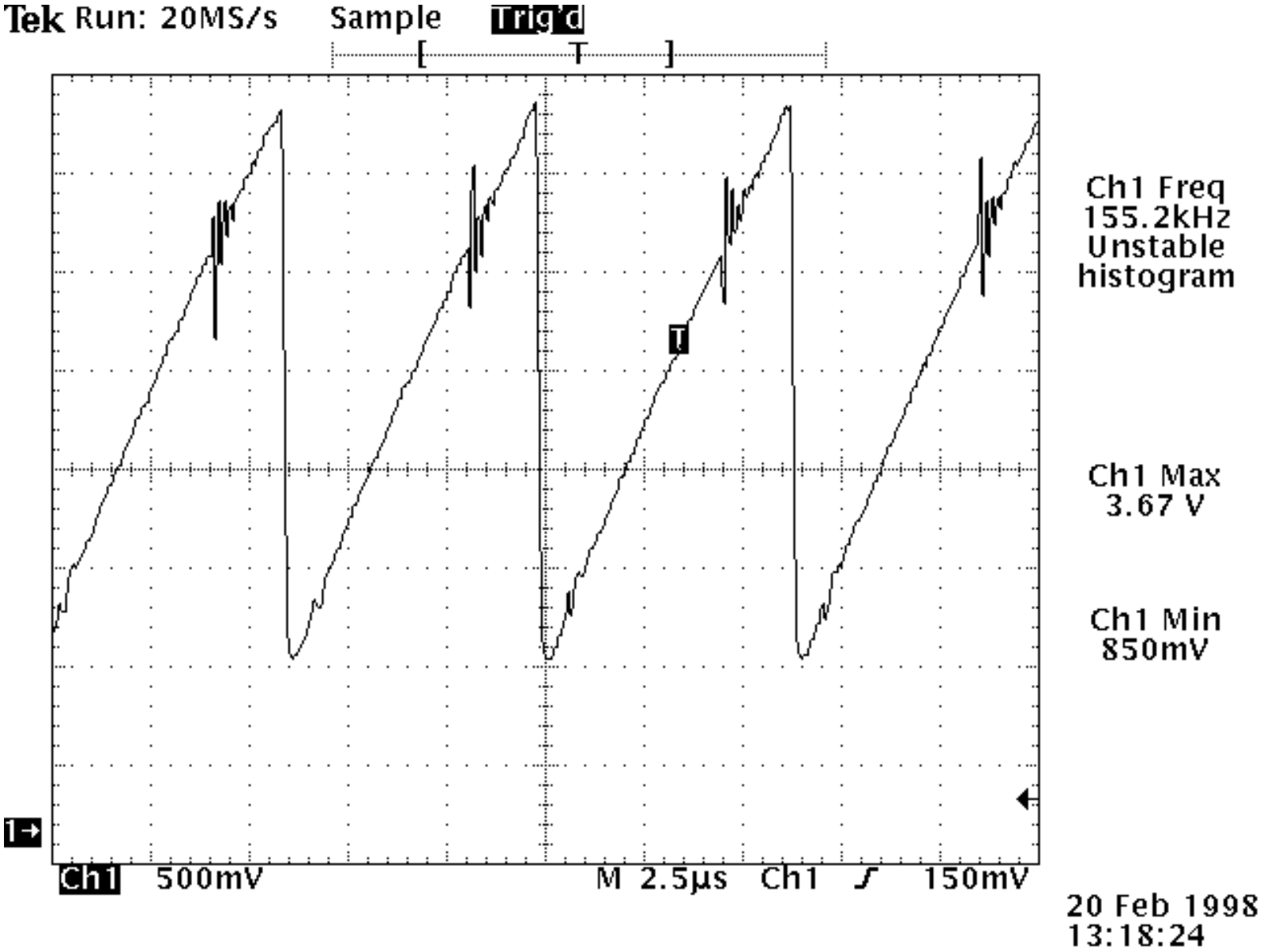


Figure 15-15: Simulated Modified Low Drop Out Regulator Turn On


R22
.05
11
4
V(19)
SWITCH
L2
100U
I(V3)
IND
V(13)
FEEDBACK
V(13)
OUT
X5 MTP12P10
19
I(V2)
ISWITCH
V2
10
C5
.1U
X6
MBR2045
C6
220U
R16
2
Q3
QN2222
6
V(13)
FEEDBACK
R18
1.482K
R17
21.4K
10
C4
.047U
R11
9.85K
R12
978K
D2
DN4148
R14
4.7
5
12
R15
100M
R21 9.5K
R13
46.4
C7
6.8N
INV
VREF
21
NINV
VIN
8
R19
46.1K
R20
21.5K
SYNC
EB
CL
X3
UC1524
CB
7
26
C8
.01U
CL
CA
R10 3.25K
RT
EA
2
CT
SD
C3 2.2N
GND
COMP
16
V(7)
DRIVE
V(16)
COMP


R6
21.5K
R3
21.4K
R8
6.7
1
4.84
6
4.84
C2
6.91N
R4
1.482K
3
2.43
R2
46.1K
C1
10.3N
4
2.29
-5
2.43
+2
2.43
E/A
Comp
8
497M
R7
9.3K
C4
.047U
R1
9.85K
11
5.00
5V
Ref.
Osc.
V1
10
9
10.00
7
4.97
15
4.97
L1
100U
R9
.05
10
4.97
13
4.85
C3
220U
12
0
R5
100M
RLOAD
2


Tek Run: 500MS/s Sample Trig'd
Δ: 104ns
@: −52ns
2→
1→
Ch1 5 V Ch2 5 V M 50ns Ch1 ƒ 200mV
20 Feb 1998
13:34:26


Tek Run: 20MS/s Sample Trig'd
Ch1 Freq
155.2kHz
Unstable
histogram
Ch1 Max
3.67 V
Ch1 Min
850mV
Ch1 500mV
M 2.5µs Ch1 ƒ 150mV
20 Feb 1998
13:18:24

$$L_2 := 100\,10^{-6}$$

$$C_6 := 220\,10^{-6}$$

$$F_1 := \frac{1}{2 \cdot \pi \cdot \sqrt{L_2 \cdot C_6}}$$

$$F_1 = 1.07310^3$$

R_{17}:=2140(

$$C_7 := 6.8 \cdot 10^{9}$$

$$F_2 := \frac{1}{2 \cdot \pi \cdot R_{17} C_7}$$

$$F_2 = 1.09410^3$$

R_{19}:=4610(

$C_8 := .011 \cdot 10^{-6}$

$$F_3 := \frac{1}{2 \cdot \pi \cdot R_{19} C_8}$$

$$F_3 = 345.238$$

$$R_{15} := 100\,10^{3}$$

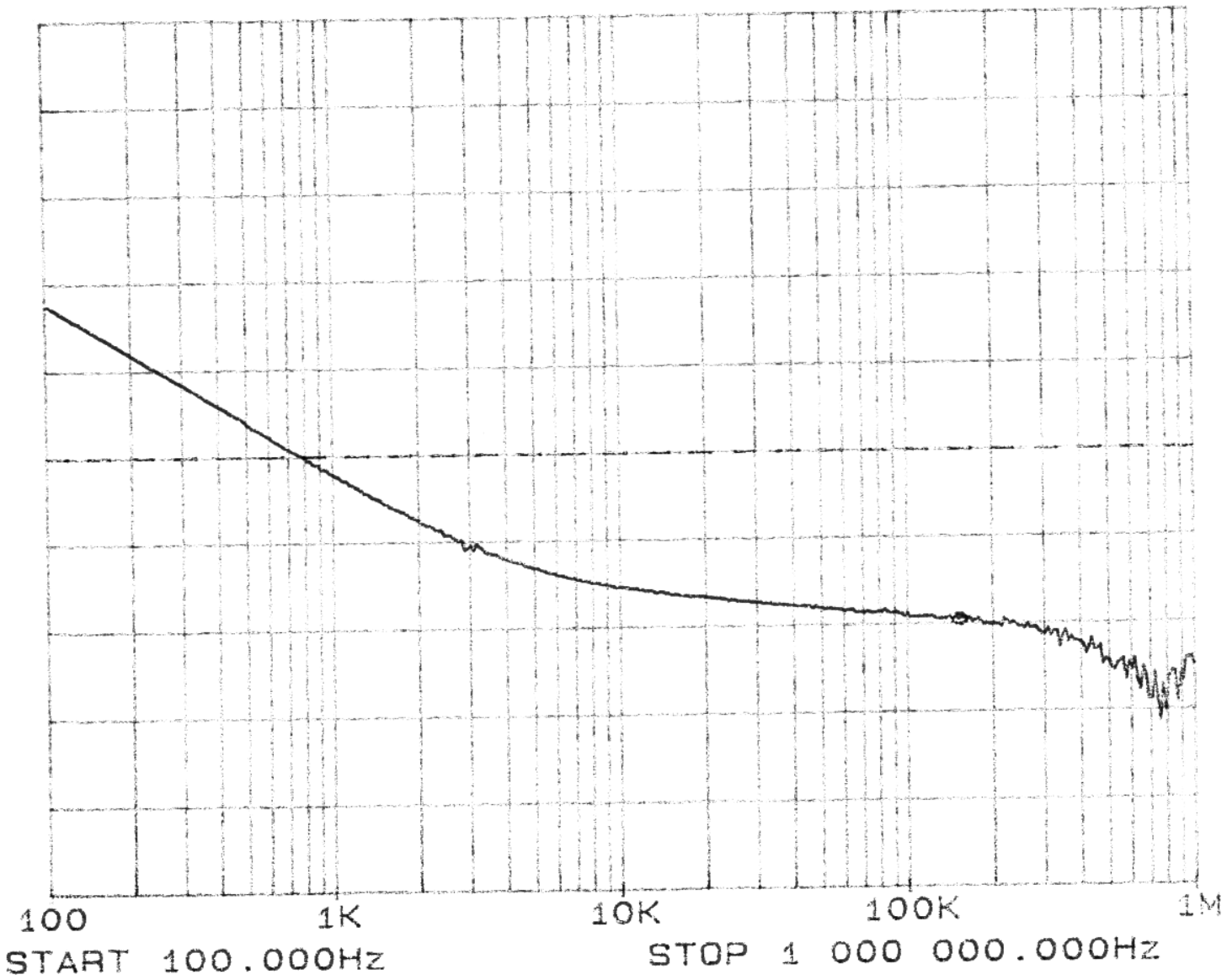
$$F_4 = \frac{1}{2 \cdot \pi \cdot R_{15} C_6}$$

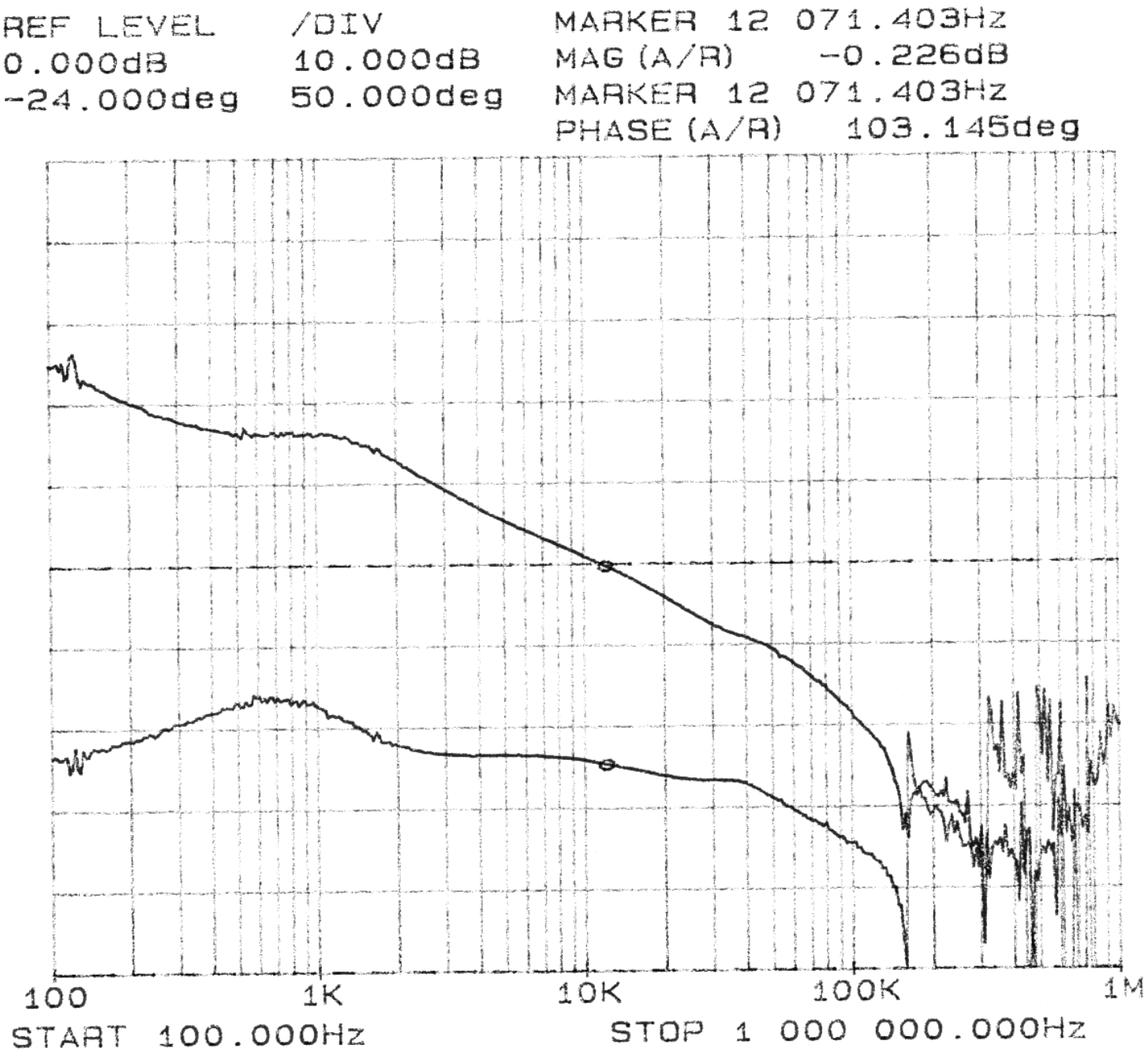
$$F_4 = 7.23410^3$$

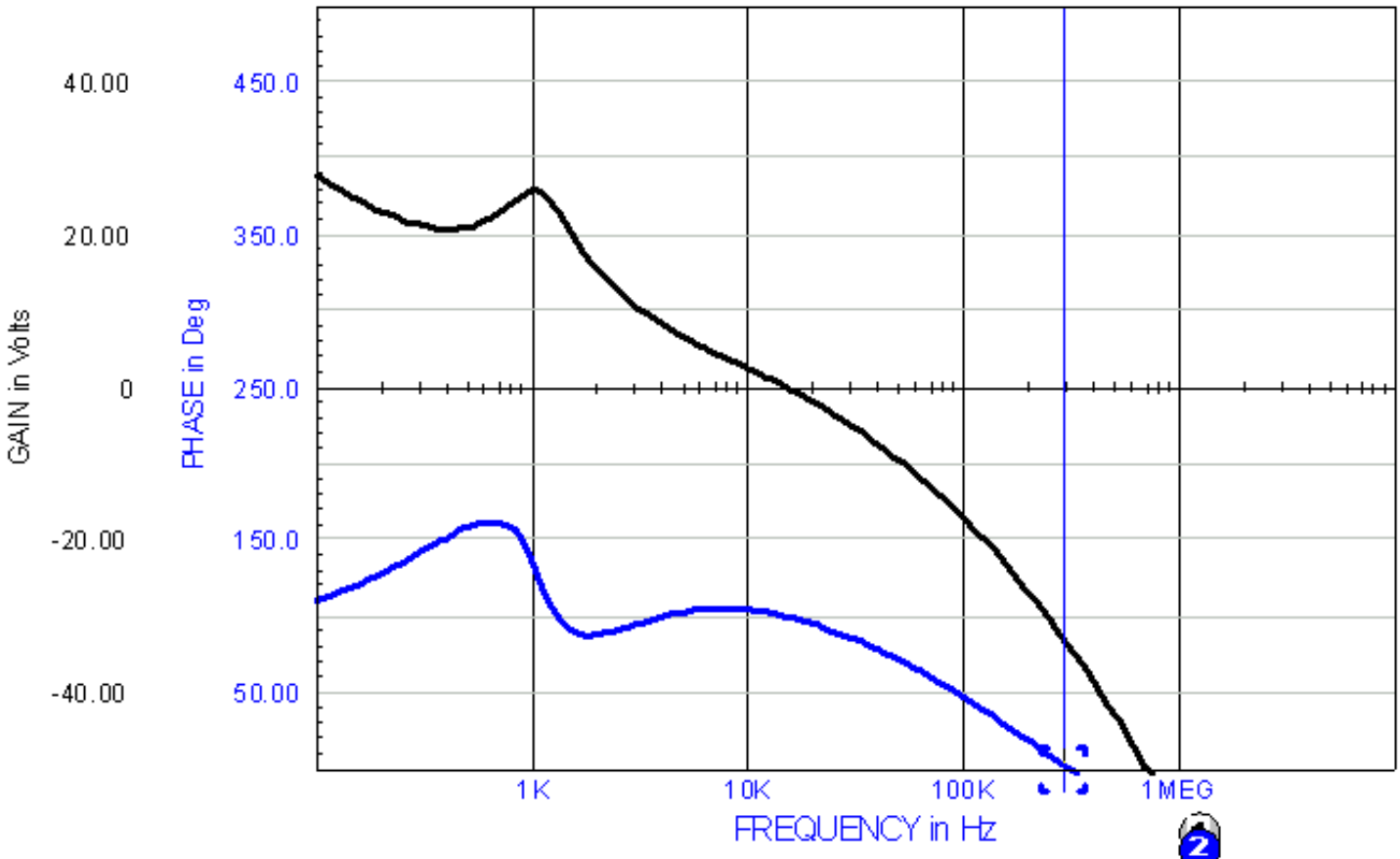
$$R_{18} := 1.428 10^{3}$$

$$F_5 = \frac{1}{2 \cdot \pi \cdot R_{18} C_7}$$

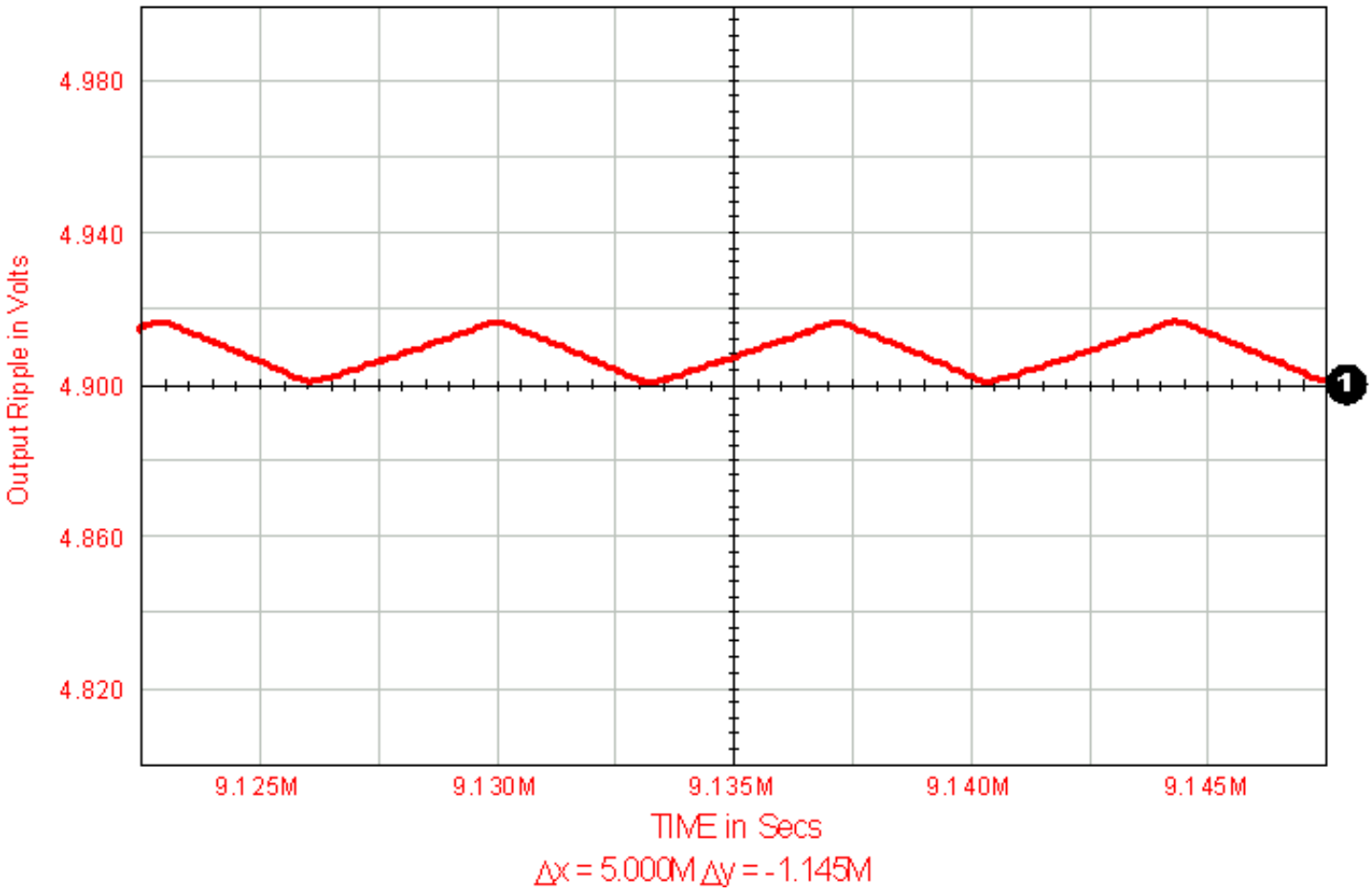
$$F_5 = 1.63910^4$$

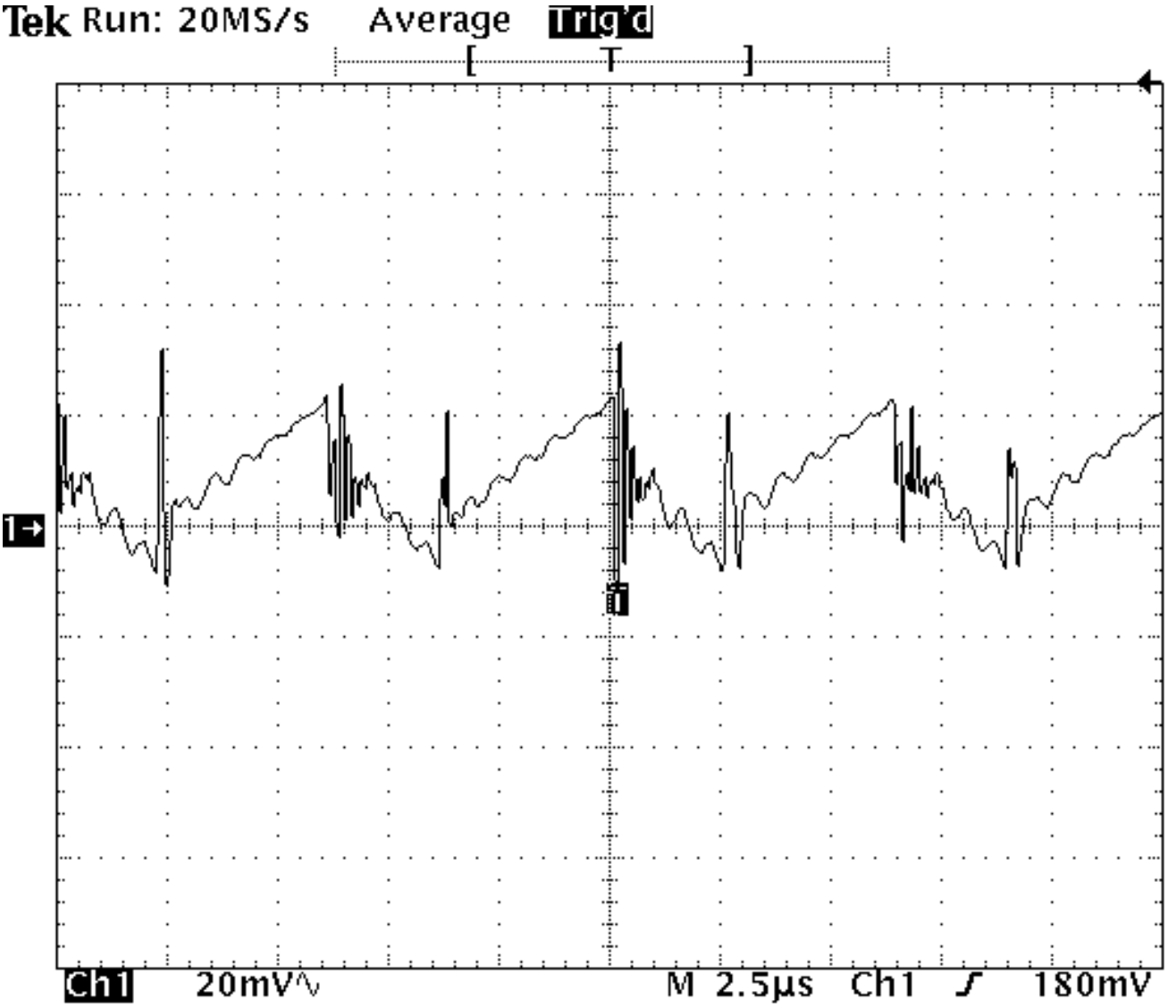

REF LEVEL
0.000dB
/DIV
10.000dB
MARKER 151 969.963Hz
MAG (A/R) -19.522dB
100
1K
10K
100K
1M
START 100.000Hz
STOP 1 000 000.000Hz

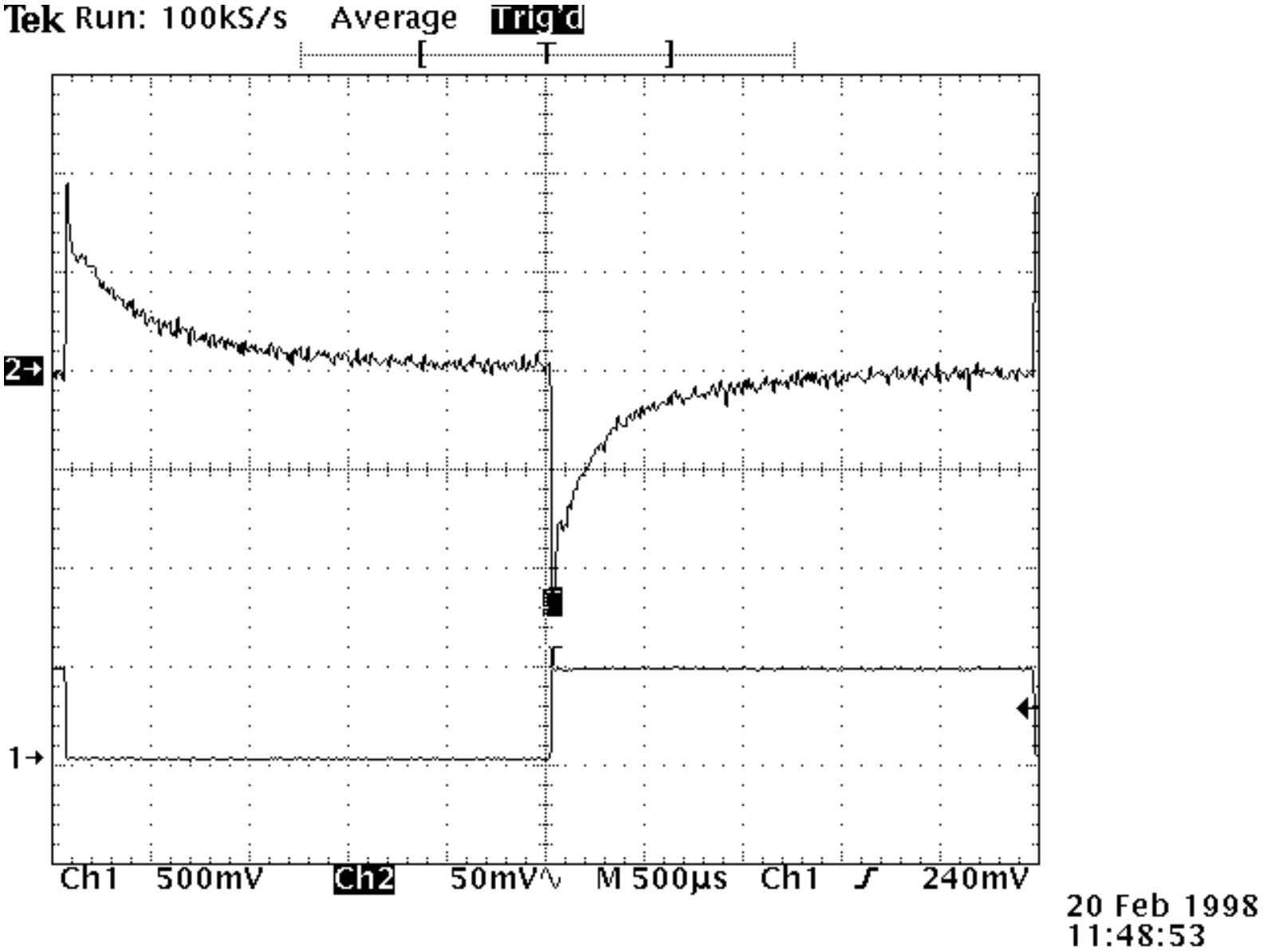

REF LEVEL
0.000dB
-24.000deg
/DIV
10.000dB
50.000deg
MARKER 12 071.403Hz
MAG (A/R) -0.226dB
MARKER 12 071.403Hz
PHASE (A/R) 103.145deg
100
1K
10K
100K
1M
START 100.000Hz
STOP 1 000 000.000Hz

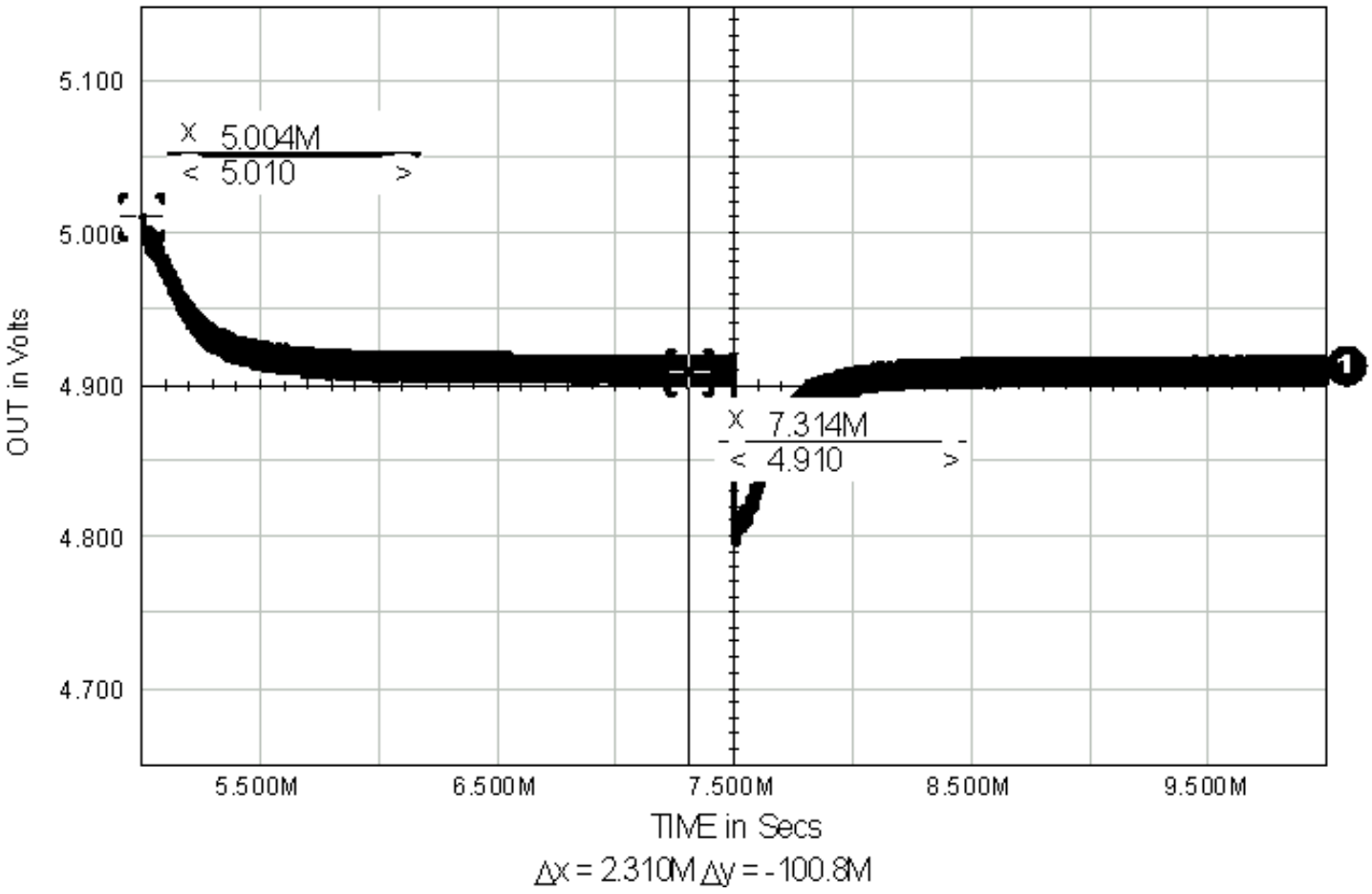


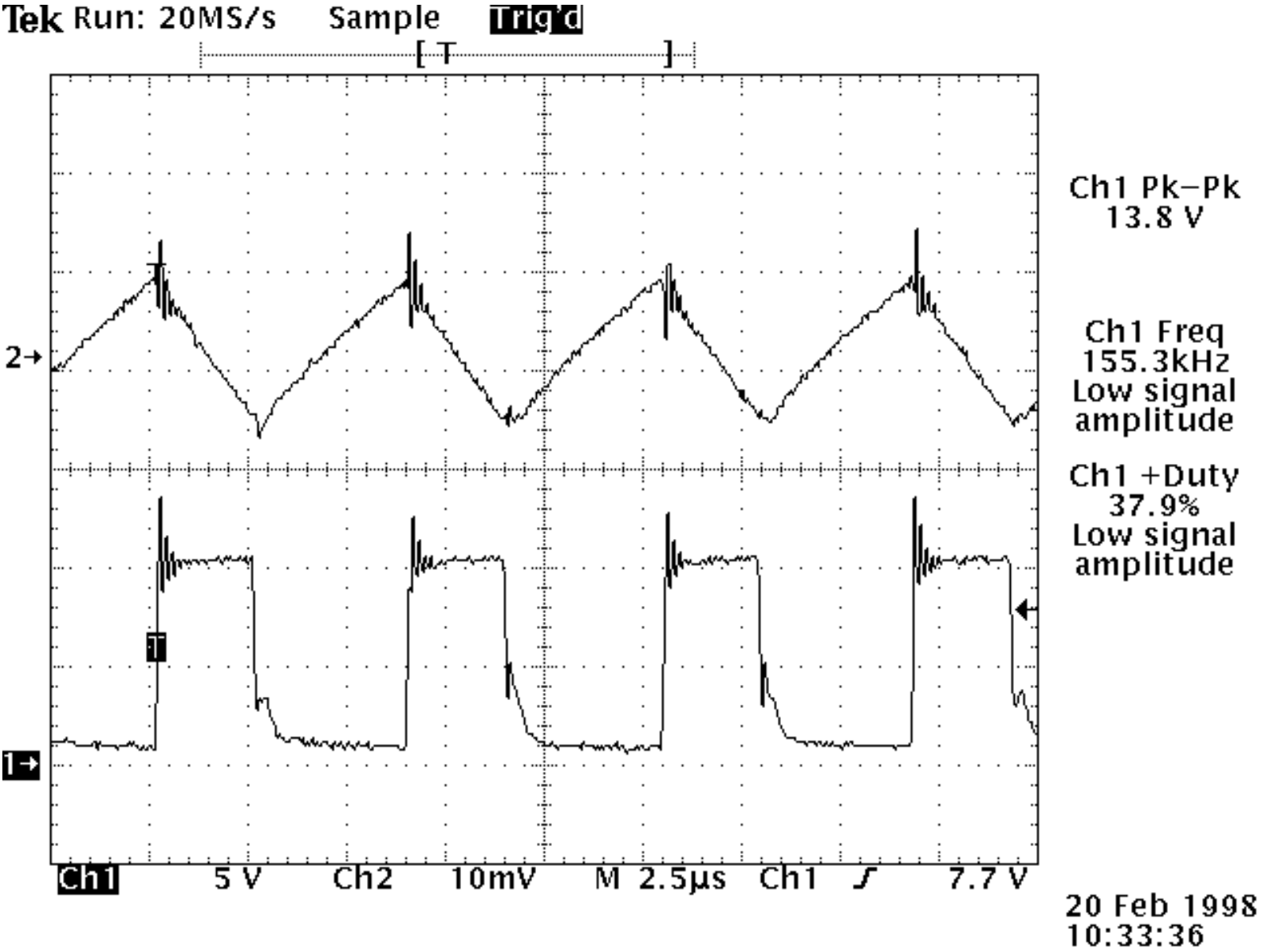
Phase=99.23 degrees; Gain=33.4 dB; Bandwidth=14.5KHz

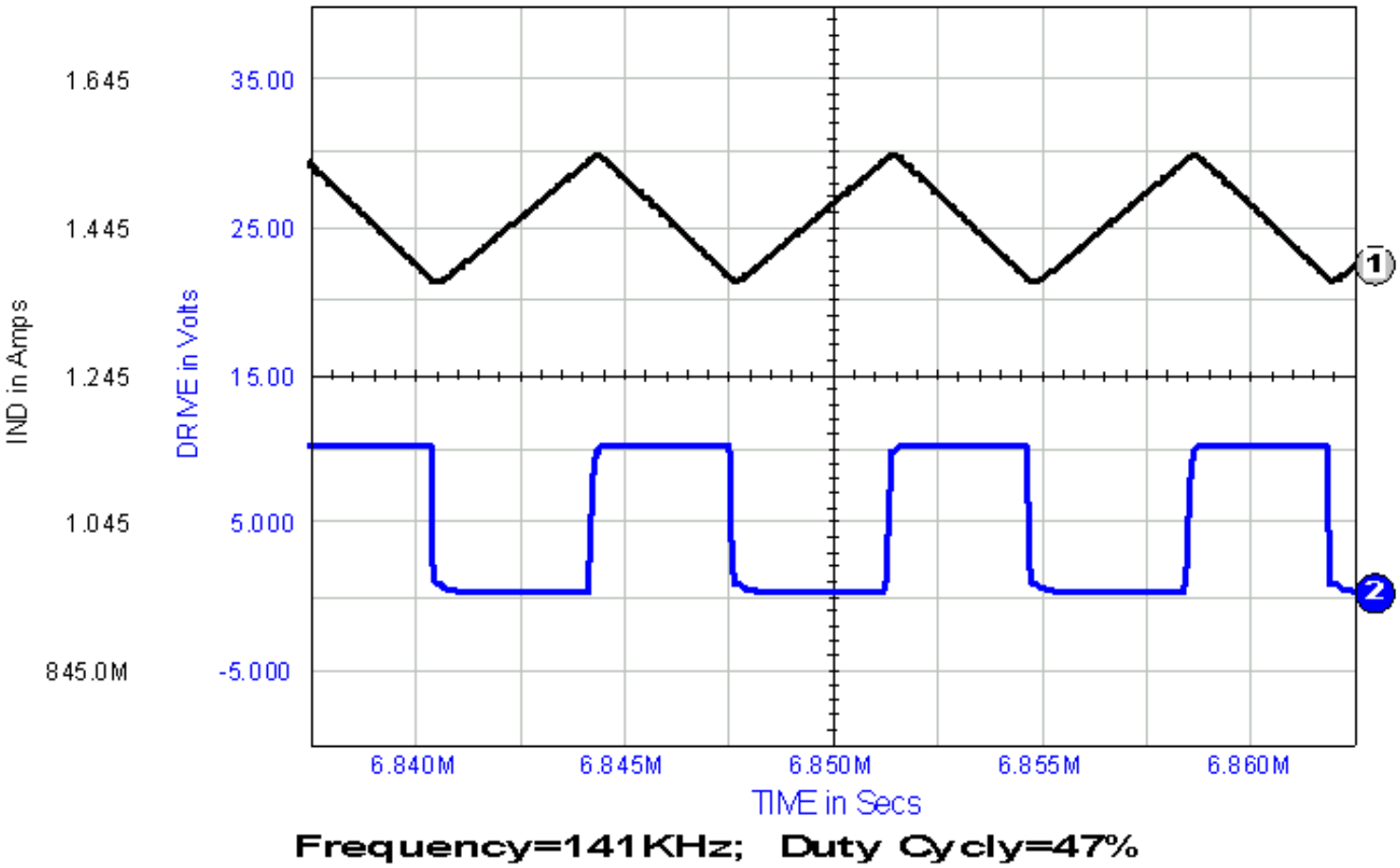

4.980
4.940
4.900
4.860
4.820
Output Ripple in Volts
9.125M
9.130M
9.135M
9.140M
9.145M
TIME in Secs
Δx = 5.000M Δy = -1.145M
1


Tek Run: 20MS/s Average Trig'd
Ch1 20mV
M 2.5µs Ch1 ƒ 180mV
20 Feb 1998
11:08:49

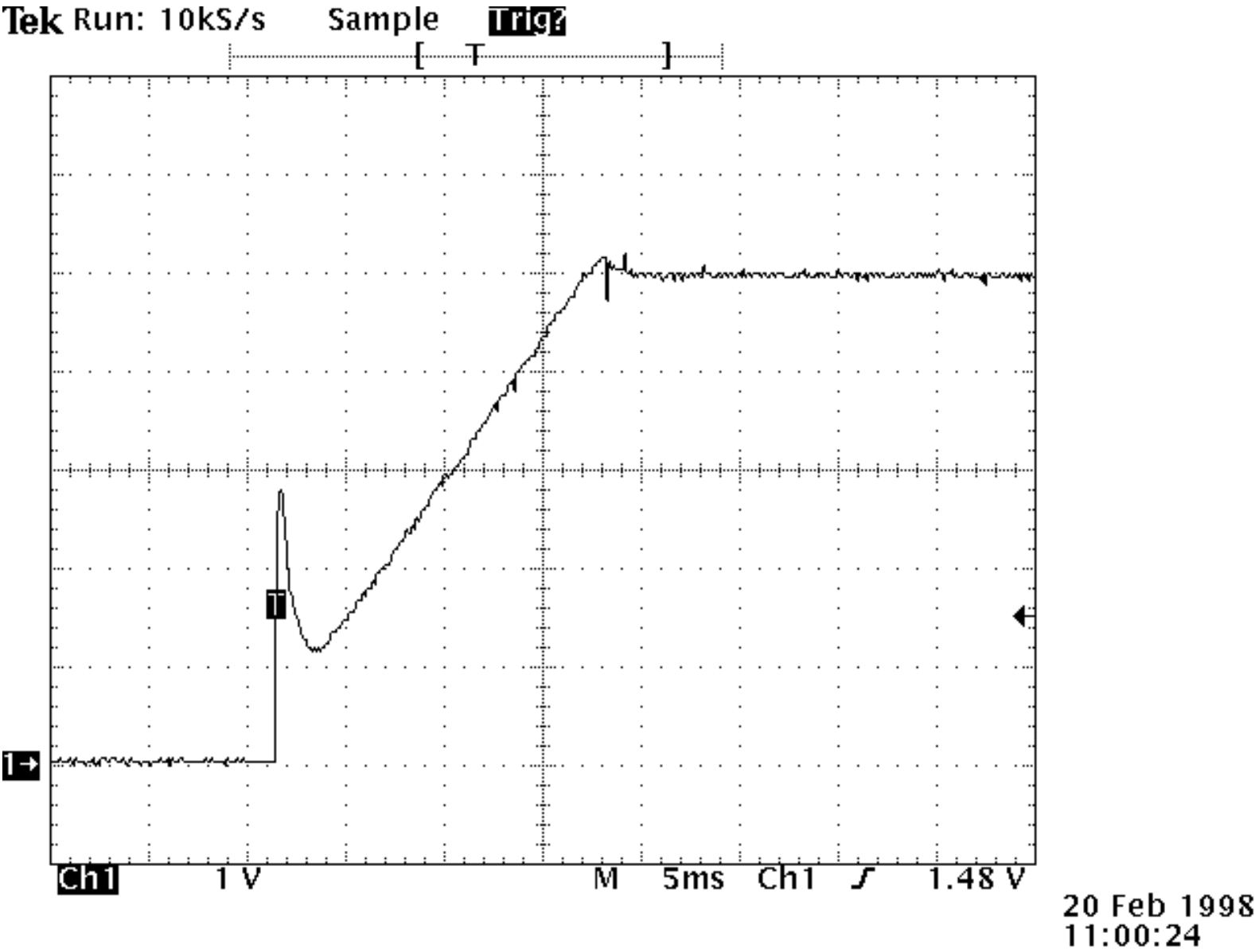

Tek Run: 100kS/s Average Trig'd
2→
1→
Ch1 500mV Ch2 50mV M 500µs Ch1 240mV
20 Feb 1998
11:48:53

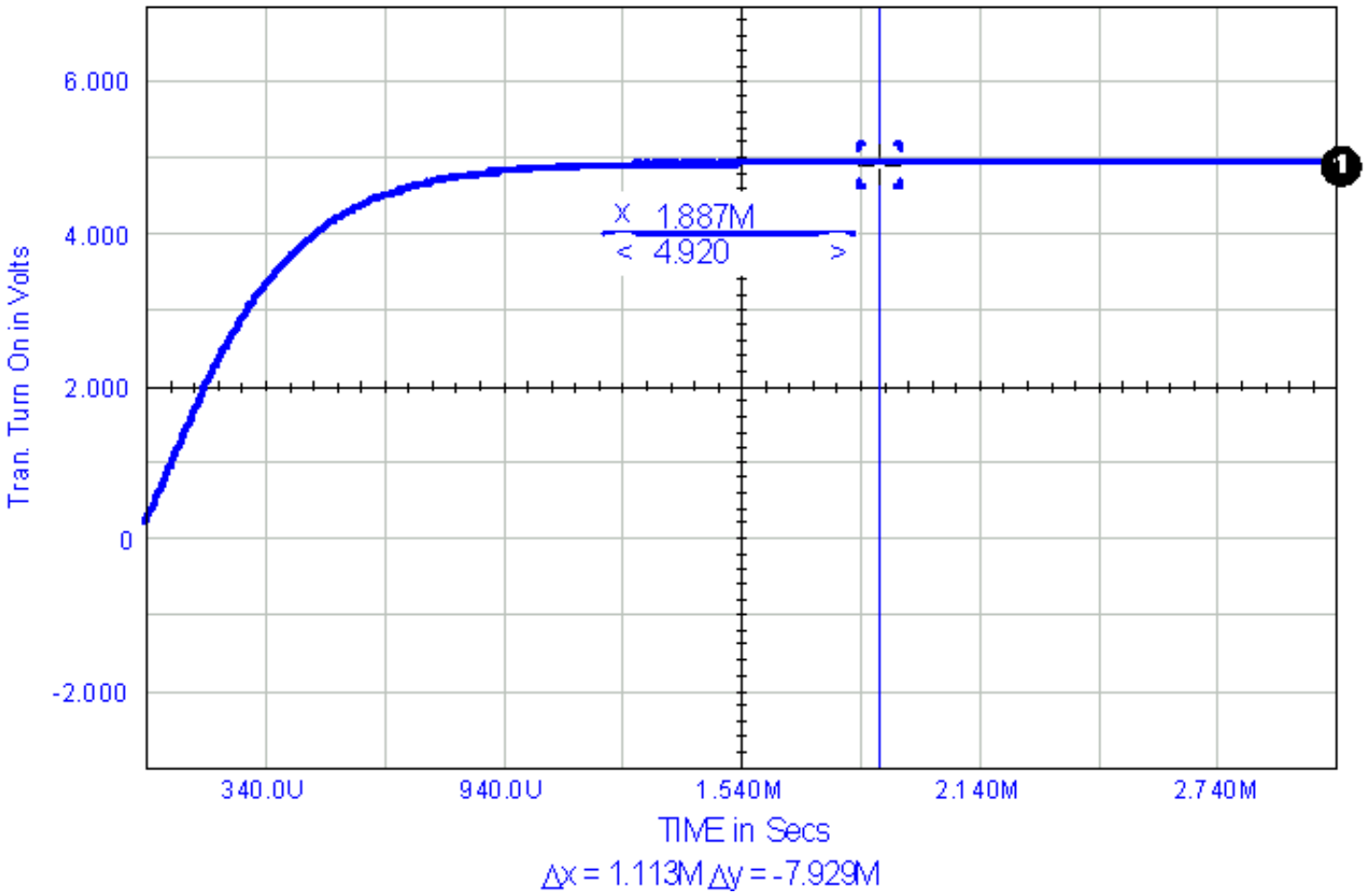

5.100
5.000
4.900
4.800
4.700
OUT in Volts
X 5.004M
< 5.010 >
X 7.314M
< 4.910 >
1
5.500M
6.500M
7.500M
8.500M
9.500M
TIME in Secs
Δx = 2.310M Δy = -100.8M

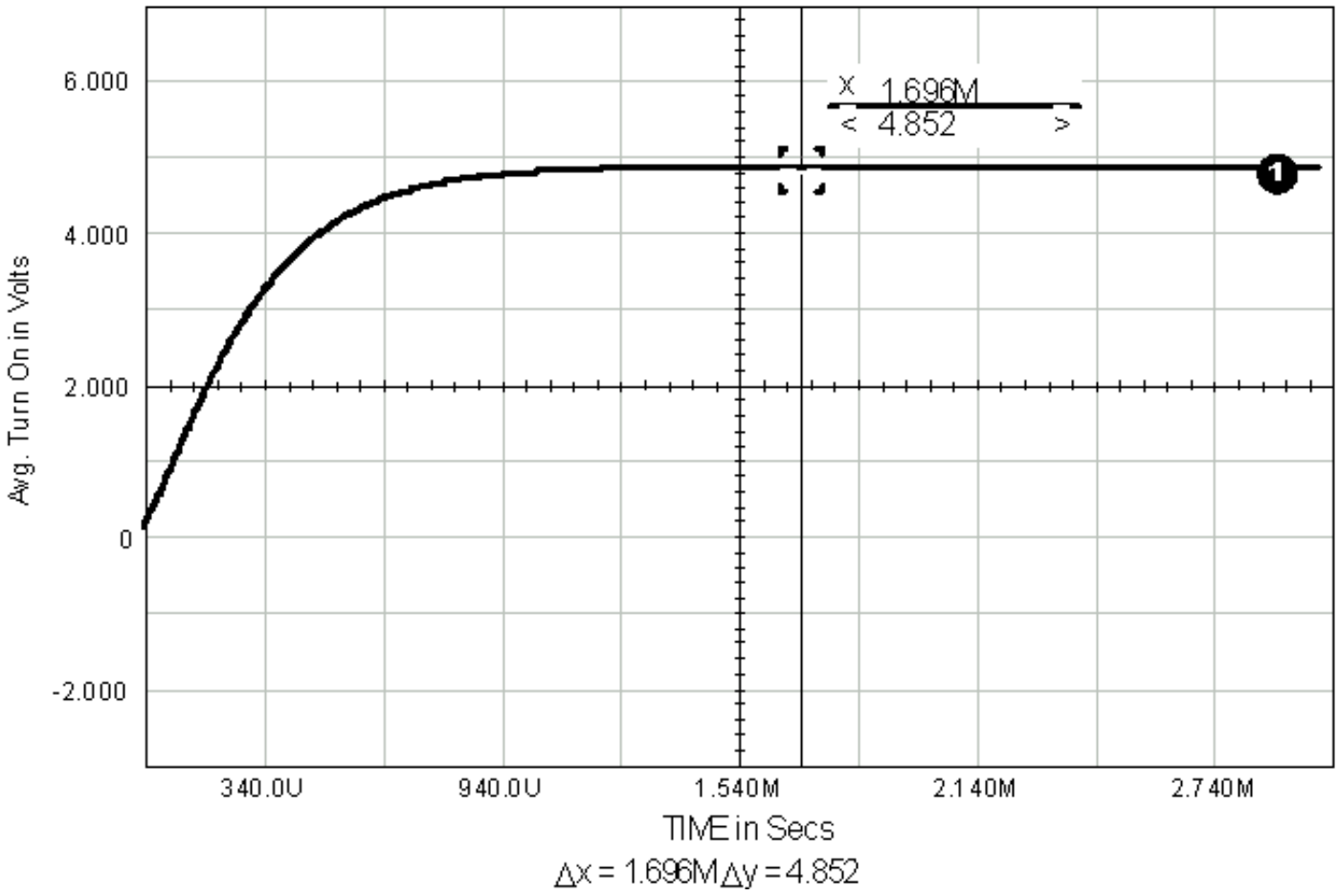

Tek Run: 20MS/s Sample Trig'd
Ch1 Pk-Pk
13.8 V
Ch1 Freq
155.3kHz
Low signal
amplitude
Ch1 +Duty
37.9%
Low signal
amplitude
Ch1 5 V Ch2 10mV M 2.5µs Ch1 7.7 V
20 Feb 1998
10:33:36

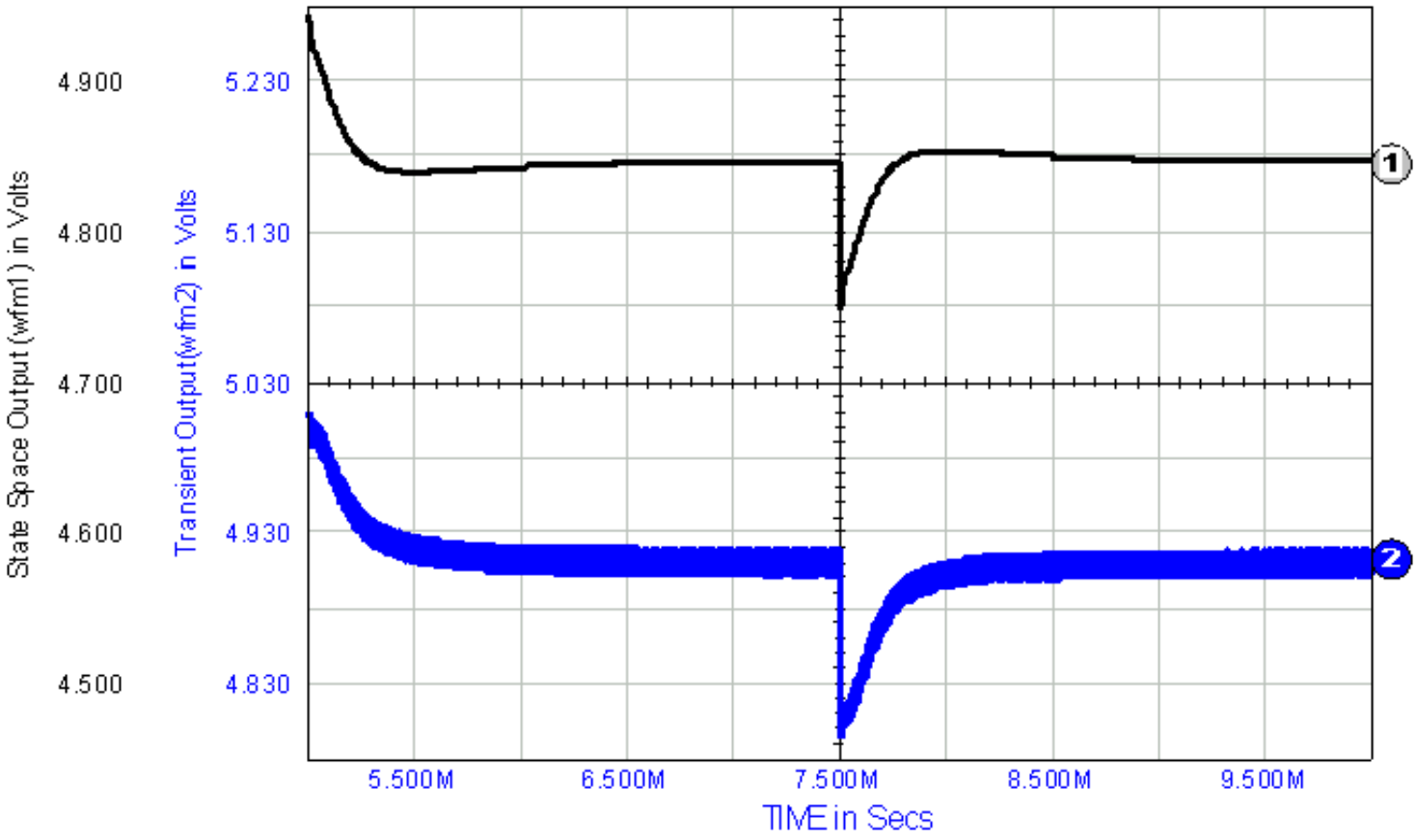


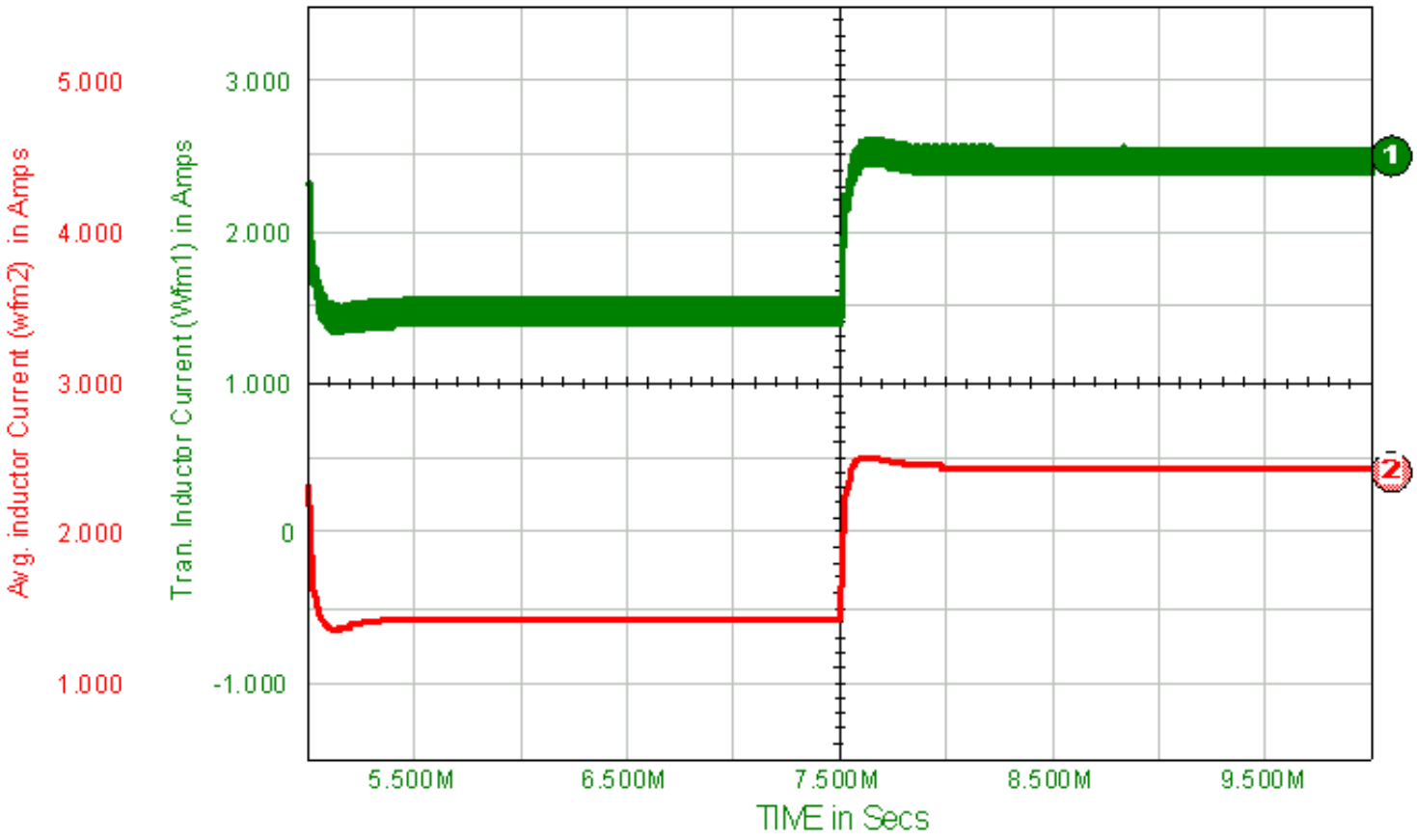
Frequency=141KHz; Duty Cycly=47%


Tek Run: 10kS/s Sample Trig?
Ch1 1 V M 5ms Ch1 ƒ 1.48 V
20 Feb 1998
11:00:24


6.000
4.000
2.000
0
-2.000
Tran. Turn On in Volts
X 1.887M
< 4.920 >
1
340.0U
940.0U
1.540M
2.140M
2.740M
TIME in Secs
Δx = 1.113M Δy = -7.929M


6.000
4.000
2.000
0
-2.000
Avg. Turn On in Volts
X 1.696M
< 4.852 >
1
340.0U
940.0U
1.540M
2.140M
2.740M
TIME in Secs
Δx = 1.696M Δy = 4.852


4.900
4.800
4.700
4.600
4.500
State Space Output (wfm1) in Volts
5.230
5.130
5.030
4.930
4.830
Transient Output(wfm2) in Volts
5.500M
6.500M
7.500M
8.500M
9.500M
TIME in Secs
1
2


5.000
4.000
3.000
2.000
1.000
Avg. inductor Current (wfm2) in Amps
3.000
2.000
1.000
0
-1.000
Tran. Inductor Current (Wfm1) in Amps
5.500M
6.500M
7.500M
8.500M
9.500M
TIME in Secs
1
2

#16: STR6600 Quasi-Resonant Discontinuous Flyback

Quasi-Resonant converters have additional desirable characteristics that standard switching converters do not. Quasi-Resonant converters can greatly decrease the power losses dissipated in the semiconductor components while reducing radiated interference [Brown, 1994]. These converters accomplish this by forcing the voltage or current into a sinusoidal waveform. The Quasi-Resonant converter switches the MOSFET while the current or voltage is at zero, resulting in little or no switching losses.

The following example of this type of power supply is a Zero-Current Switching (ZCS) Quasi-Resonant power supply utilizing the STR6600 hybrid IC. The STR6600 contains both the power MOSFET and the control circuitry for implementing this type of power supply. In a ZCS type circuit, the current through the power switch is forced to be sinusoidal and the transistor is switched when this current is at or near zero.

The following circuit (Figure 16-1) shows the implementation of a Quasi-Resonant flyback converter featuring the STR6600.

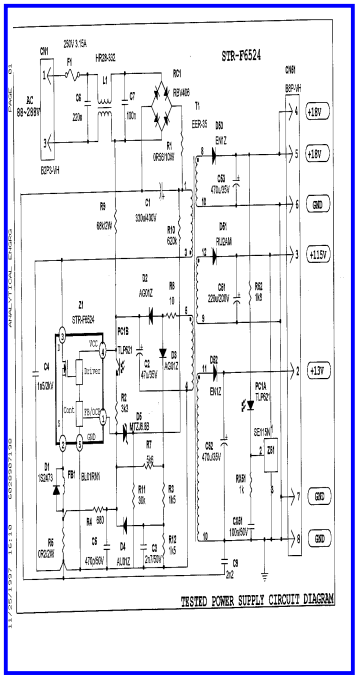


Figure 16-1: Circuit schematic for Quasi-resonant flyback converter

A switching cycle begins with the turn on of the Power Mosfet, which is internal to the STR-F6524. The current in the Mosfet rises, starting at approximately zero amps and increasing at a rate determine by the input voltage and the primary inductance of the power transformer.

The current generates a proportional voltage across the resistor, connected from the source pin to the input return A control signal is added to the current signal via a resistor connected from the source pint to the OCP pin, allowing a voltage or current injection into the OCP pin. The Mosfet will be turned off when the sum of the source current and the control signal reach 0.73 volts.

After the Mosfet turns off, the drain voltage rises and the primary peak current is delivered to the load. The current then falls at a rate determined by the output voltage and the primary inductance. Once the energy in the primary inductance is depleted, the drain voltage falls, in accordance with the resonant characteristics of the primary inductance and the resonant capacitance (plus the primary transformer capacitance and the Mosfet output capacitance).

Several modifications have been made to the values listed on the schematic, based on actual measurements of the components. Resistor R5 is actually 0.14 Ohms in the breadboard. The primary inductance of the power transformer measured 324 uHy. The output capacitor measured 200 uFd with an ESR of 0.13 Ohms.

Construction of the SPICE model to measure the AC characteristics of this circuit made some simplifications. The low power outputs have a negligible effect on the AC characteristics of the control loop, and are not included in the SPICE model. The SPICE model schematic is shown in Figure 16-2.

The control loop was effectively opened for the open loop test by injecting a voltage source directly into the FB/OCP pin. This voltage was adjusted to provide an output voltage of approximately 102 volts. For the closed loop test, this external voltage source was not used.

In the SPICE model, when the closed loop bode plot was measured, L1 was increased to 1 H and C3 was increased to 1 F.

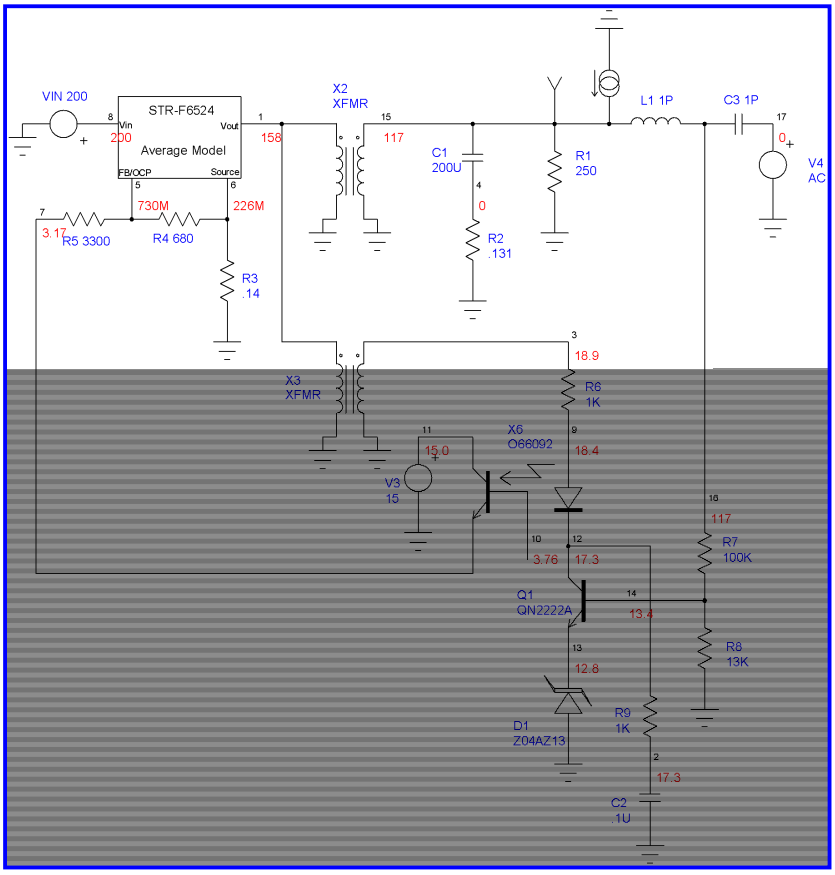


Figure 16-2: SPICE model of average mode operation of Quasi-Resonant Flyback

Measurements on the breadboard configuration were made at several output capacitor values. The results are shown in Figure 16-3. The SPICE model was simulated at Vin=110 VDC [85 volts AC], with the 200 uF output capacitor. The results of the SPICE model are shown in Figure 16-4.

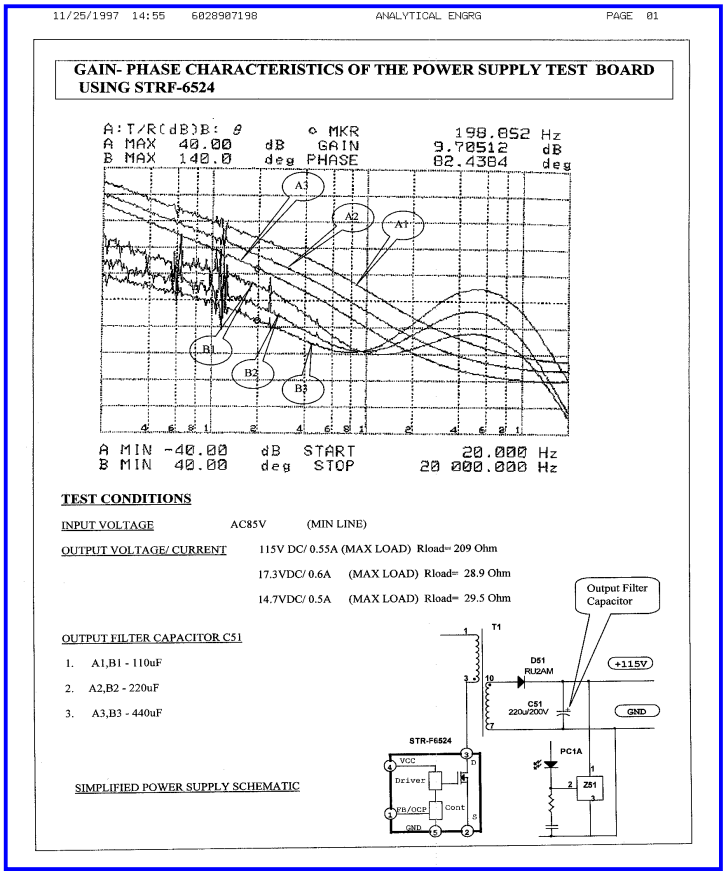


Figure 16-3: Breadboard bode plots [Data provided courtesy of Allegro ®]

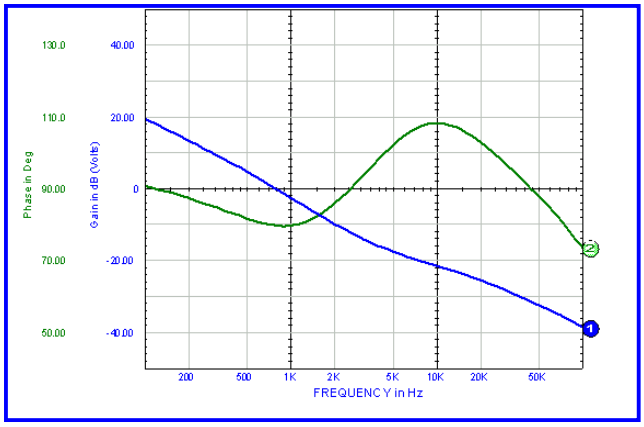


Figure 16-4: IsSpice bode plot results (Vin=110DC [85AC], Cout=200uF)

Comparing the results of Figure 16-3 and 16-4, the phase margin is 78 degrees in the breadboard plot, compared to 79.6 degrees in the IsSpice plot. The crossover in the breadboard plot was 800 Khz, compared to 783 Khz in the IsSpice plot. The general shapes of the curves are also very similar.

The modulation gain of the test circuit was also measured. The modulation gain is the gain from the output of the opto-coupler to the output of the STR-F6524 average mode model. The breadboard results are shown in Figure 16-5. The IsSpice results are shown in Figure 16-6.

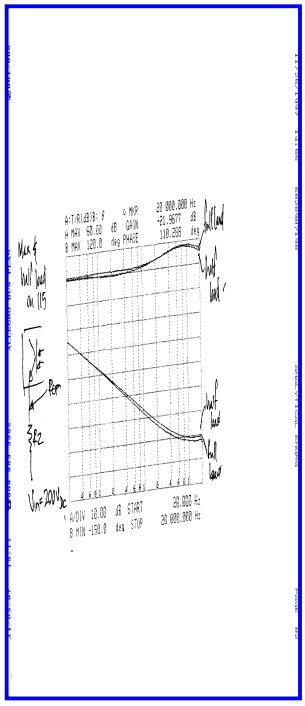


Figure 16-5: breadboard modulation gain bode plot

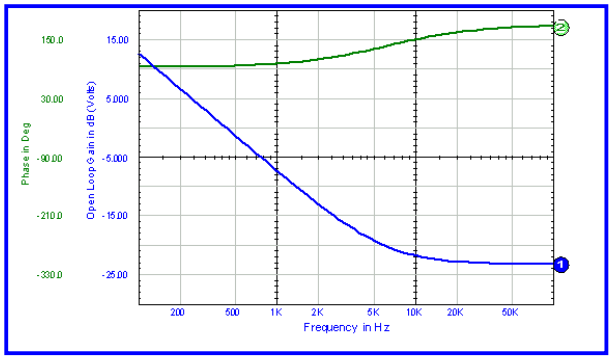


Figure 16-6: IsSpice modulation gain bode plot

Output impedance was measured on both the breadboard and the IsSpice model. To simulate the output impedance, the voltage source V4 was changed to AC 1P and the current source on the output was changed to AC 1. The breadboard measurements are shown in Figure 16-7 while the IsSpice results are shown in Figure 16-8.

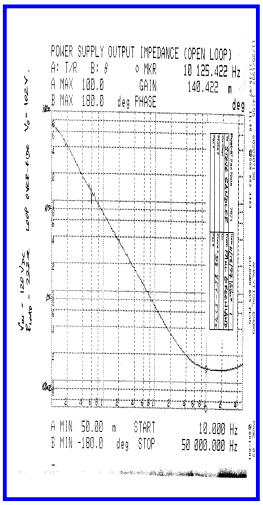


Figure 16-7: Breadboard open loop output impedance

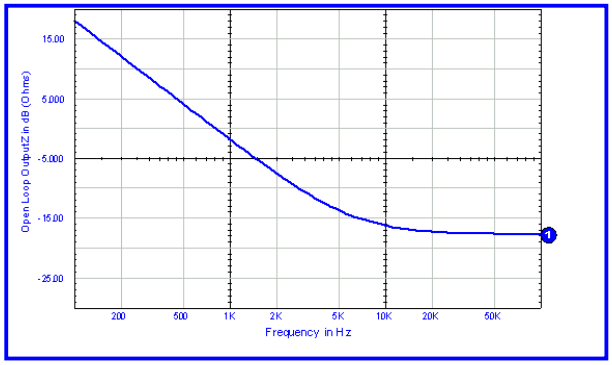


Figure 16-8: IsSpice open loop output impedance

The simulation results from Microcap and Pspice for the control loop characteristics of the Quasi-Resonant converter are shown in Figure 16-9 and 16-10.

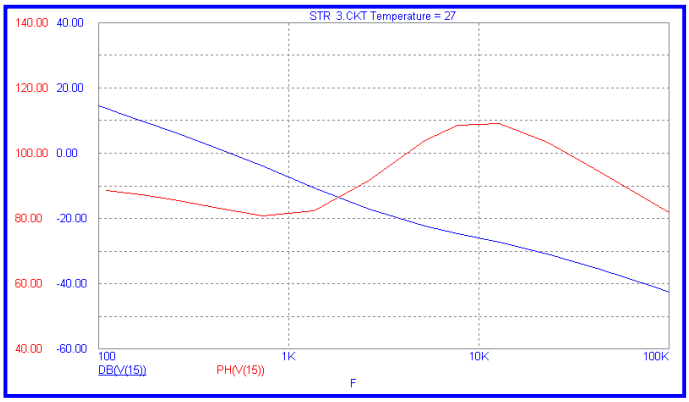


Figure 16-9: Microcap bode plot results

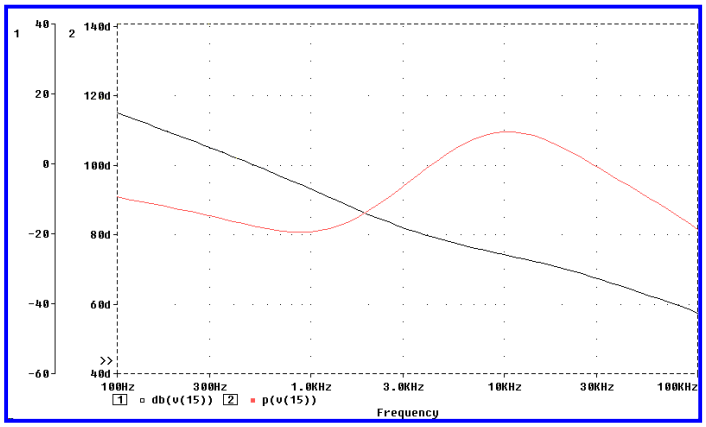
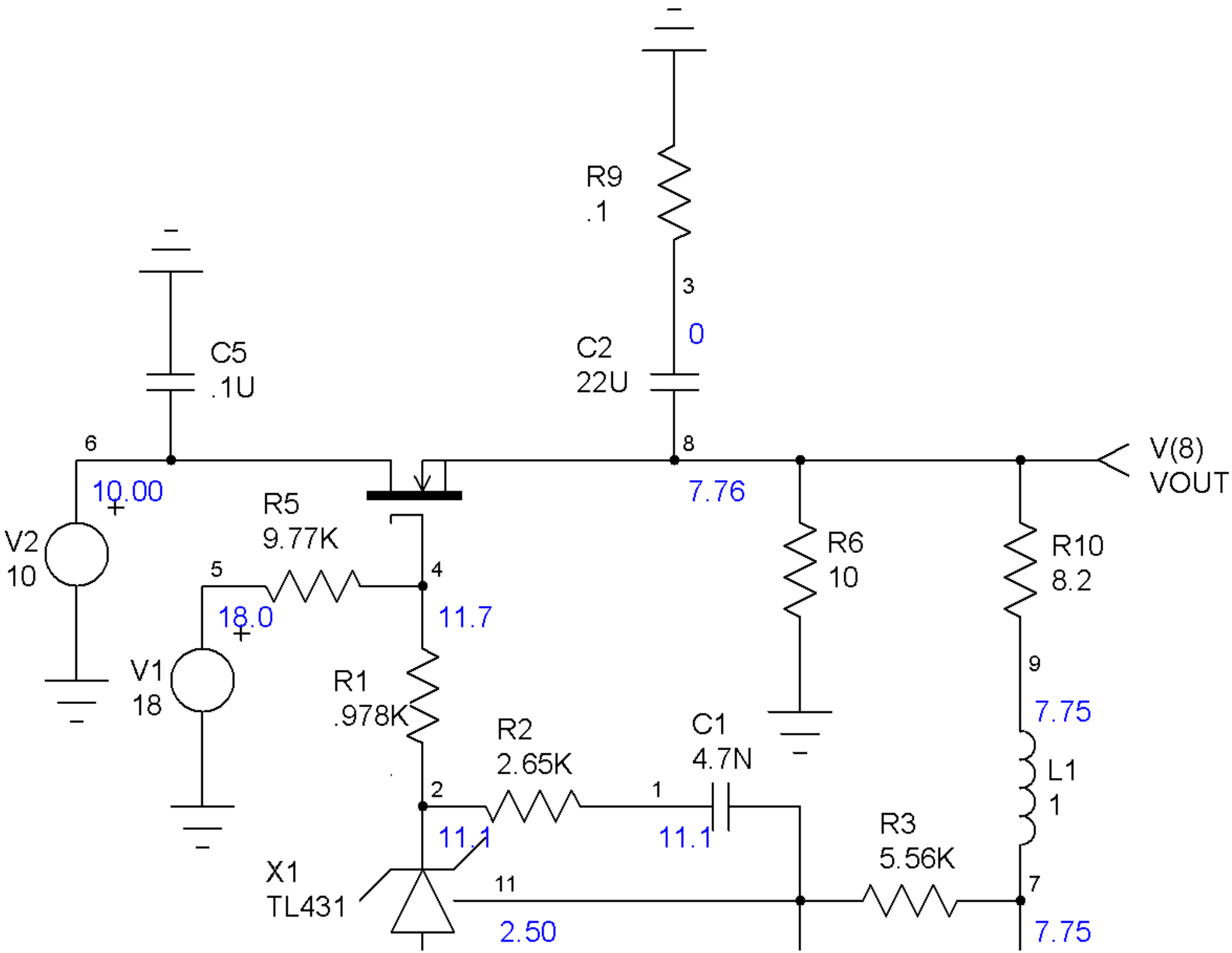
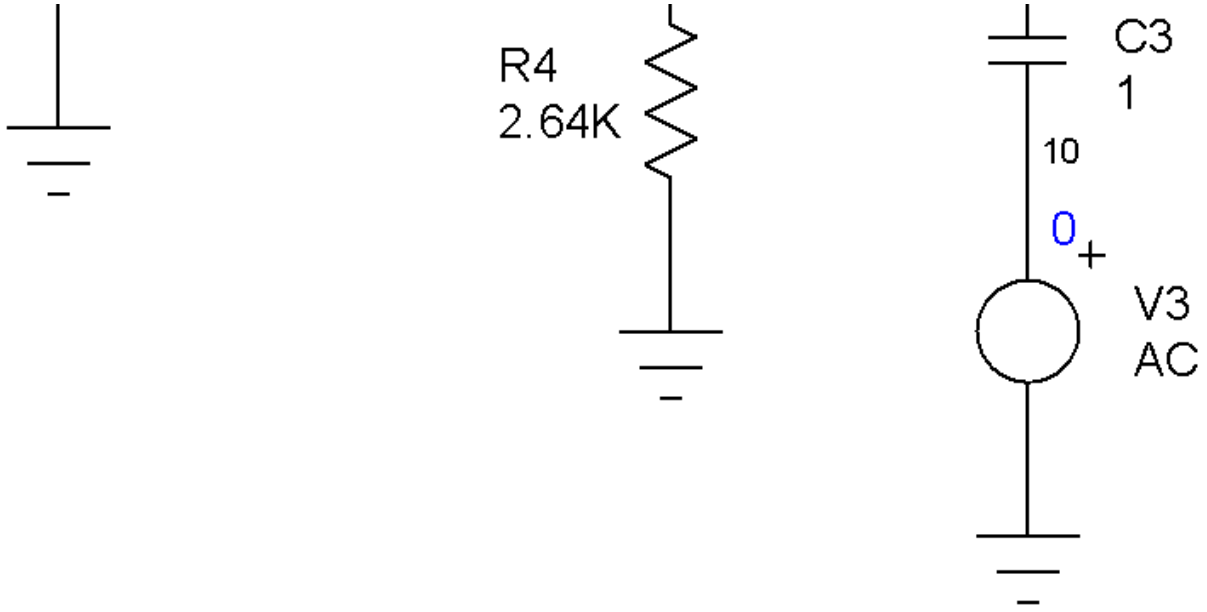


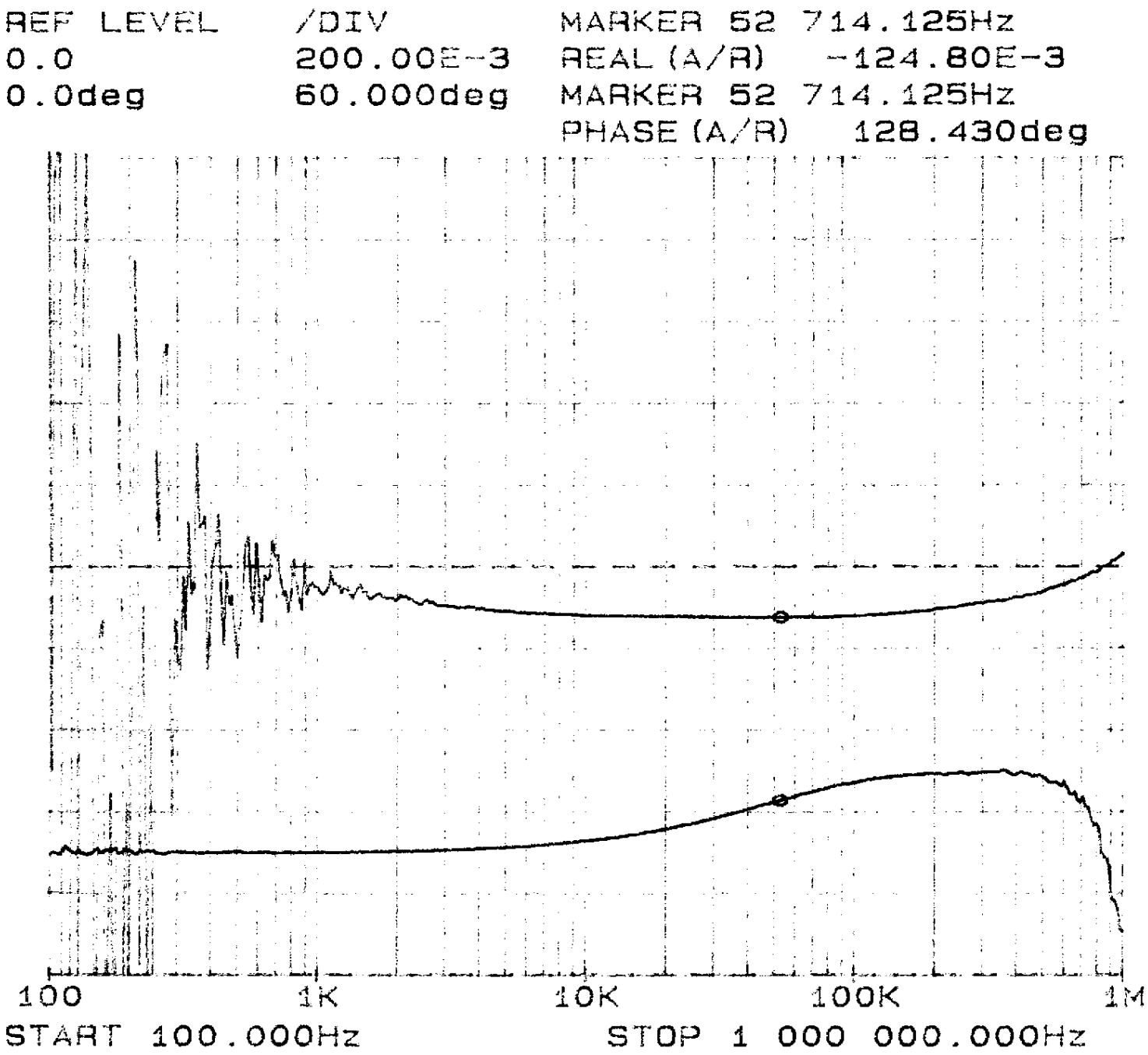
Figure 16-10: Pspice bode plot results

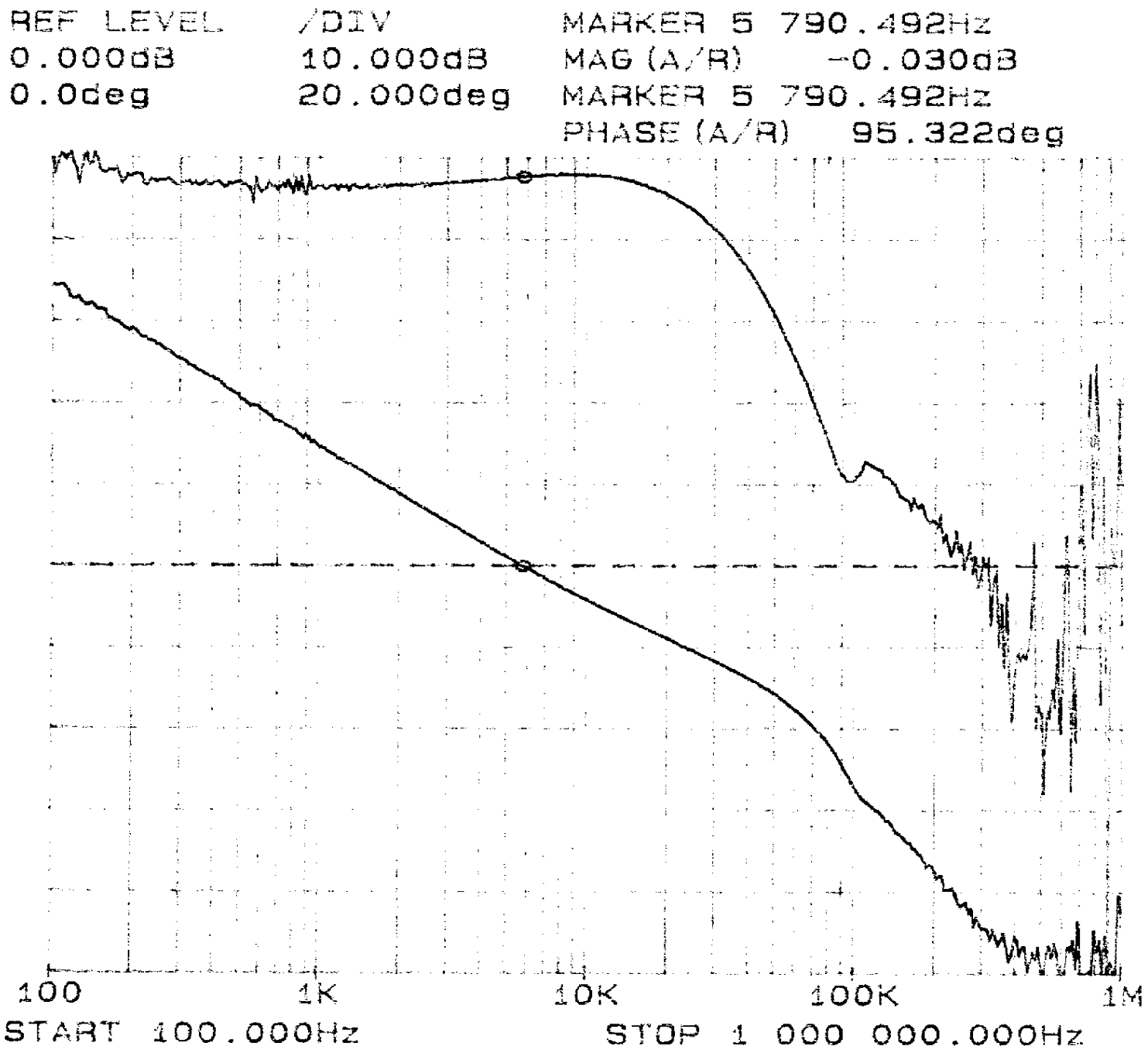
Run Time Summary		
IsSpice v 7.6	PsPice v 6.3	Micro-Cap V v2
0.833 Sec	0.20 Sec	0.32 Sec
Advantages: Reduced MOSFET switching losses, reduced EMI		
Disadvantages: Added circuit complexity, increased cost from additional components		

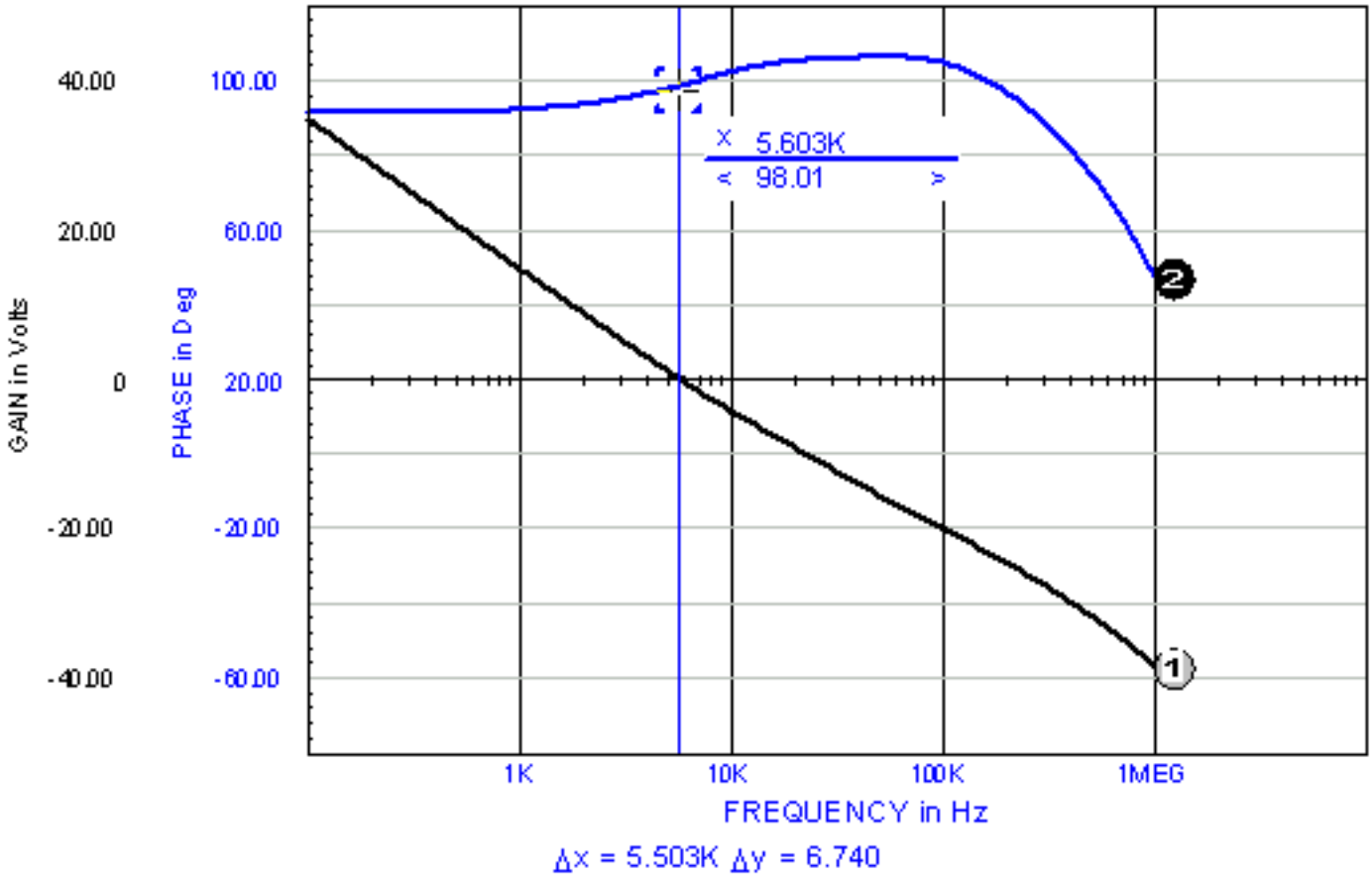
Filenames: STR6500 (IsSpice) str_3 (Microcap) str_2 (Pspice)

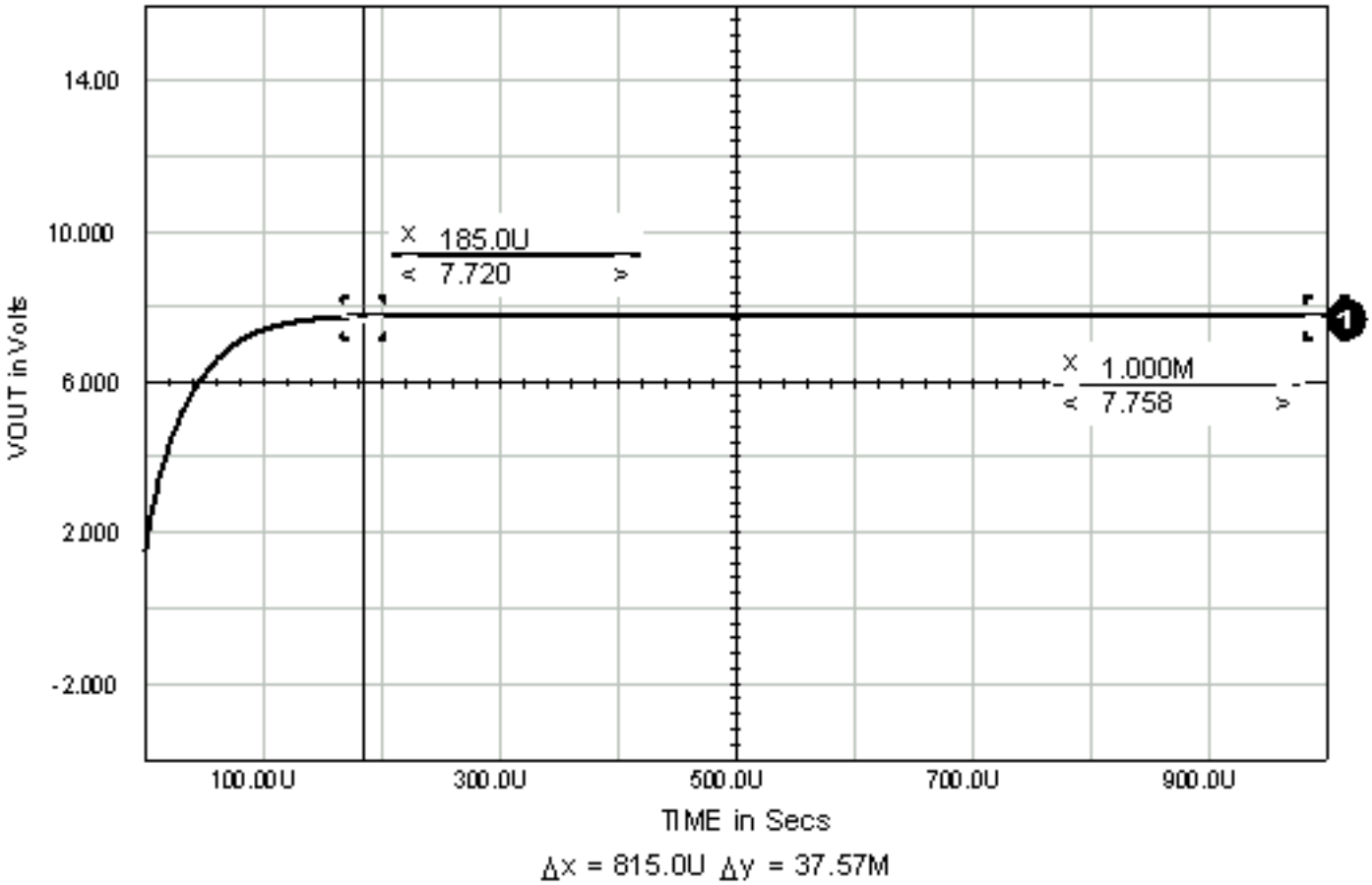

R9
.1
3
0
C2
22U
C5
.1U
6
8
V(8)
VOUT
10.00
7.76
V2
10
R5
9.77K
5
4
18.0
11.7
R6
10
R10
8.2
V1
18
R1
.978K
9
7.75
R2
2.65K
C1
4.7N
L1
1
2
1
11.1
11.1
R3
5.56K
X1
TL431
11
7
2.50
7.75

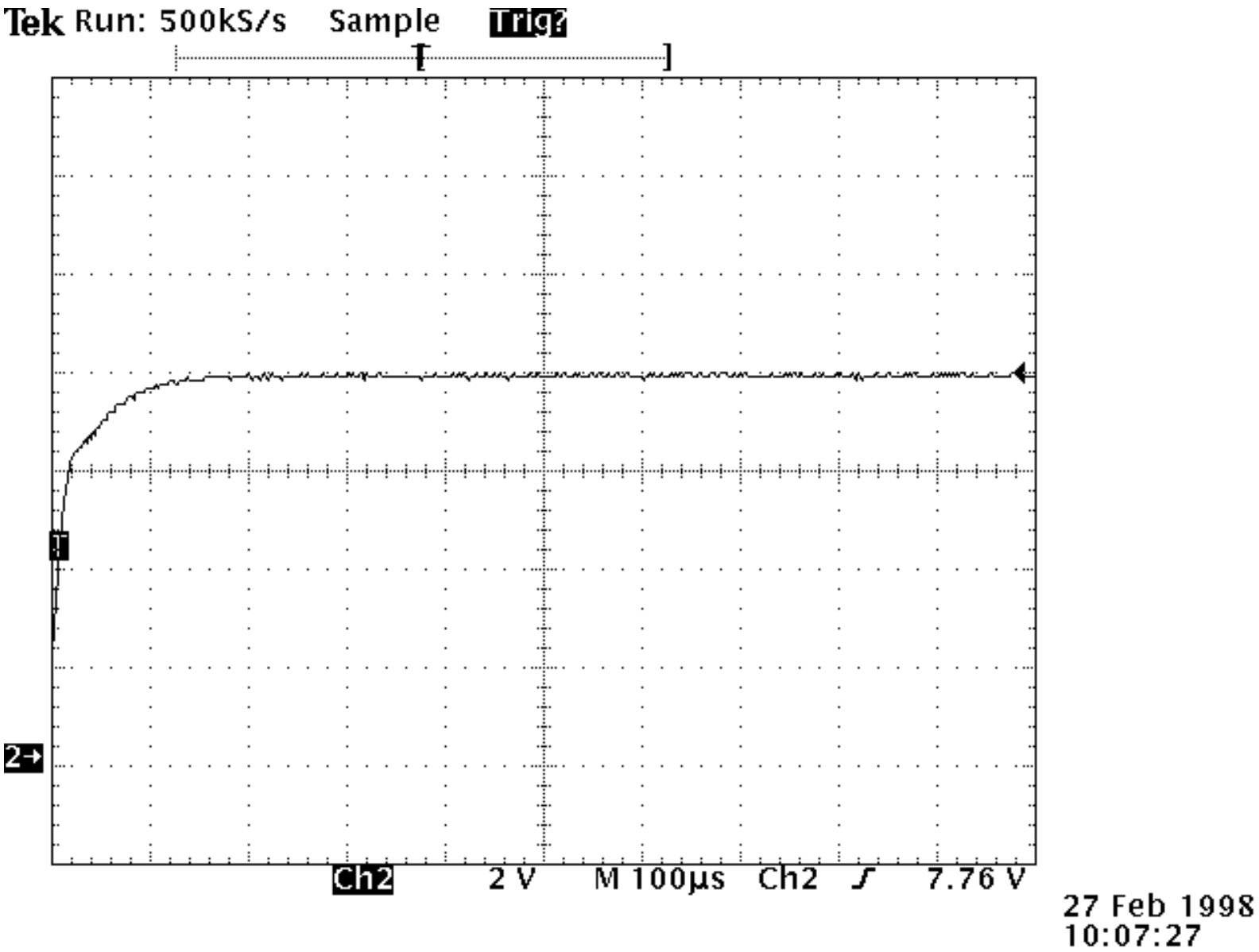

R4
2.64K
C3
1
10
0
+
V3
AC

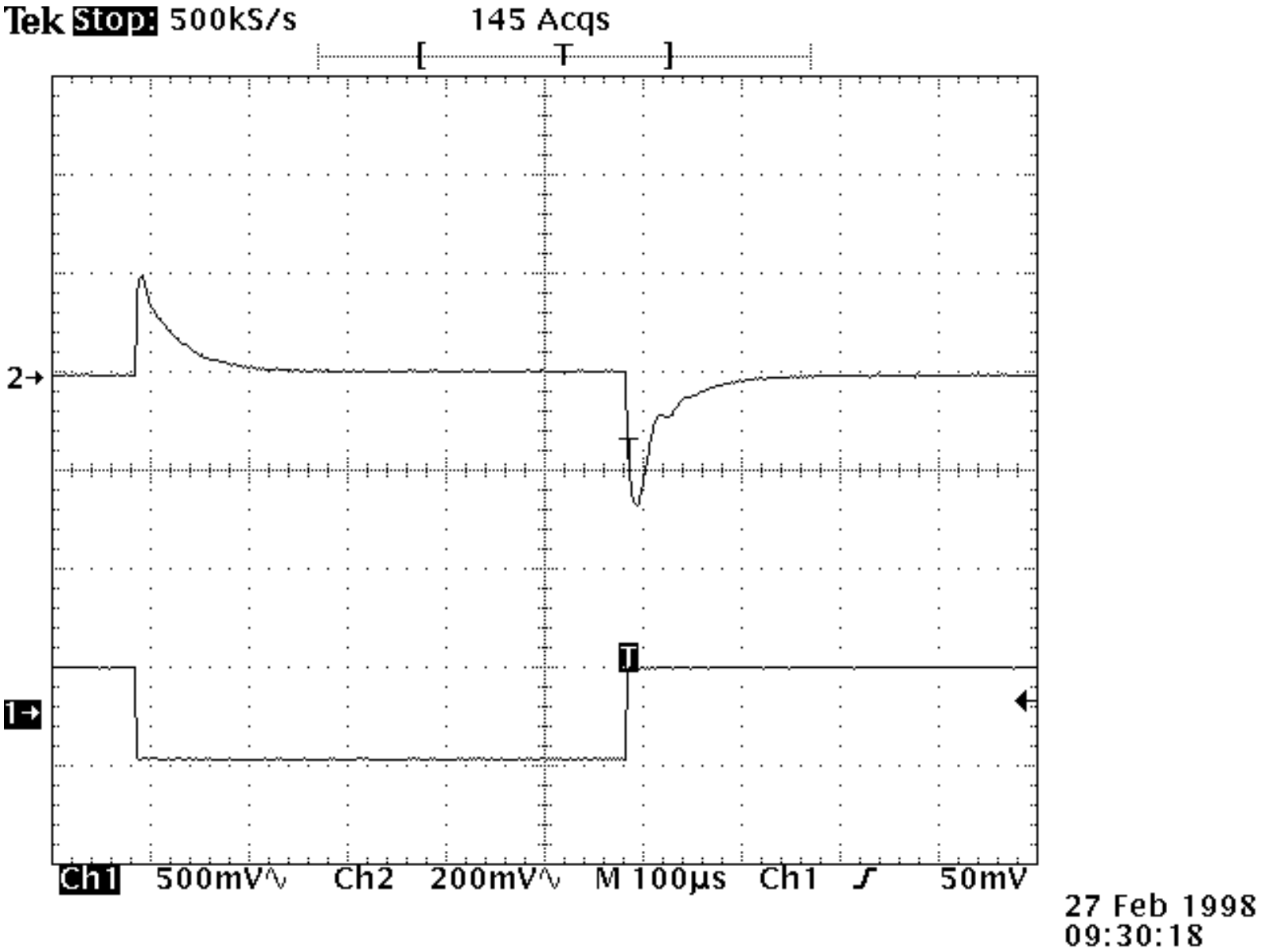

REF LEVEL
0.0
0.0deg
/DIV
200.00E-3
60.000deg
MARKER 52 714.125Hz
REAL (A/R) -124.80E-3
MARKER 52 714.125Hz
PHASE (A/R) 128.430deg
100
1K
10K
100K
1M
START 100.000Hz
STOP 1 000 000.000Hz

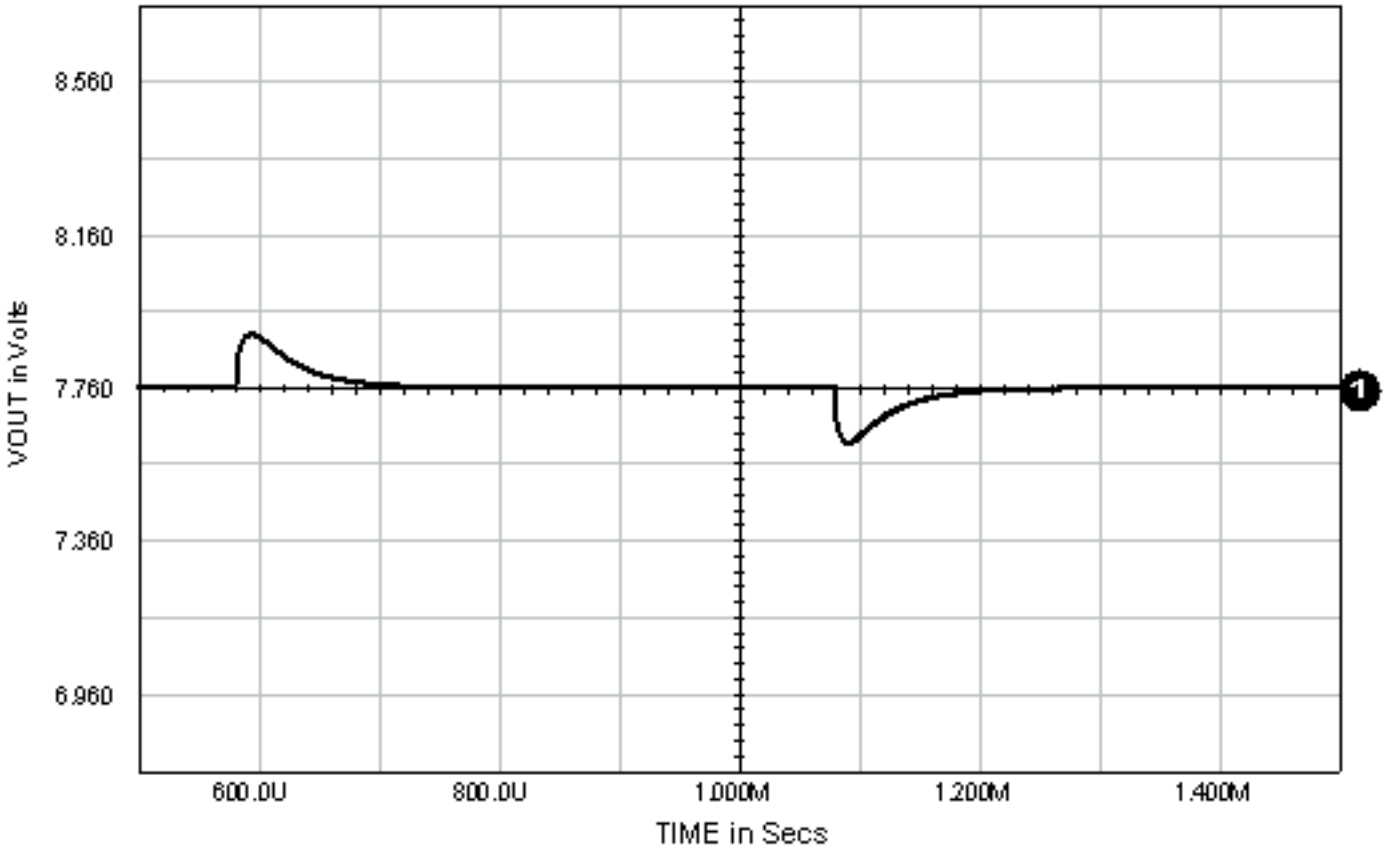

REF LEVEL
0.000dB
0.0deg
/DIV
10.000dB
20.000deg
MARKER 5 790.492Hz
MAG (A/R) -0.030dB
MARKER 5 790.492Hz
PHASE (A/R) 95.322deg
100
1K
10K
100K
1M
START 100.000Hz
STOP 1 000 000.000Hz

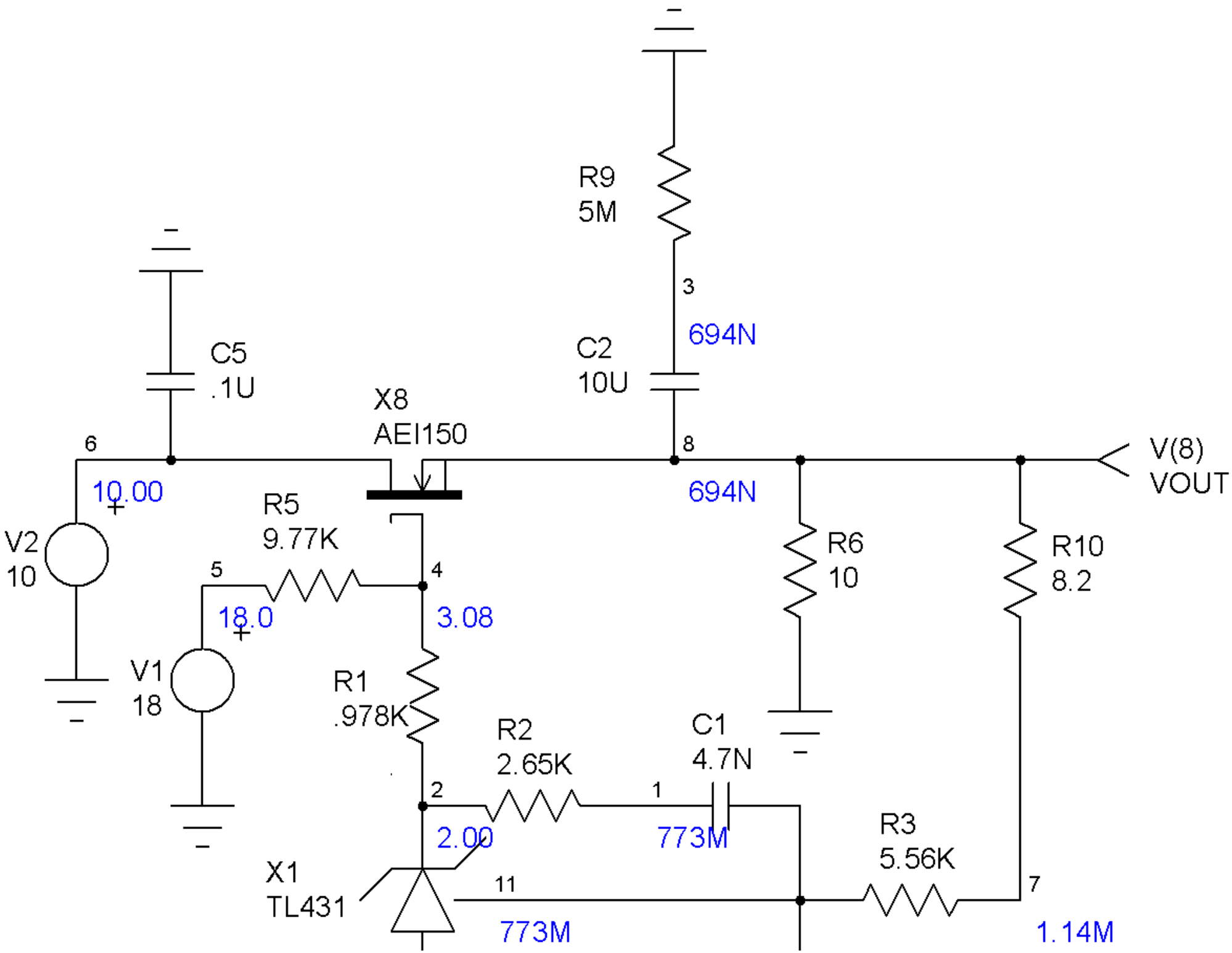

40.00
20.00
0
-20.00
-40.00
GAIN in Volts
100.00
60.00
20.00
-20.00
-60.00
PHASE in Deg
X 5.603K
< 98.01 >
1K
10K
100K
1MEG
FREQUENCY in Hz
Δx = 5.503K Δy = 6.740


14.00
10.000
6.000
2.000
-2.000
VOUT in Volts
X 185.0U
< 7.720 >
X 1.000M
< 7.758 >
1
100.00U
300.0U
500.0U
700.0U
900.0U
TIME in Secs
Δx = 815.0U Δy = 37.57M

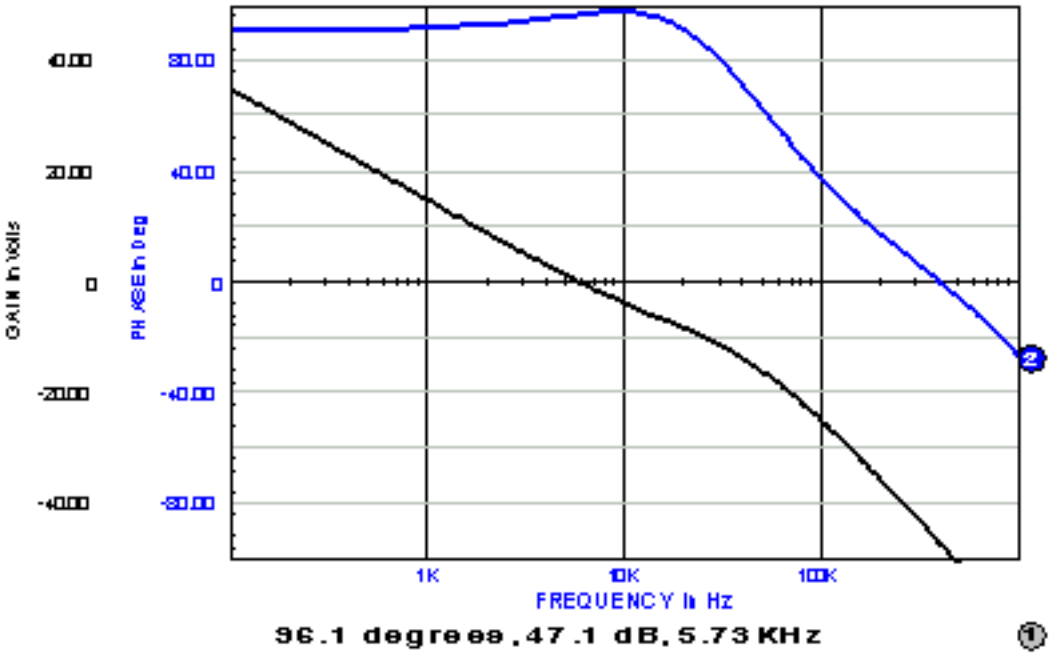

Tek Run: 500kS/s Sample Trig?
Ch2 2 V M 100µs Ch2 ƒ 7.76 V
27 Feb 1998
10:07:27

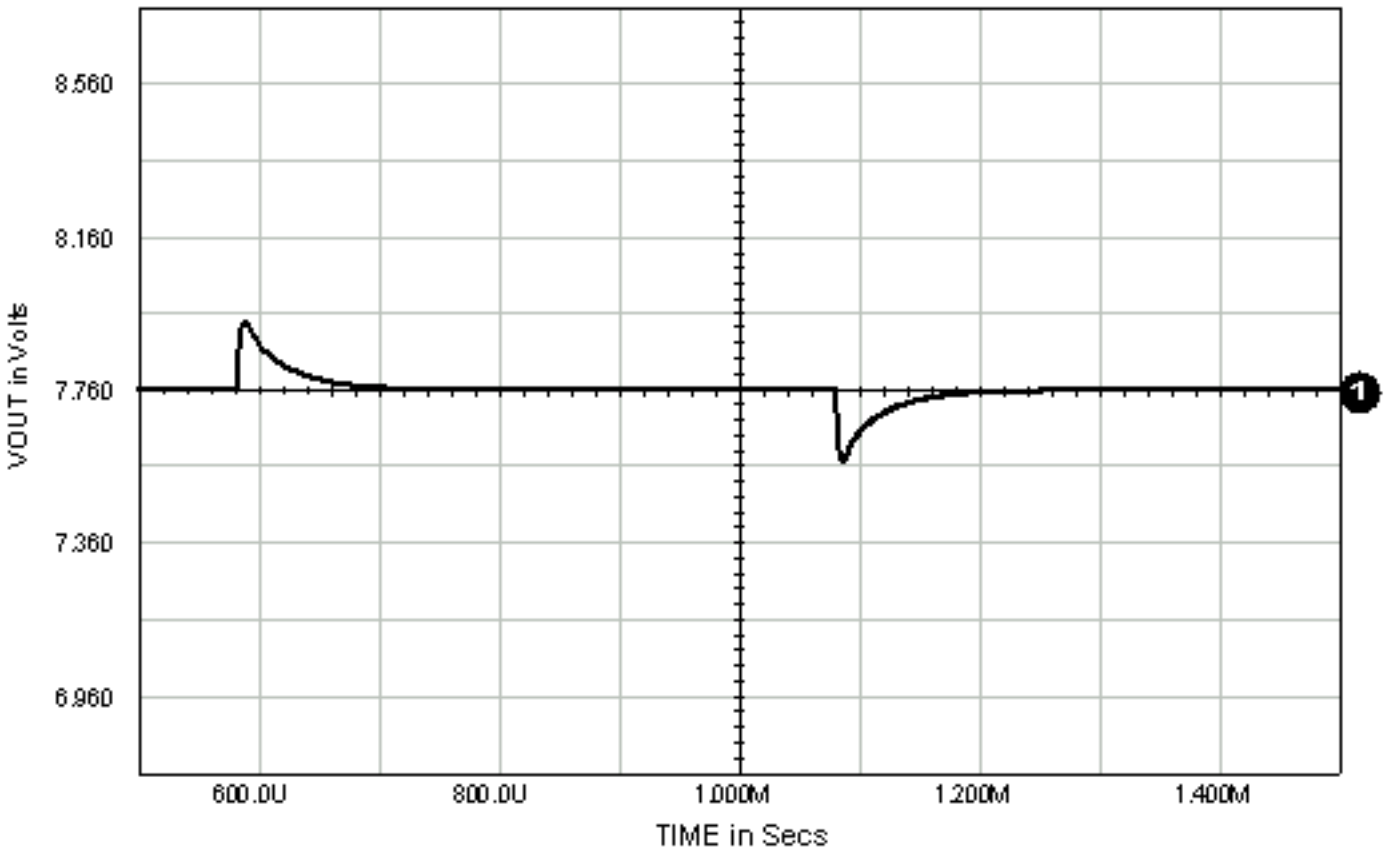

Tek Stop: 500kS/s
145 Acqs
2→
1→
Ch1 500mV∿ Ch2 200mV∿ M 100µs Ch1 ∫ 50mV
27 Feb 1998
09:30:18

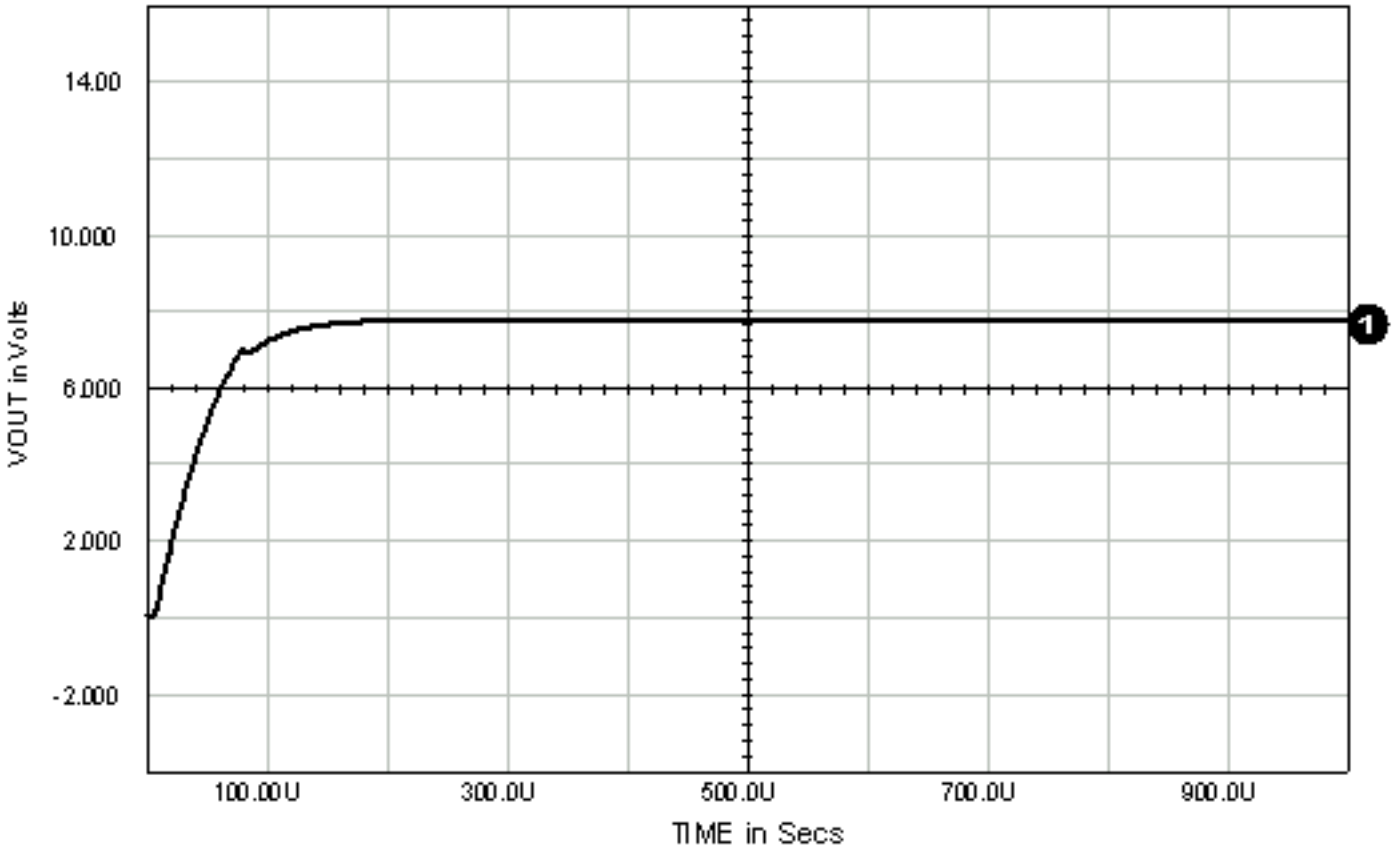

8.560
8.160
7.760
7.360
6.960
VOUT in Volts
600.0U
800.0U
1.000M
1.200M
1.400M
TIME in Secs
1


R9
5M
3
694N
C2
10U
C5
.1U
X8
AEI150
6
8
V(8)
VOUT
10.00
694N
V2
10
R5
9.77K
5
4
R6
10
R10
8.2
18.0
3.08
V1
18
R1
.978K
R2
2.65K
C1
4.7N
2
1
2.00
773M
R3
5.56K
X1
TL431
11
7
773M
1.14M


R4
2.64K


40.00
20.00
0
-20.00
-40.00
GAIN in Volts
80.00
40.00
0
-40.00
-80.00
PHASE in Deg
1K
10K
100K
FREQUENCY in Hz
96.1 degrees, 47.1 dB, 5.73 KHz
1
2

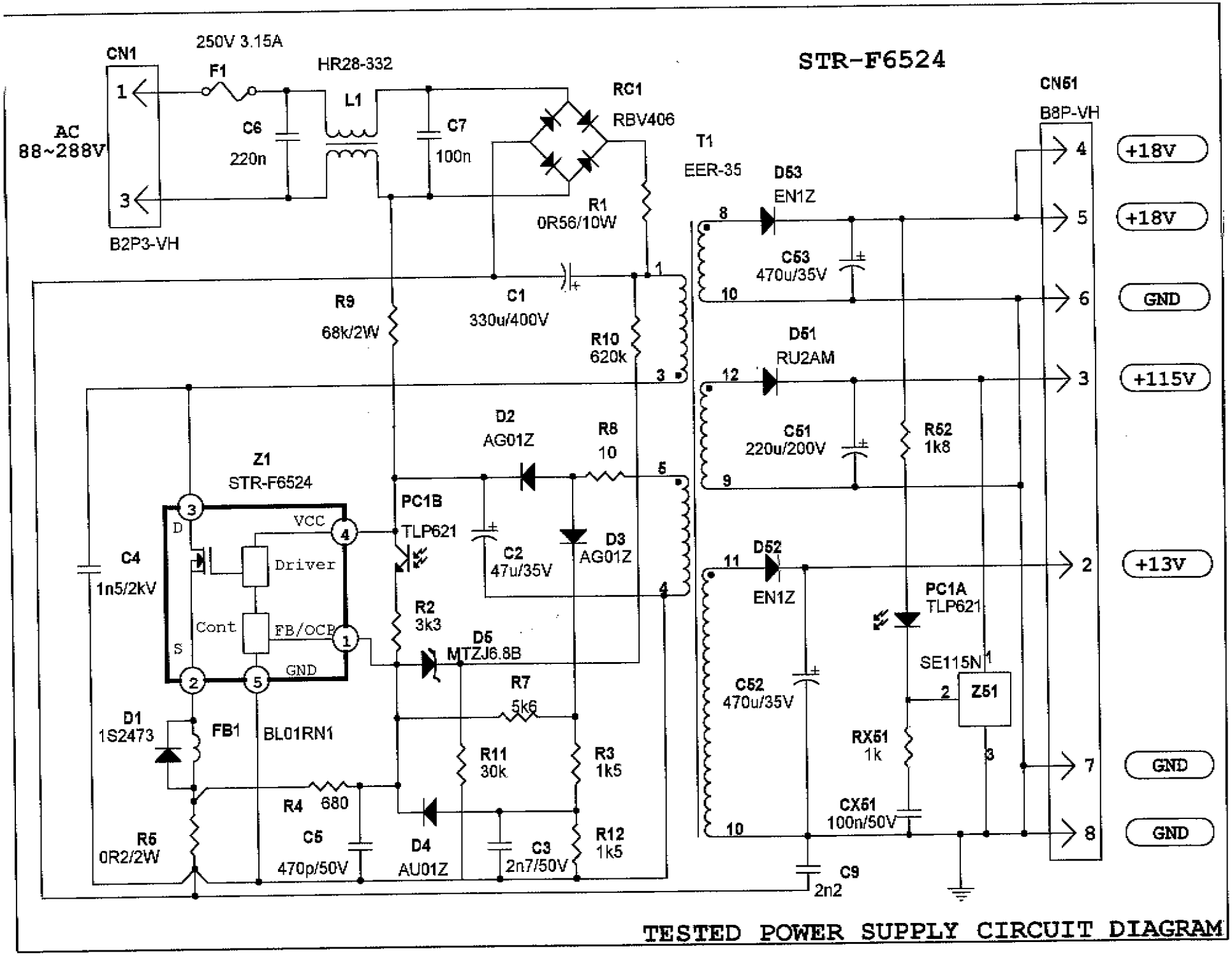

8.560
8.160
7.760
7.360
6.960
VOUT in Volts
600.0U
800.0U
1.000M
1.200M
1.400M
TIME in Secs
1


14.00
10.000
6.000
2.000
-2.000
VOUT in Volts
100.00U
300.0U
500.0U
700.0U
900.0U
TIME in Secs
1

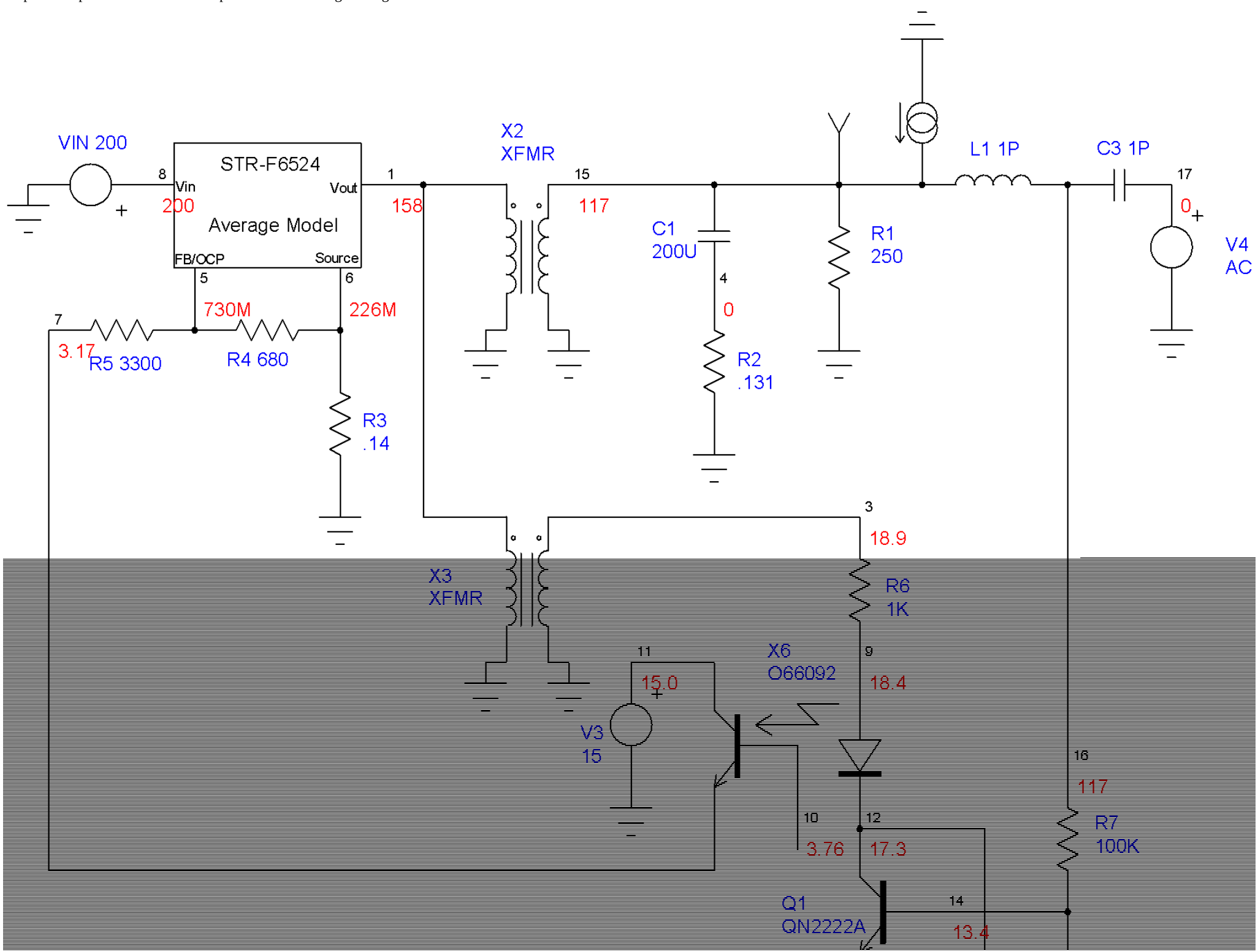
5
Electronic Load Circuits

Power conversion circuits can be designed to provide large amounts of output power. In order to test these high power output circuits, a load must be created that can safely dissipate the maximum power of the power converter. There are two ways to dissipate this power. Using high wattage rating resistors is a typical solution. However, by definition, these resistors are large and bulky. If the designer wishes to test the power converter at different loads, more resistors must be purchased. When the power dissipation required is very large (> 200W), power resistors required to dissipate this load can become unwieldy.

The second alternative is an electronic load. This device is a circuit that has a controllable switch (typically a Darlington configured pair of bipolar transistors or a MOSFET) that can be modulated to conduct any level of current the user desires. An example of an electronic load circuit is presented in this chapter. The electronic load will be constructed piece by piece and tested separately. When all the pieces are constructed and simulated, the whole sum of the electronic load can be assembled and tested as a unit.

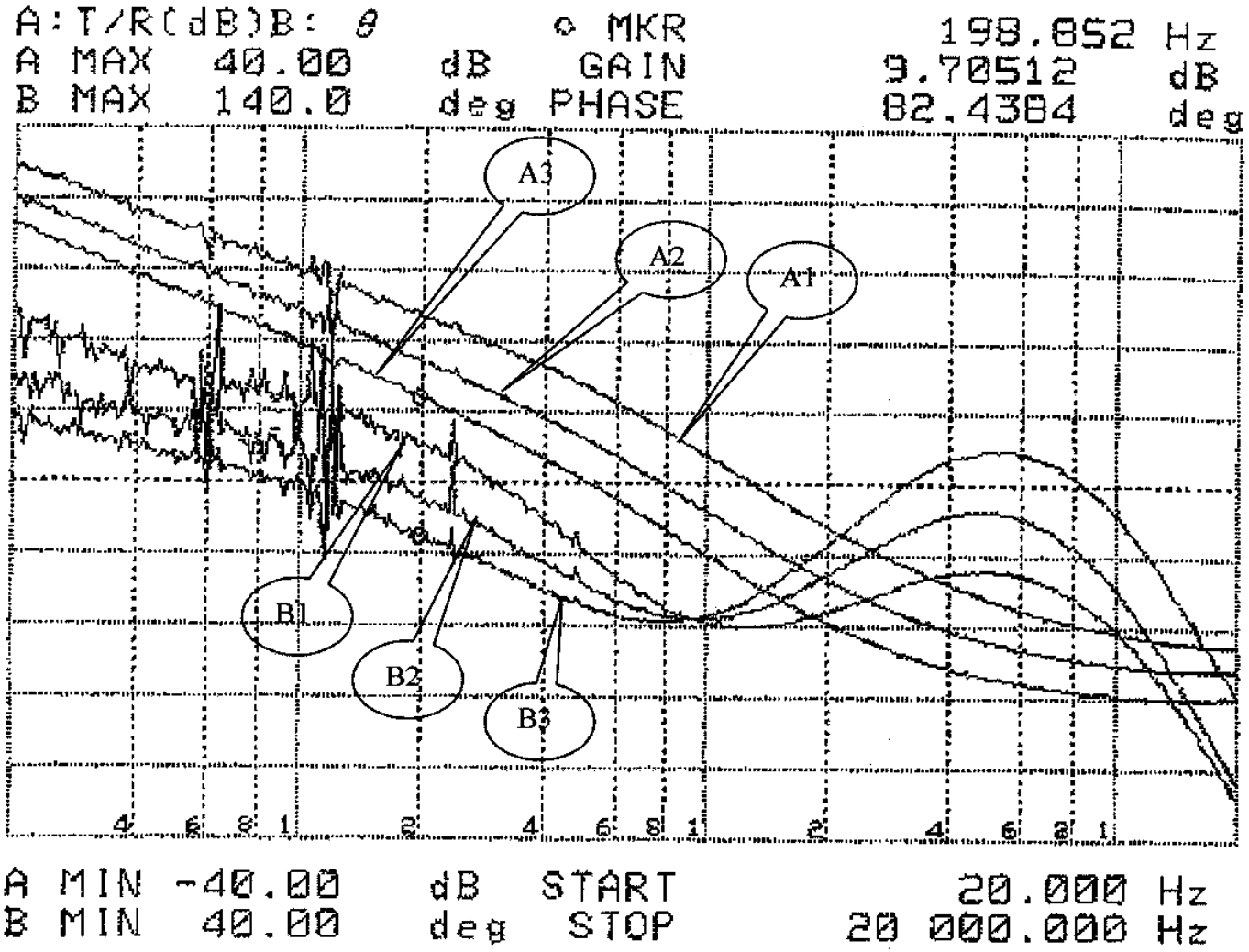


11


VIN 200
STR-F6524
8
Vin
200
Vout
1
158
Average Model
FB/OCP
5
Source
6
730M
226M
7
3.17
R5 3300
R4 680
R3
.14
X2
XFMR
15
117
C1
200U
4
0
R2
.131
R1
250
L1 1P
C3 1P
17
0
V4
AC
3
18.9
X3
XFMR
R6
1K
X6
O66092
11
15.0
9
18.4
V3
15
16
117
R7
100K
10
3.76
12
17.3
Q1
QN2222A
14
13.4


13
12.8
R8
13K
R9
1K
D1
Z04AZ13
2
17.3
C2
.1U

GAIN- PHASE CHARACTERISTICS OF THE POWER SUPPLY TEST BOARD USING STRF-6524



TEST CONDITIONS

INPUT VOLTAGE	AC85V	(MIN LINE)

OUTPUT VOLTAGE/ CURRENT

115V DC/ 0.55A (MAX LOAD) Rload= 209 Ohm

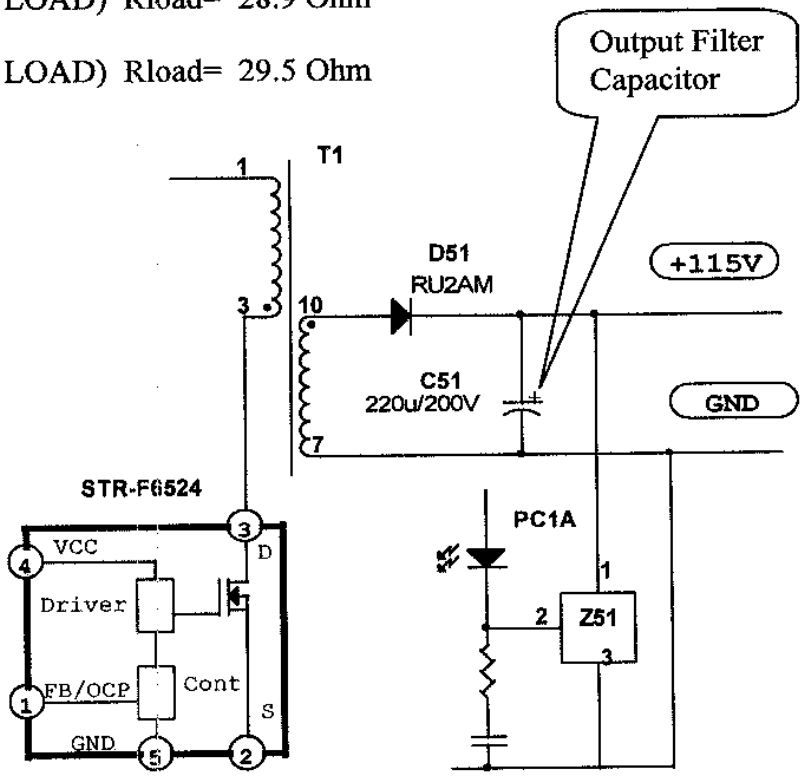
17.3VDC/ 0.6A (MAX LOAD) Rload= 28.9 Ohm

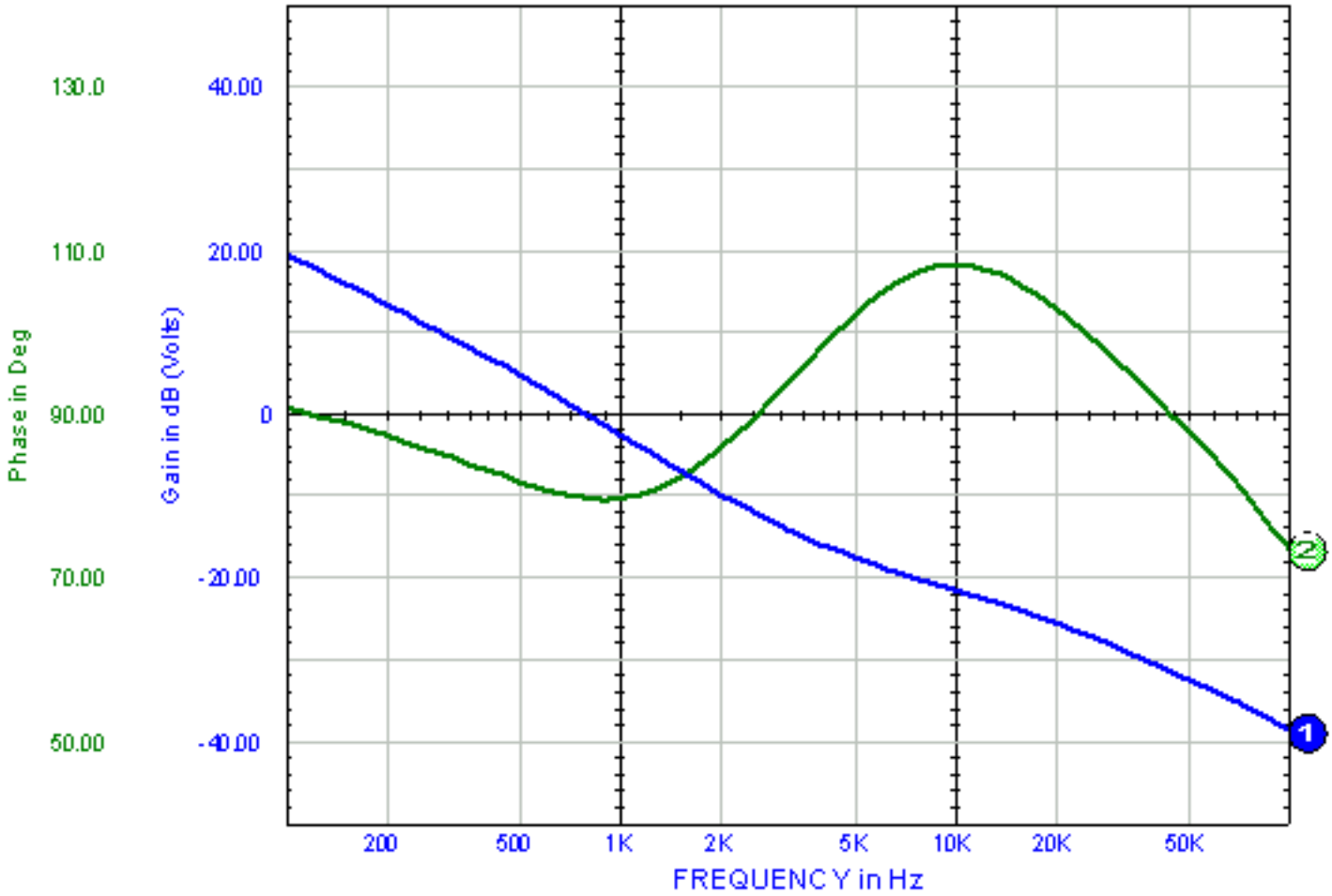
14.7VDC/ 0.5A (MAX LOAD) Rload= 29.5 Ohm

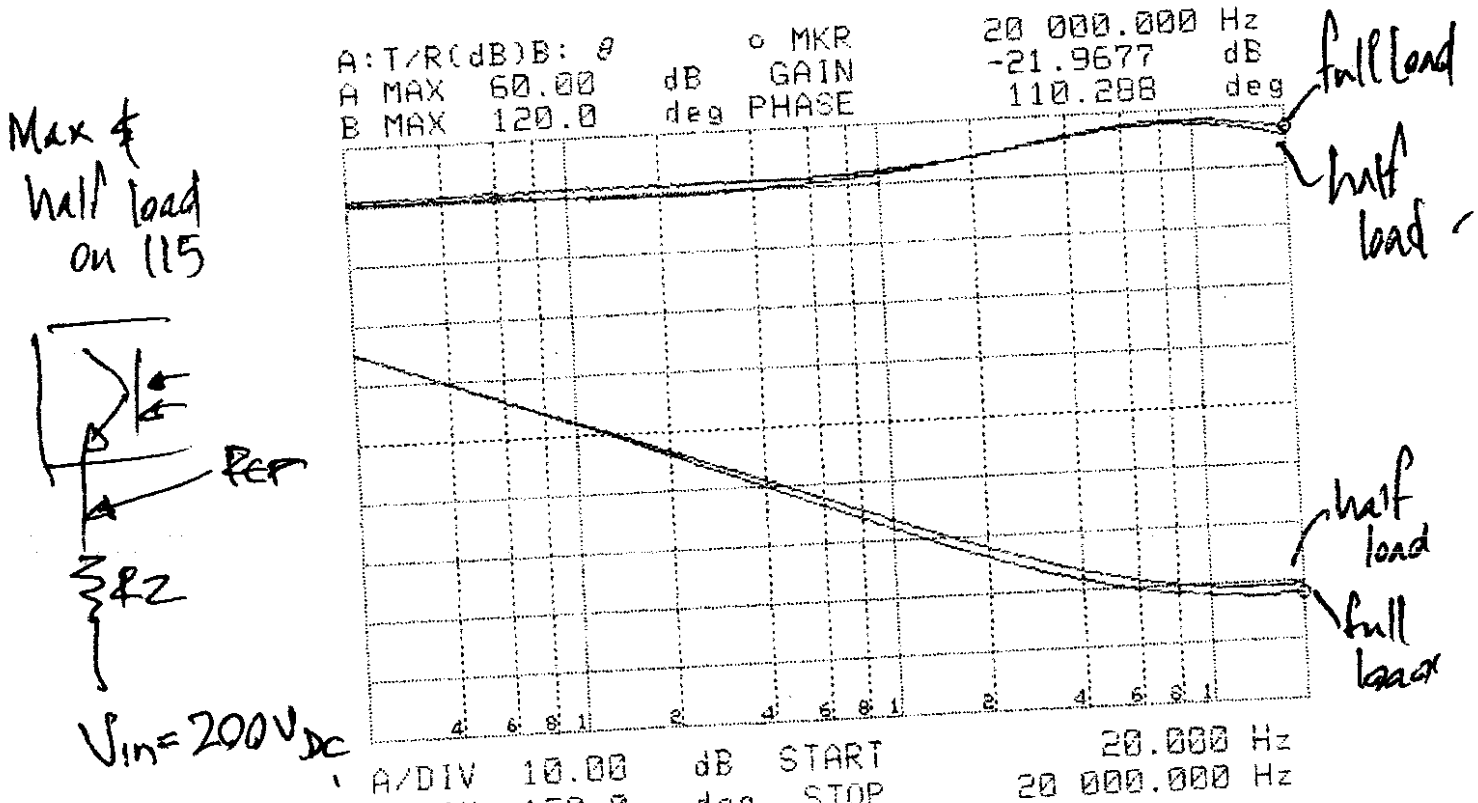
OUTPUT FILTER CAPACITOR C51

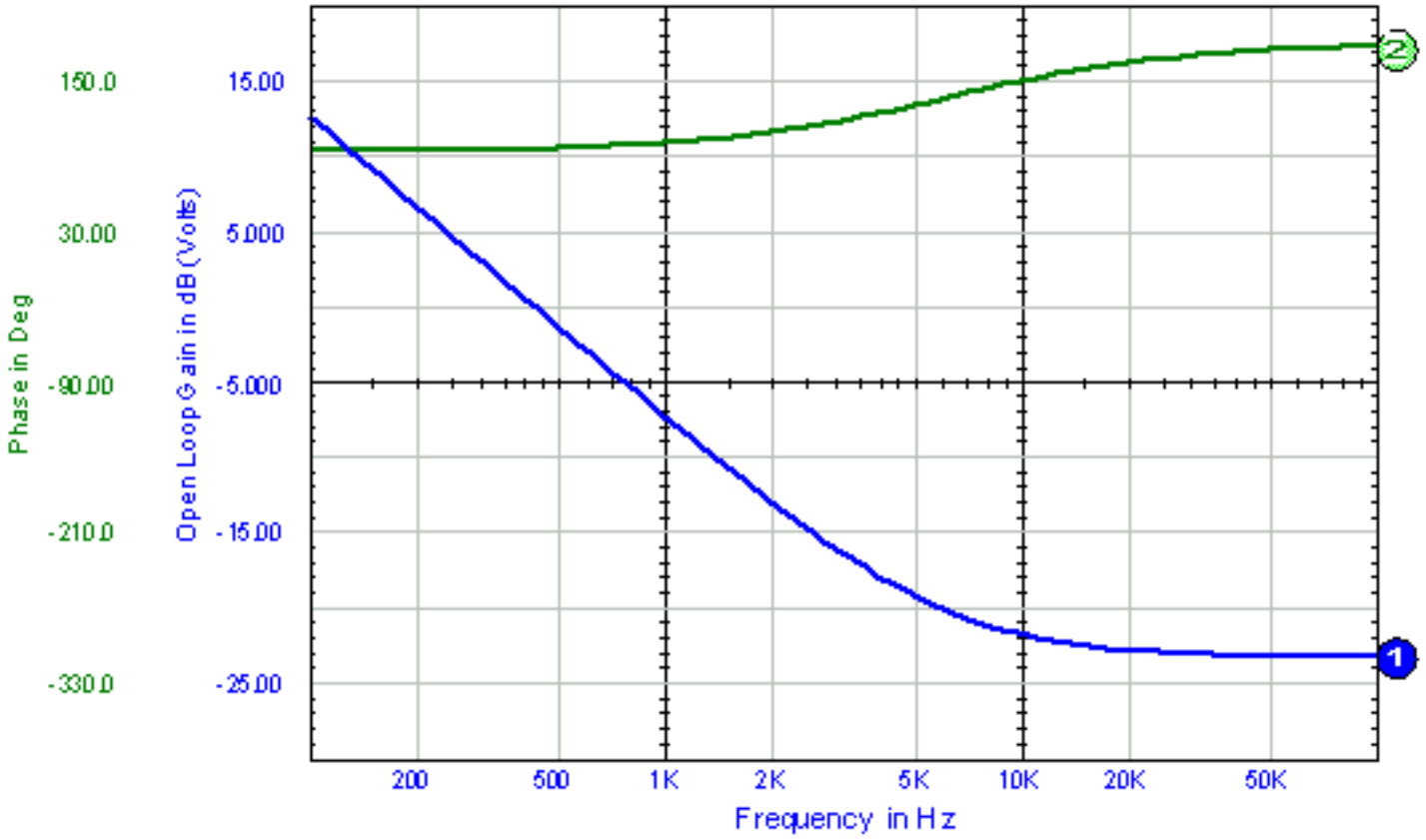
1. A1,B1 - 110uF
2. A2,B2 - 220uF
3. A3,B3 - 440uF

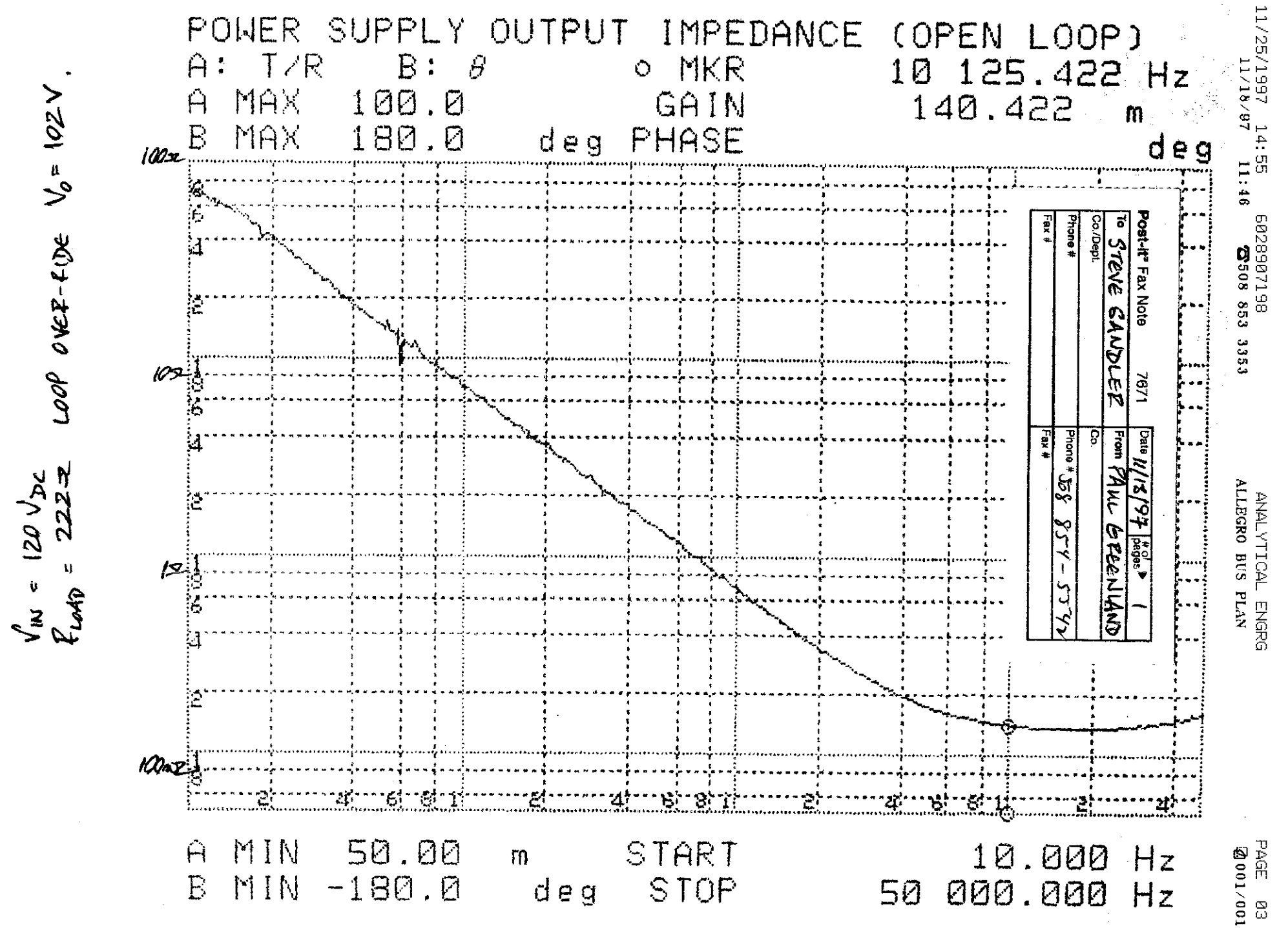
SIMPLIFIED POWER SUPPLY SCHEMATIC

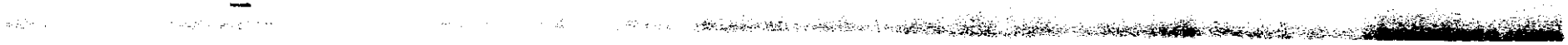


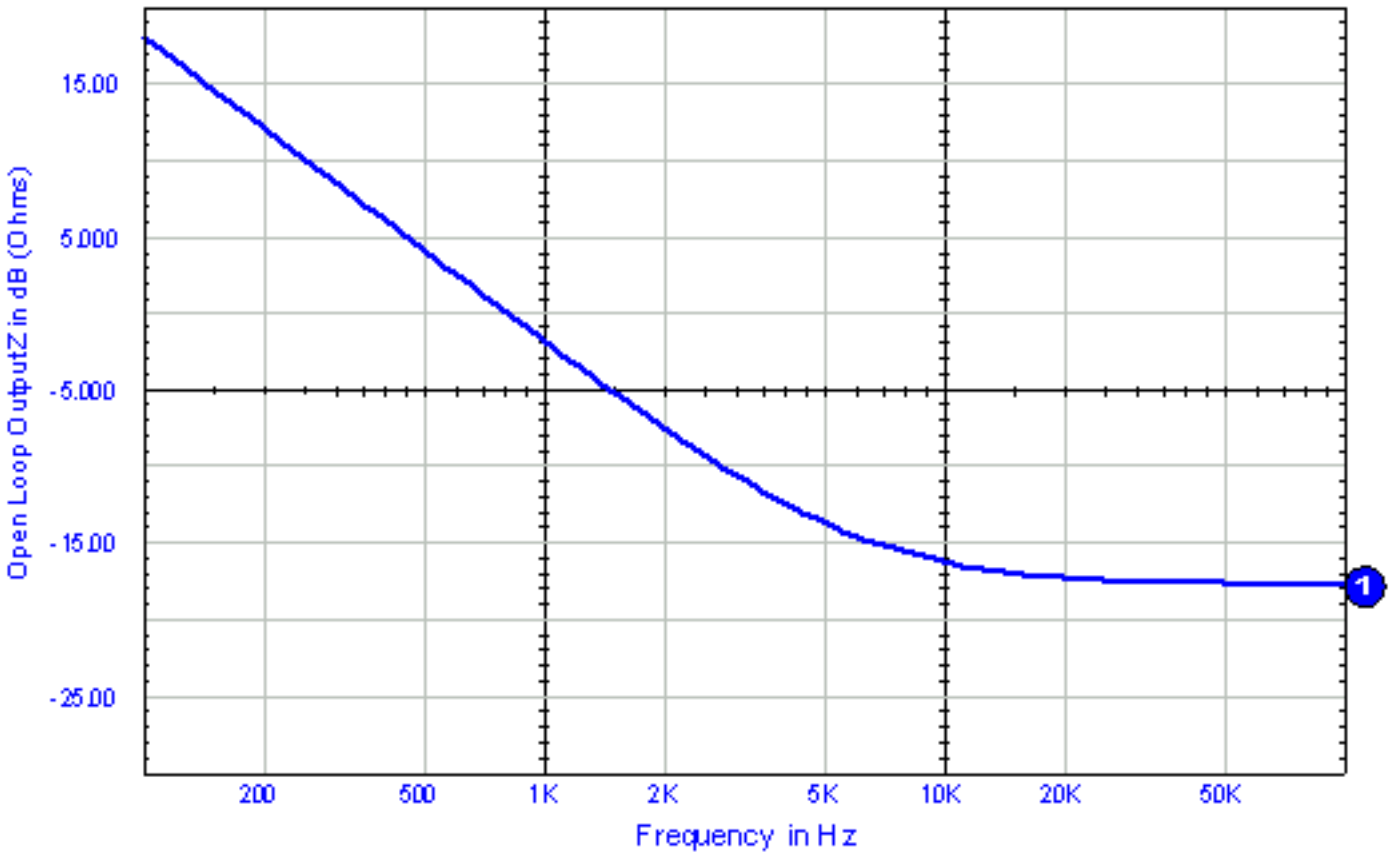

130.0
110.0
90.00
70.00
50.00
Phase in Deg
40.00
20.00
0
-20.00
-40.00
Gain in dB (Volts)
200
500
1K
2K
5K
10K
20K
50K
FREQUENCY in Hz
1
2

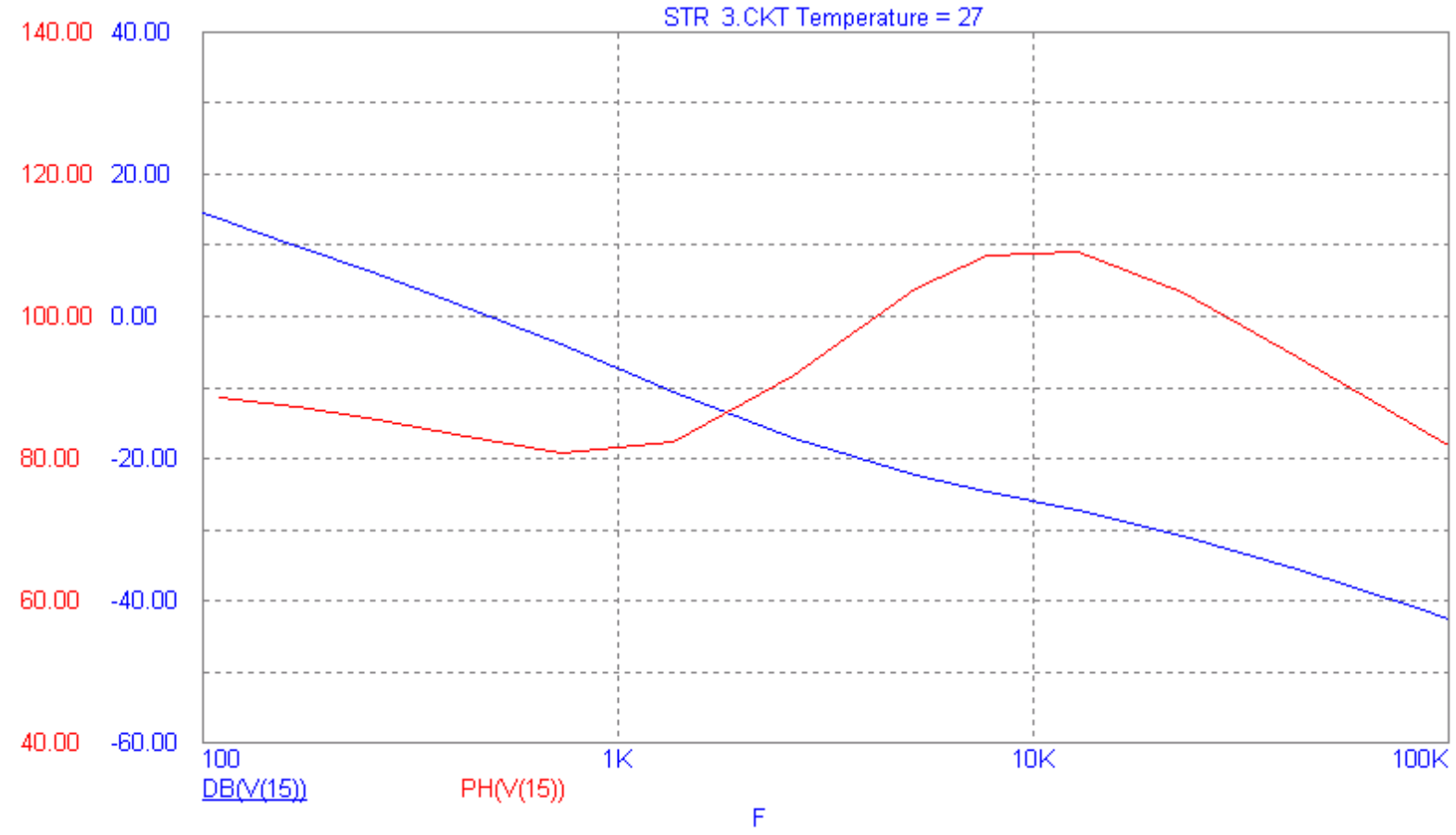


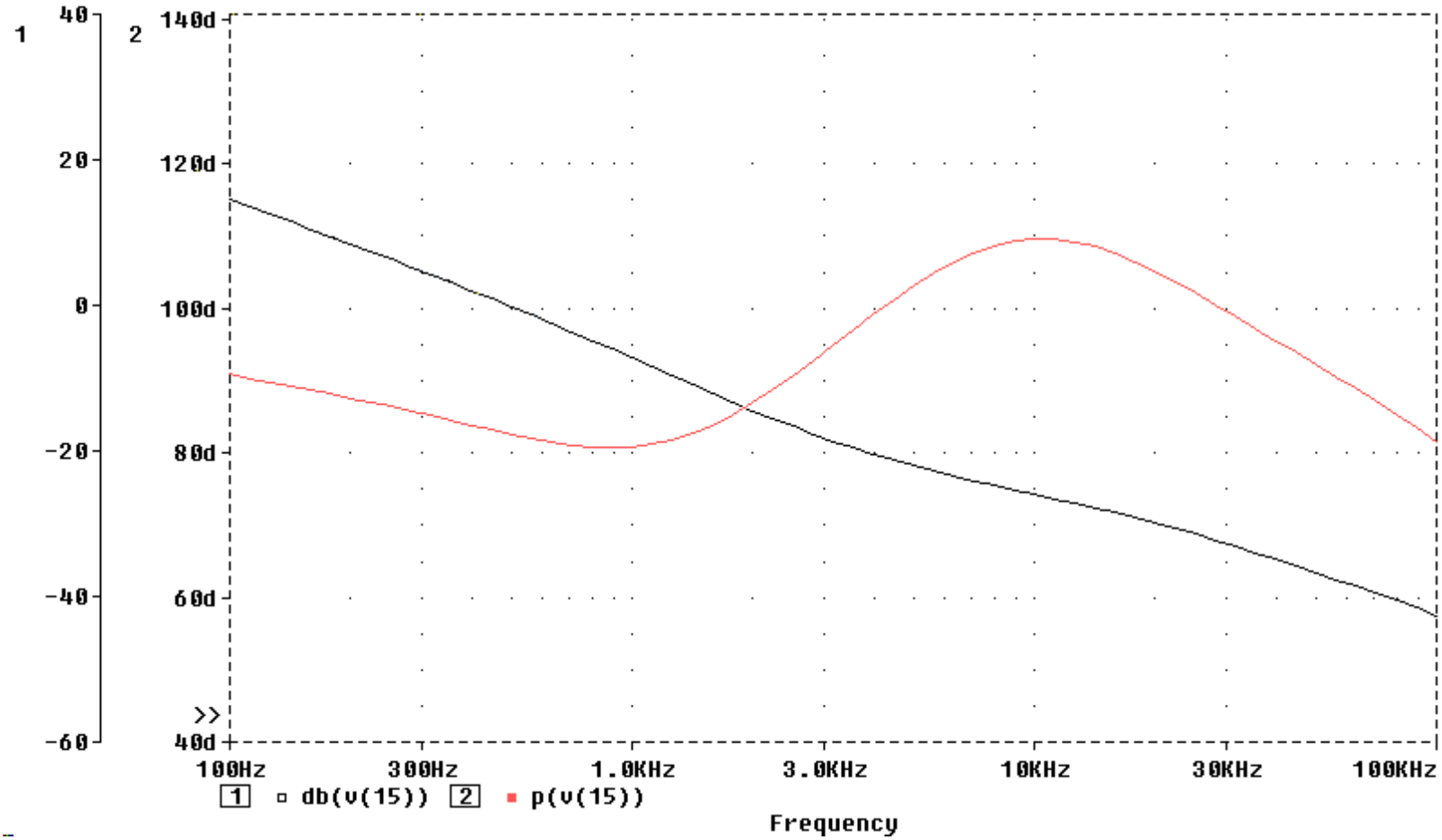

150.0
30.00
-90.00
-210.0
-330.0
Phase in Deg
15.00
5.000
-5.000
-15.00
-25.00
Open Loop Gain in dB (Volts)
200
500
1K
2K
5K
10K
20K
50K
Frequency in Hz
1
2


POWER SUPPLY OUTPUT IMPEDANCE (OPEN LOOP)
A: T/R B: θ ○ MKR 10 125.422 Hz
A MAX 100.0 GAIN 140.422 m
B MAX 180.0 deg PHASE
deg
100Ω
10Ω
1Ω
100mΩ
A MIN 50.00 m START 10.000 Hz
B MIN -180.0 deg STOP 50 000.000 Hz
V_{IN} = 120 V_{DC}
R_{LOAD} = 222Ω LOOP OVER-RIDE V_O = 102 V.
Post-it® Fax Note 7671
To STEVE SANDLER
From PAUL GREENLAND
Co.
Phone # 508 853-3352
Fax #
Date 11/18/97 # of pages ▶ 1
Co/Dept.
Phone #
Fax #
11/25/1997 14:55 6028907198
11/18/97 11:46 ☎508 853 3353
ANALYTICAL ENGRG
ALLEGRO BUS PLAN
PAGE 03
001/001




15.00
5.000
-5.000
-15.00
-25.00
Open Loop OutputZ in dB (Ohms)
200
500
1K
2K
5K
10K
20K
50K
Frequency in Hz
1


STR 3.CKT Temperature = 27
140.00
120.00
100.00
80.00
60.00
40.00
40.00
20.00
0.00
-20.00
-40.00
-60.00
100
1K
10K
100K
DB(V(15))
PH(V(15))
F


1
2
40
20
0
-20
-40
-60
140d
120d
100d
80d
60d
40d
>>
100Hz
300Hz
1.0KHz
3.0KHz
10KHz
30KHz
100KHz
1 db(v(15)) 2 p(v(15))
Frequency

#17: Power Section of an Electronic Load

The power section in this electronic load will be a power N-Channel Mosfet. This design utilizes an IRF250 manufactured by International Rectifier® . If a substitute part is used, pick a Mosfet that has the power, drain to source voltage, and current rating required for your range, and try to minimize drain to source on resistance. The schematic of the power Mosfet and drive circuitry is shown in Figure 17-1.

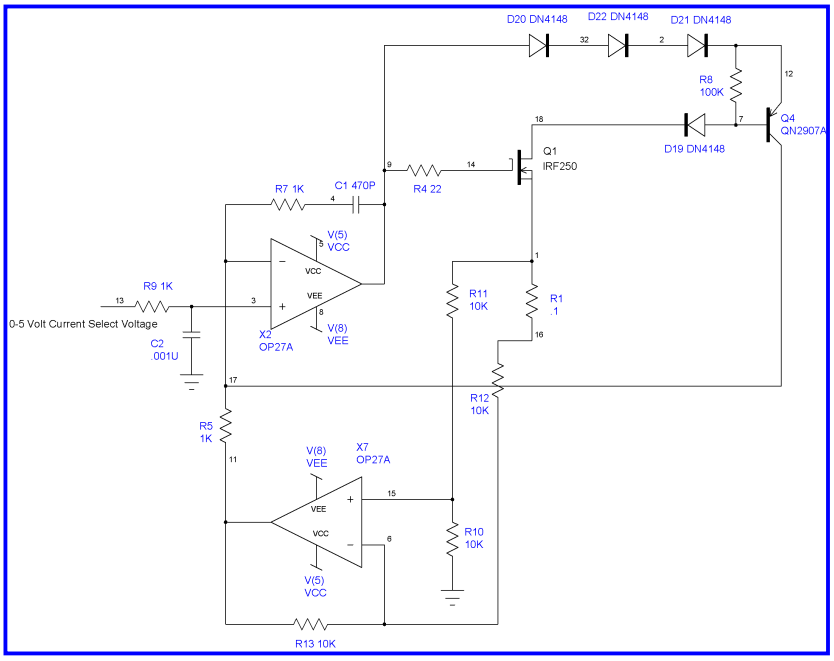


Figure 17-1: Schematic of Electronic Load Power stage

- Breadboard Tip: Although SPICE does not need bypass capacitors, breadboard circuits do! .01uF capacitors from VCC and VEE to ground may be necessary to extract full performance from this circuit. The supply for the Operational Amplifier should be > ± 10v (The breadboard in this example used ±15 volts). Also, if high currents are being supplied by the electronic load, make sure the Mosfet is heat sunk or air cooled and also make sure the 0.1 ohm sense resistor has a wattage rating appropriate to the current through it.

The connections for the output power supply under test are shown in Figure 17-1

as **+ Load** and **- Load**. Load current passes through the 0.1 ohm sense resistor (R1) and is sensed by an operational amplifier (X7) operating as a differential amplifier (R11, R12, R10, R13). The differential amplifier creates a voltage representation of the current, which is sensed by the inverting terminal of another operational amplifier (X2 via R5). This signal is compared to a 0-5 volt reference corresponding to 0-5 Amps of current (sensed by the non-inverting terminal of X2). An RC filter is used to filter noise spikes on the reference voltage (R9 and C2). The output of X2 provides gate voltage to the power Mosfet (Q1). R4 is a gate resistor used to limit the current in the gate and to avoid any self oscillations of the Mosfet due to noise. Components R7 and C1 provide compensation for the control loop.

One nice bonus feature of this circuit is provided by the 1N4148 diodes (D19-D22) and the 2N2907A PNP transistor (Q4). This circuit serves to limit inrush current (and subsequent overshoot) of the output power supply under test when the electronic load is first activated. When there is no voltage on the output load, the control operational amplifier is usually railed high. The diode circuit clamps this output at a voltage just beneath the turn on of the Mosfet (close to 2.4 volts) in order to prevent this occurrence. When the power supply under test is connected (and exceeds the 2.4 volt clamp level), the regulation swing of the output of the Op-amp is much less than if the Op-amp had been railed, allowing for a much faster response and a controlled turn on.

The SPICE transient model for this circuit is shown in Figure 17-2. Notice the additional 10 mOhm resistor (R14) that exists on the SPICE model and not our schematic. This is inserted in order to partially represent the characteristics of the cabling. There can be an inductive part to this as well, however, it is important to note that the cabling will have an effect on the slew rate of the current regulation. The SPICE AC model is shown in Figure 17-3.

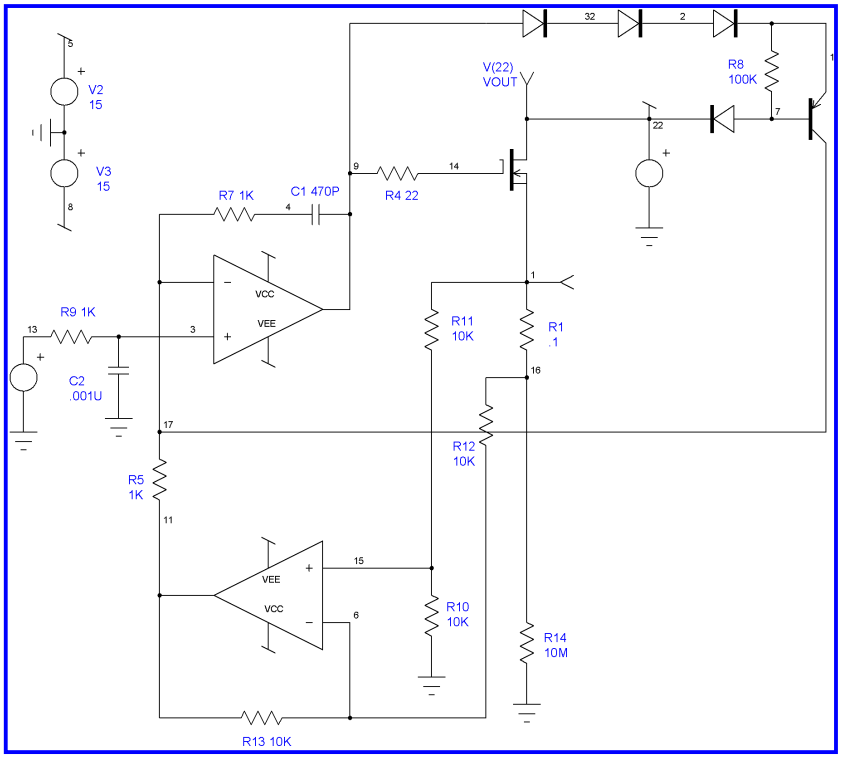


Figure 17-2: SPICE Schematic of Electronic Load Power stage (transient)

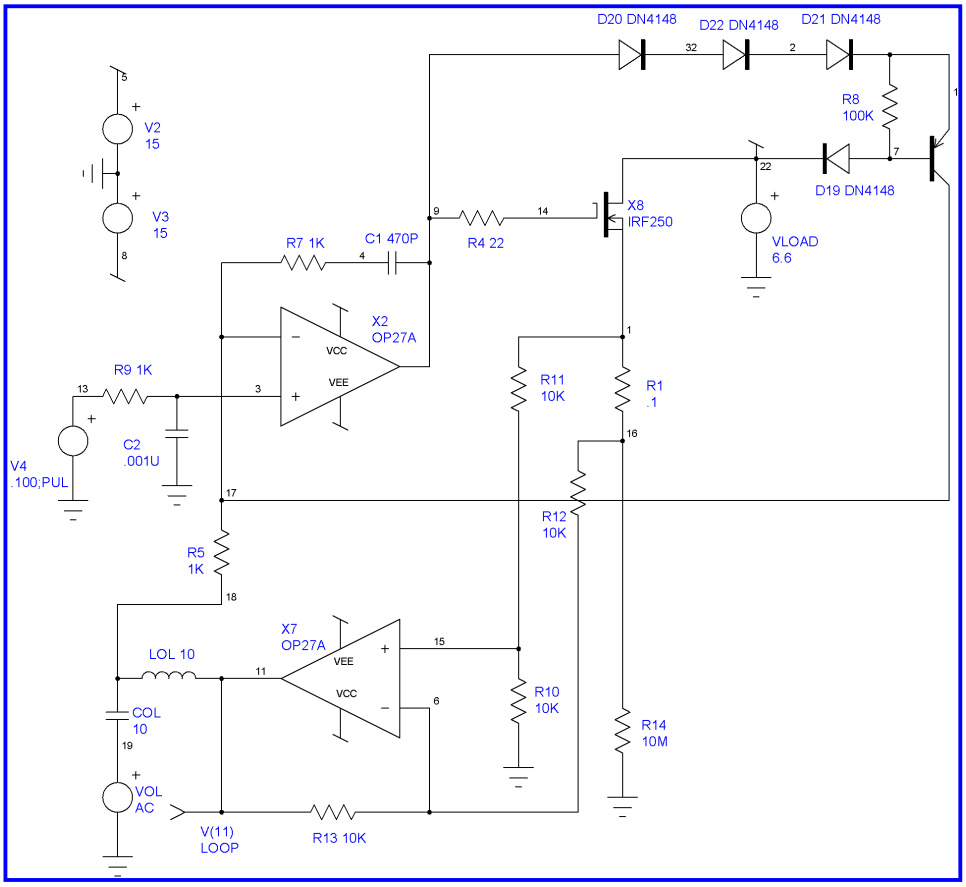


Figure 17-3: SPICE Schematic of Electronic Load Power stage (AC)

There were three measurements taken of the breadboard in order to correlate to the SPICE results. Figure 17-4A is a plot of the turn on of the current regulator. Figure 17-5A is a plot of the load current response to a stepped reference voltage. Figure 17-6A is a plot of the current regulator loop. The IsSpice results of these measurements are shown in Figures 17-4B, 17-5B, and 17-6B.

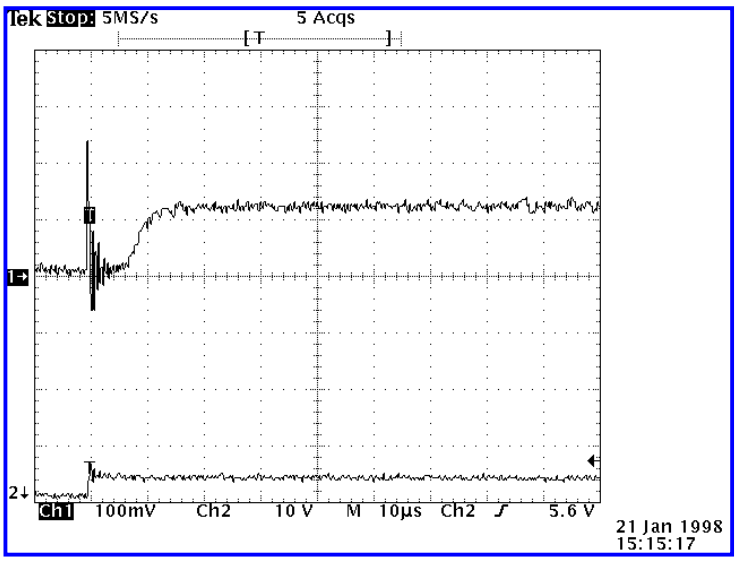


Figure 17-4A: Breadboard turn on plot (Top-current 1v=1A, Bottom-Drain voltage of Fet)

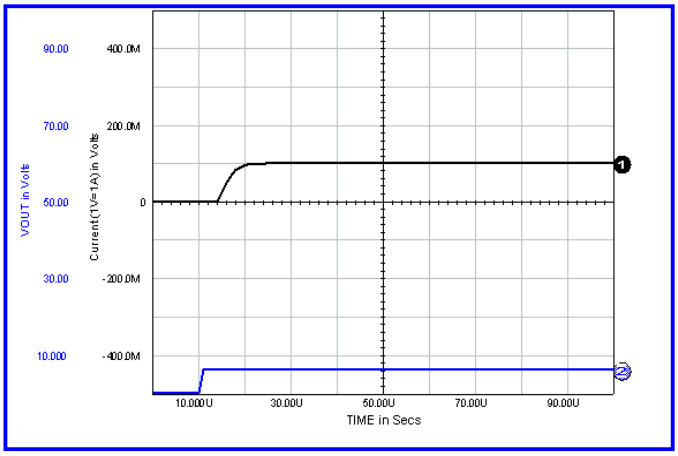


Figure 17-4B: IsSpice turn on plot

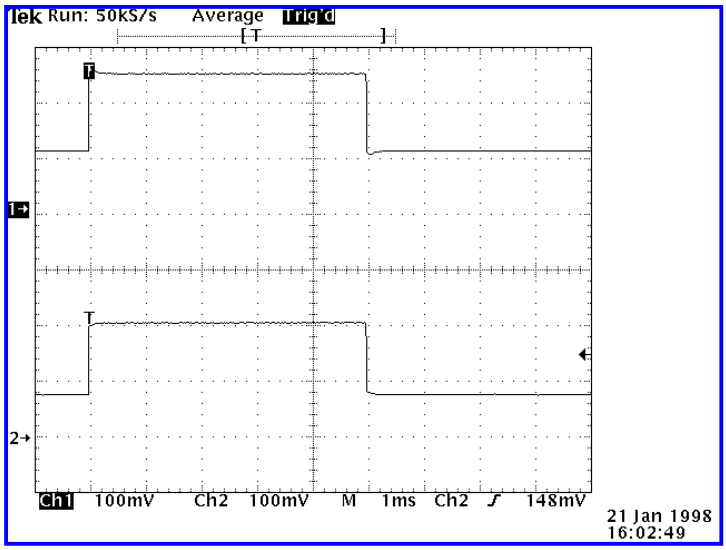


Figure 17-5A: Breadboard step response (Bottom-current 1v=1A, Top-select voltage step)

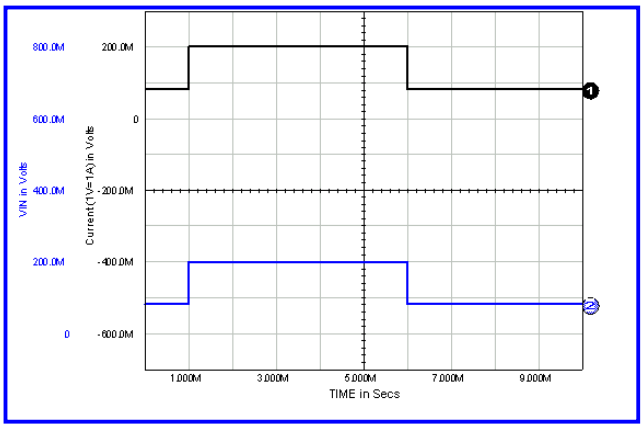


Figure 17-5B: IsSpice Current Step response

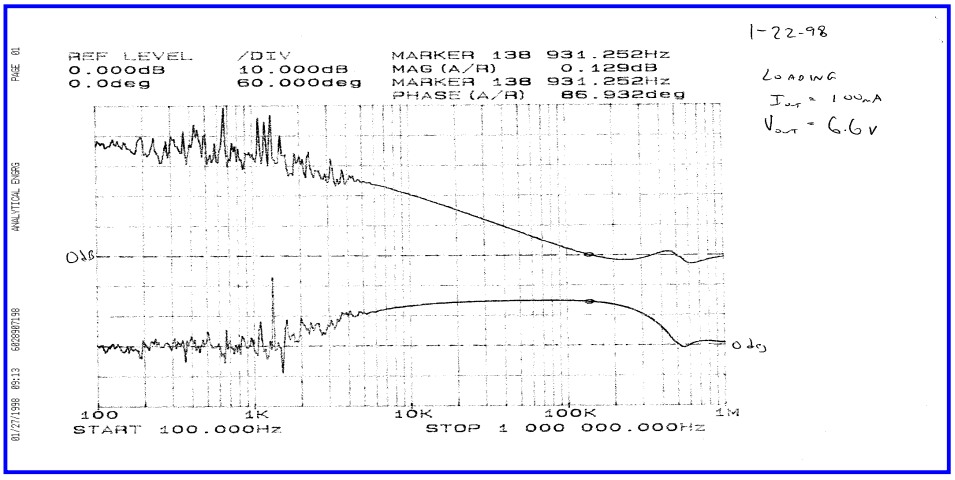


Figure 17-6A: Breadboard current regulator bode plot

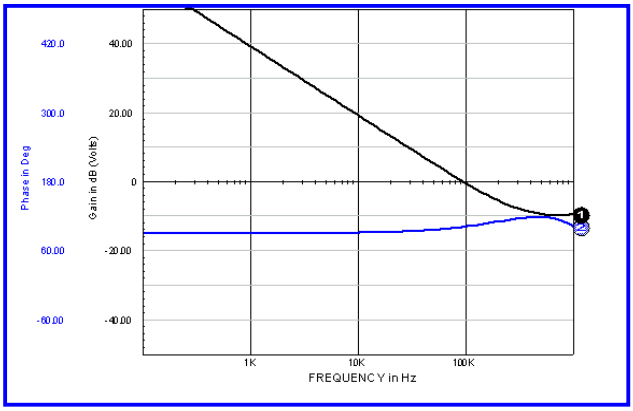


Figure 17-6B: IsSpice Current loop bode plot

Equivalent models were used from Pspice and Microcap. The results are shown in Figures 17-7 through 17-8. Note the IRF250 model was not available in the demo version of Pspice; the IRF150 was used as a substitute.

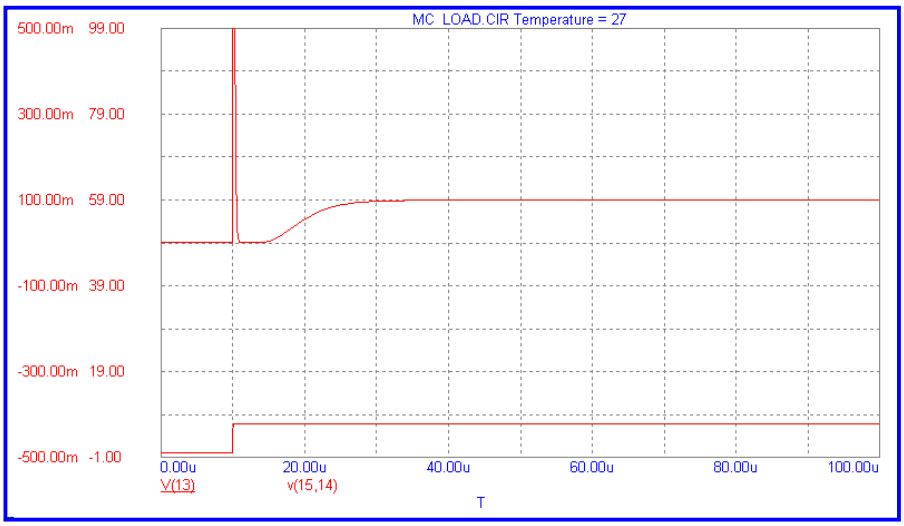


Figure 17-7A: Microcap turn on plot

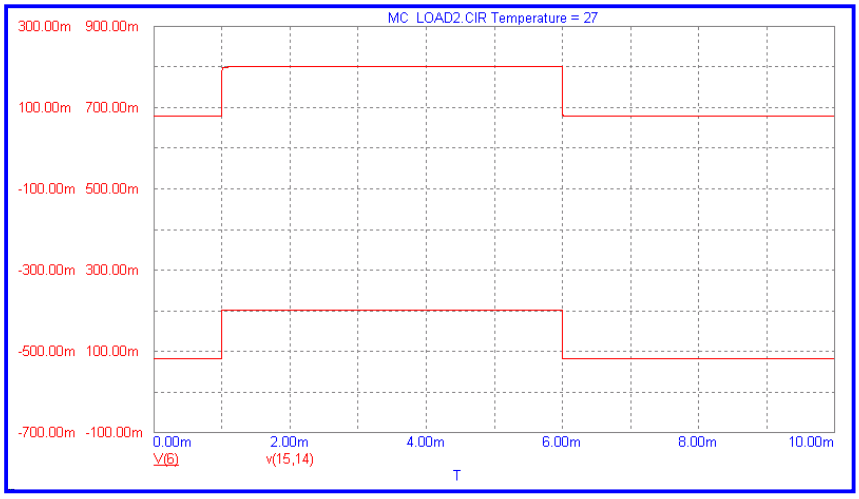


Figure 17-7B: Microcap current step response

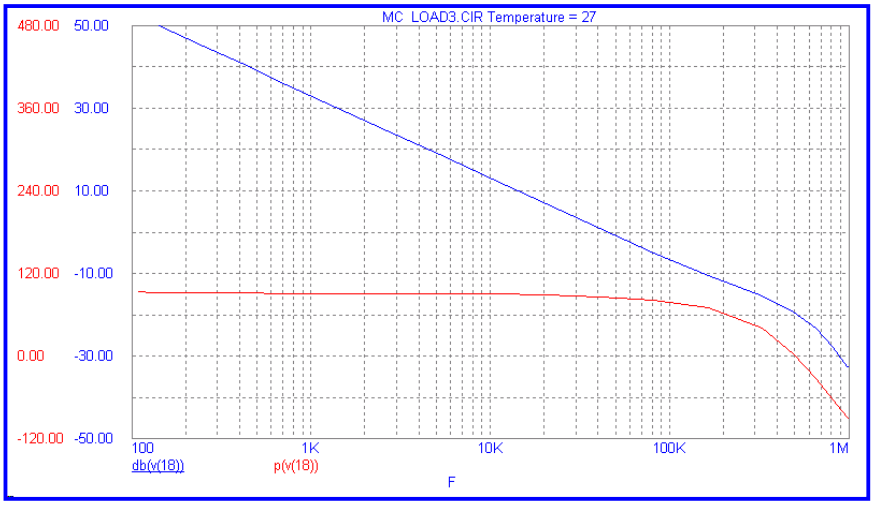


Figure 17-7C: Microcap current loop bode plot

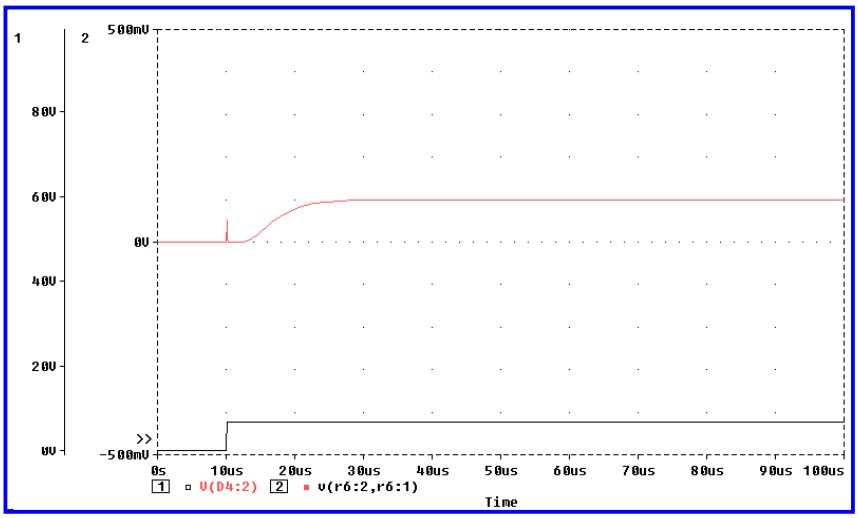


Figure 17-8A: Pspice turn on plot

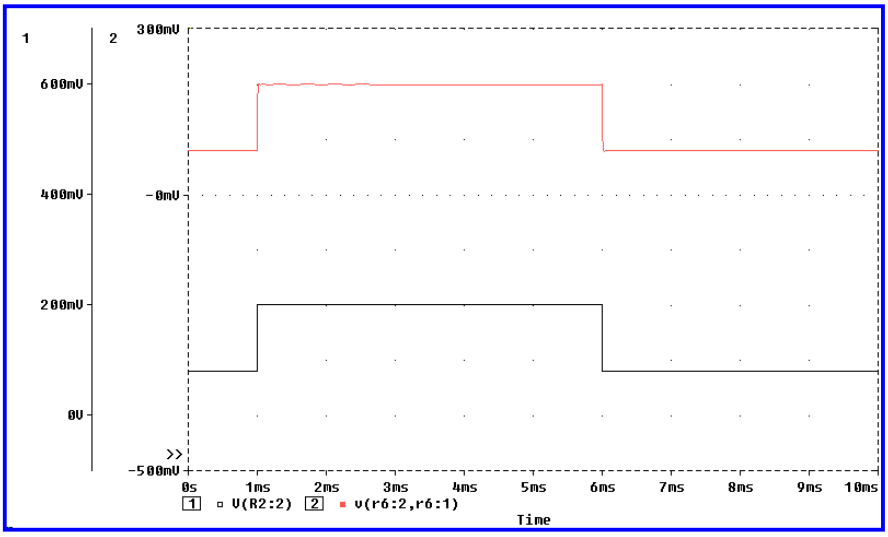


Figure 17-8B: Pspice current step response

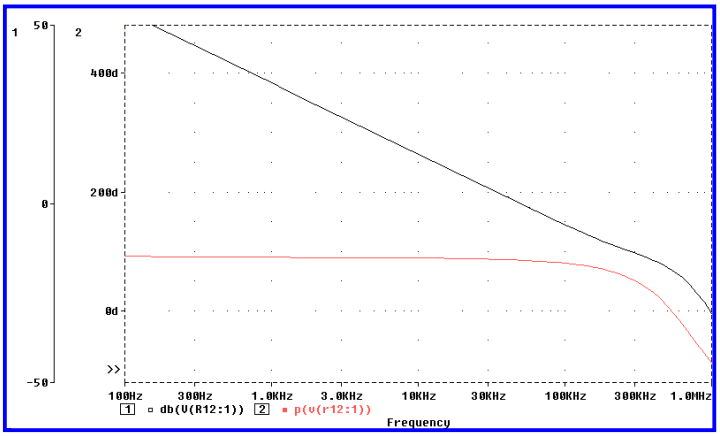


Figure 17-8C: Pspice current loop Bode plot

Examining the results of the SPICE simulations, it is noted all of the simulations show the slight current charging at the beginning of the turn on plot to some degree. This charging is due to the drain to source capacitance of the MOSFET model used in the simulation. Since all the models are slightly different, the results are not unexpected. Also as a result of the differences in the MOSFET models is the distribution of the bode plots. A summary of the phase margin and the crossover frequency of each of the simulators and the breadboard is shown in Table 17-1.

	Phase Margin	Crossover
Pspice	86 deg	49.29 Khz
Microcap	84 deg	44.73 Khz
IsSpice	100.4 deg	93.7 Khz
Breadboard	86 deg	139 Khz

Table 17-1: Bode plot results summary

The results in Table 17-1 suggest the loop characteristics are heavily dependant on the characteristics of the Mosfet.

Run Time Summary		
IsSpice v 7.6	Pspice v 6.3	Micro-Cap V v2
12.71 Sec	1.61 Sec	133.9 Sec
Advantages: no current overshoot at turn on, good loop characteristics		
Disadvantages: loop characteristics are heavily dependant on Mosfet selection		

Filenames: fetload1, fetload2, fetload3 (IsSpice) mc_load, mc_load2, mc_load3 (Micro-cap) fload1, fload2, fload3 (Pspice)

#18: Positive DC to Negative DC Comparator converter

One inconvenience associated with using operational amplifiers is the dual positive and negative power supplies that are frequently required. As a convenience, and to limit the power source of our electronic load box to one power supply, we will include the following circuit in our electronic load. The circuit takes a 15 volt DC signal and converts it to a -11 volt DC signal. The schematic for this circuit is shown in Figure 18-1. Note: Values shown are actual lab values of circuit. Standard resistor values shown in parentheses.

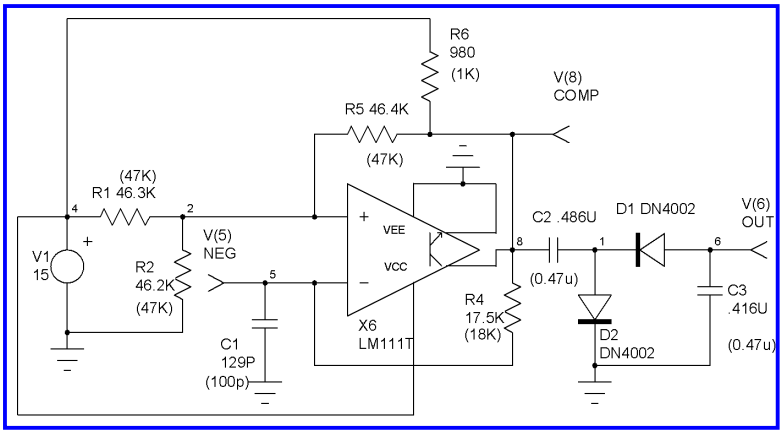


Figure 18-1: DC positive to DC negative converter schematic

The converter is powered by a external +15 volt DC supply. This voltage is divided down by R1 and R2 to form a 7.5 volt reference. The 7.5 volts on the non-inverting pin and the low voltage on the inverting pin causes the output to go to an open collector state (which is tied to the same +15 volt source through a 1K pull up resistor). This charges capacitor C1 through resistor R4. When the voltage on C1 exceeds the 7.5 volt reference, the output switches to a low state, adding the hysteresis resistor R5 into the divider. The new reference voltage is now 5 volts. The C1 capacitor now discharges through R4 and the oscillator is created. Capacitors C2 and C3, along with diodes D1 and D2 uses the square wave generated by the oscillator and rectifies it to a DC negative voltage.

The Breadboard plots of the waveforms at the inverting pin and the output pin of the LM111 are shown in Figure 18-2. The DC output voltage of the breadboard measured -13.68 volts. The Microcap waveforms are shown in Figure 18-3. The Microcap DC output voltage of the circuit measured -12.393 volts.

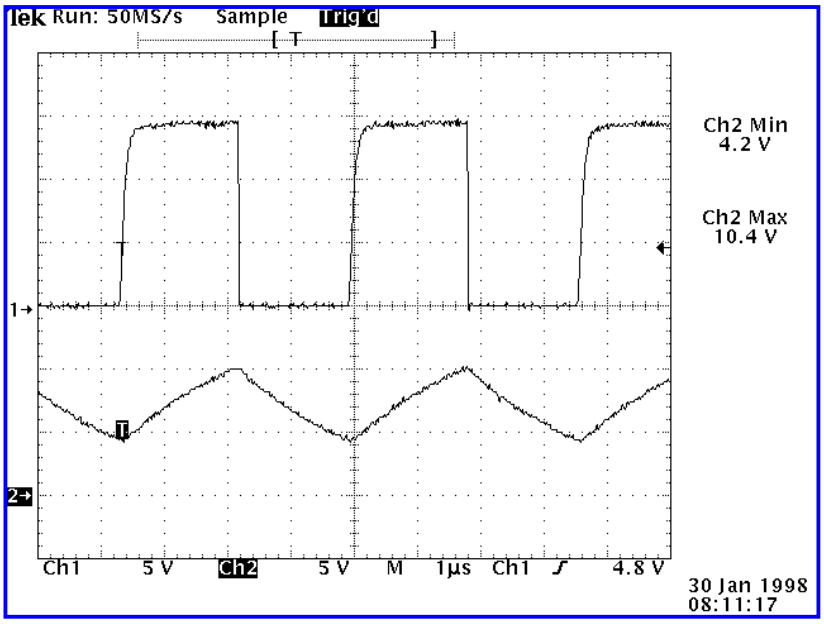


Figure 18-1: Breadboard waveforms (Top-pin 7 of LM111, Bottom - pin 3 of LM111)

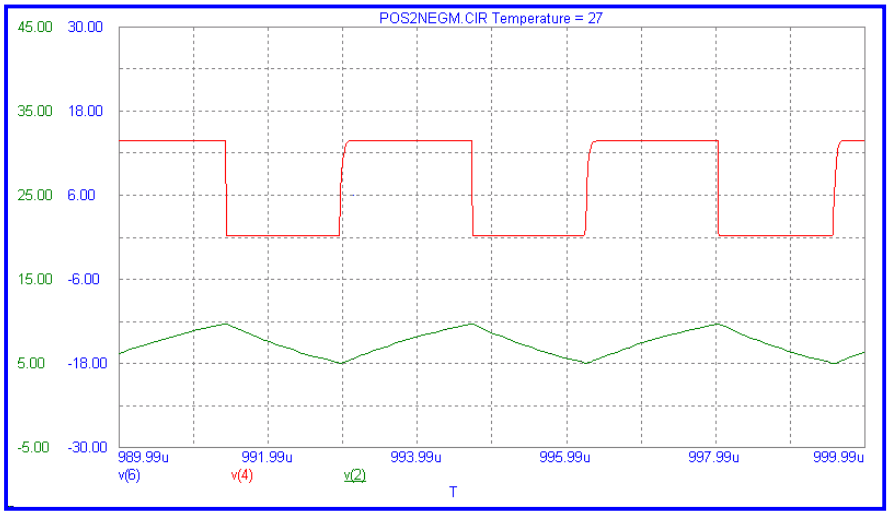


Figure 18-2: Microcap waveforms (Top-pin 7 of LM111, Bottom - pin 3 of LM111)

The positive DC to negative DC comparator converter was also simulated using Pspice and IsSpice. The inverting pin and output pin waveforms of the LM111 are shown in Figures 18-3 and 18-4. A summary of the DC output voltages of all three simulators compared to the breadboard results is shown in Table 18-1.

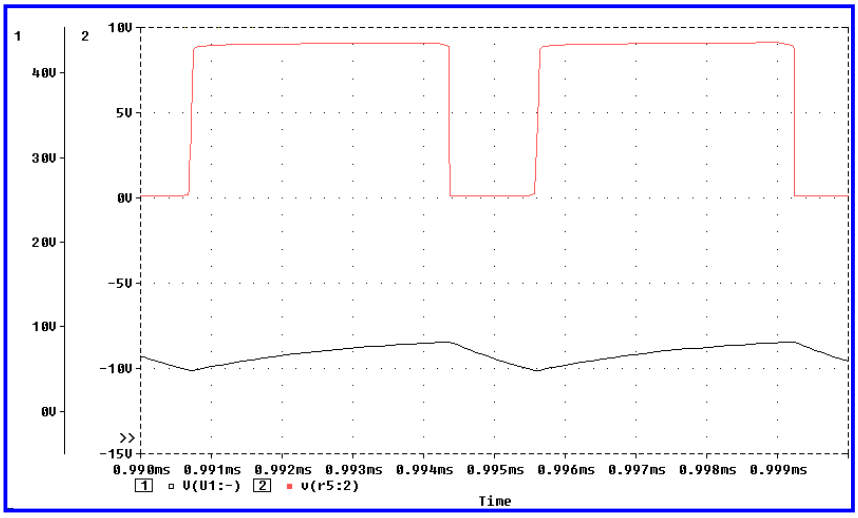


Figure 18-3: Pspice waveforms (Top-pin 7 of LM111, Bottom - pin 3 of LM111)

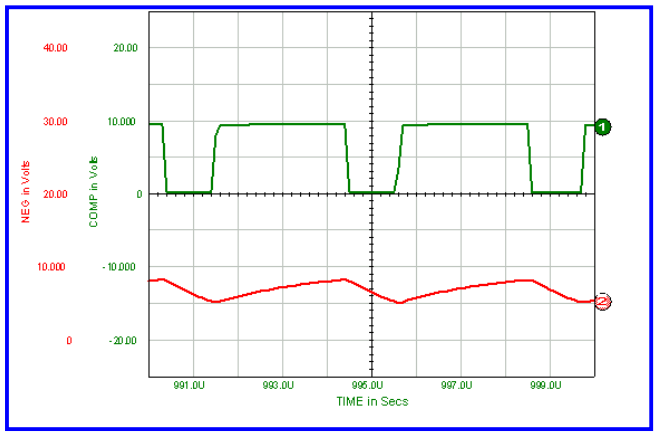


Figure 18-4: IsSpice waveforms (Top-pin 7 of LM111, Bottom - pin 3 of LM111)

	DC output voltage of circuit
Pspice	-11.000 Volts
Microcap	-12.393 Volts
IsSpice	-10.000 Volts
Breadboard	-13.68 Volts

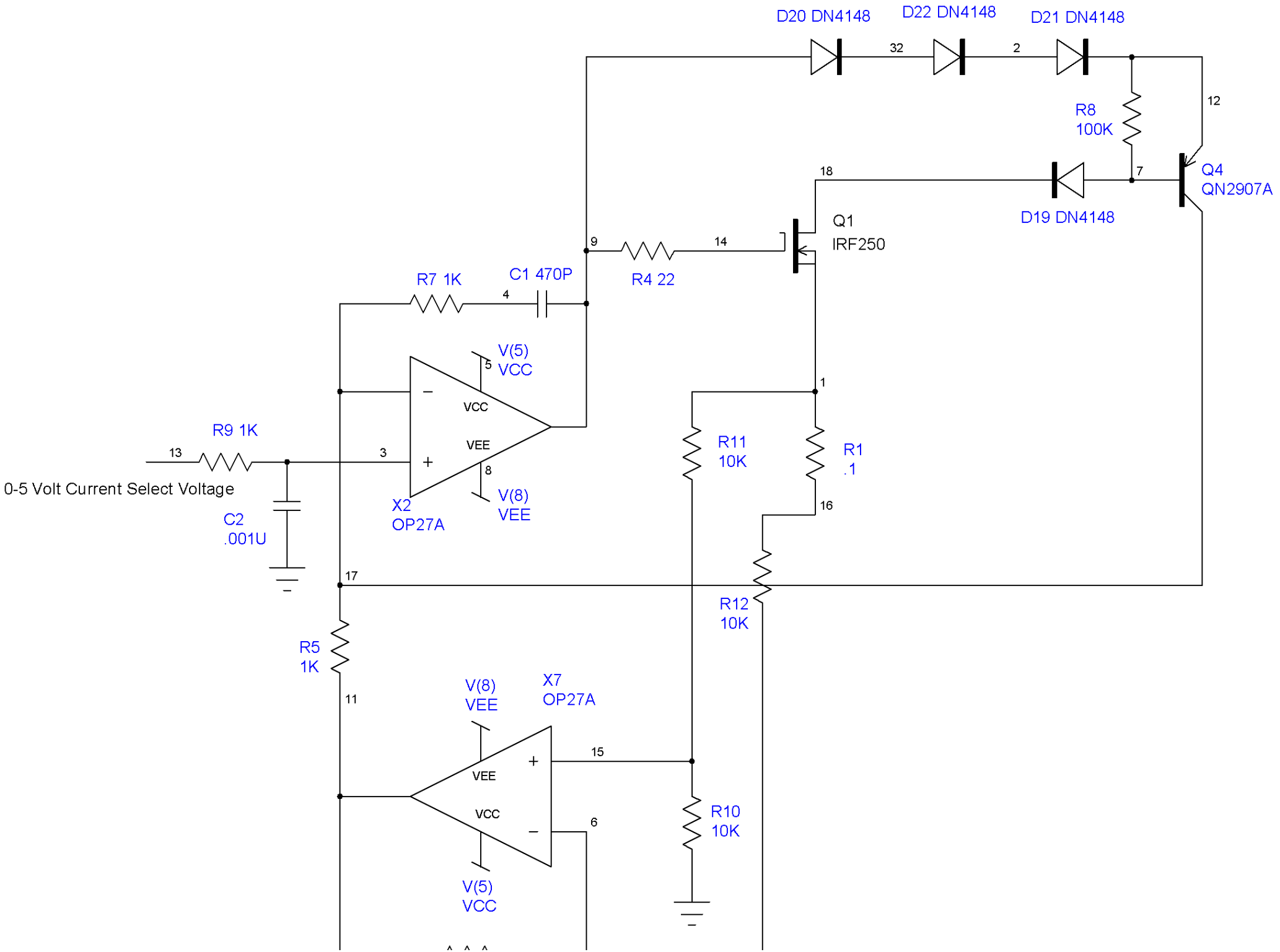
Table 18-1: DC output comparison summary

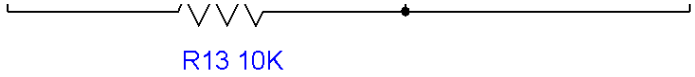
- SPICE Tip: Notice in Table 18-1, the IsSpice simulator gave us the wrong DC output voltage! Examining the model for the LM111 in IsSpice reveals the output comparator is limited internally to 10 volts. IsSpice has 5 models for the LM111 family of devices. None of these models worked correctly with this circuit. Also, none of these models use the typical propagation delay of the LM111 as a parameter in the model. This circuit is heavily effected by variations in the propagation delay. You can see this effect if you

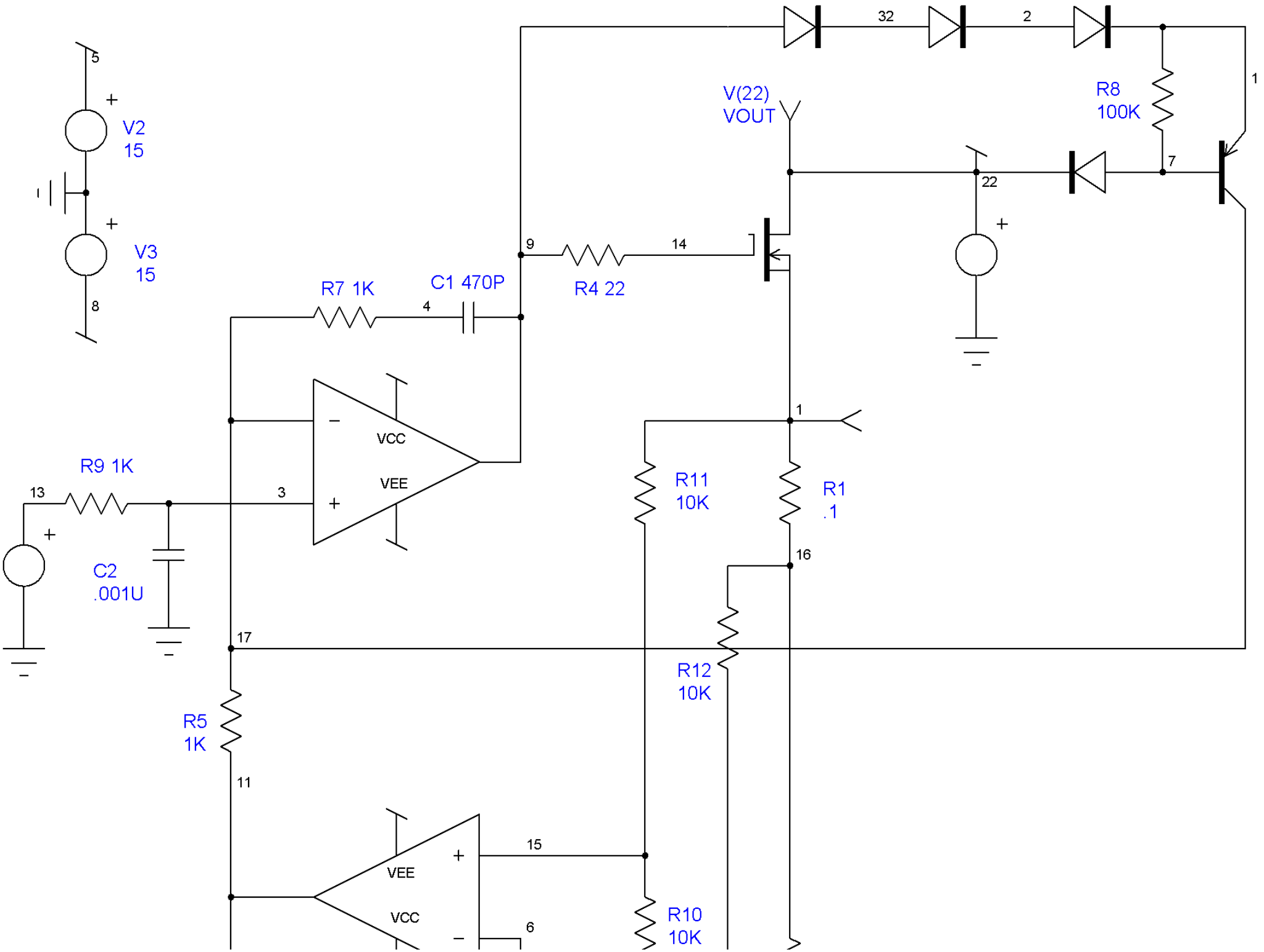
examine the results of Figures 18-1 and 18-2. The capacitor voltage continues to charge past what should have been the reference voltage. This creates an error term in the final negative output voltage of the circuit. The Texas Instruments ® Data book does not specify a minimum propagation delay, so theoretically, the propagation delay of the Intusoft models are not incorrect, however, they are probably not realistic either. The Pspice model for the LM111 also does not work properly and appears to be clamped at 9 volts. Only the Microcap model was close to the breadboard results.

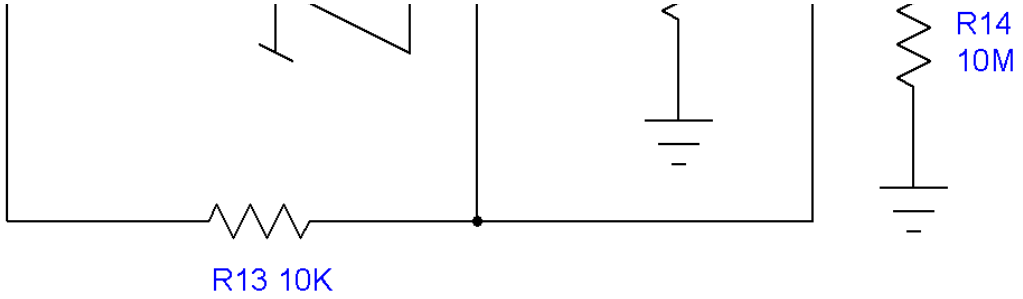
Run Time Summary		
IsSpice v 7.6	Pspice v 6.3	Micro-Cap V v2
65.033 Sec	47.59 Sec	48.00 Sec
Advantages: low parts count, only requires one lab supply to drive Op-Amps		
Disadvantages: Negative output highly dependent on propagation delay of LM111, negative drive current capability limited by LM111.		

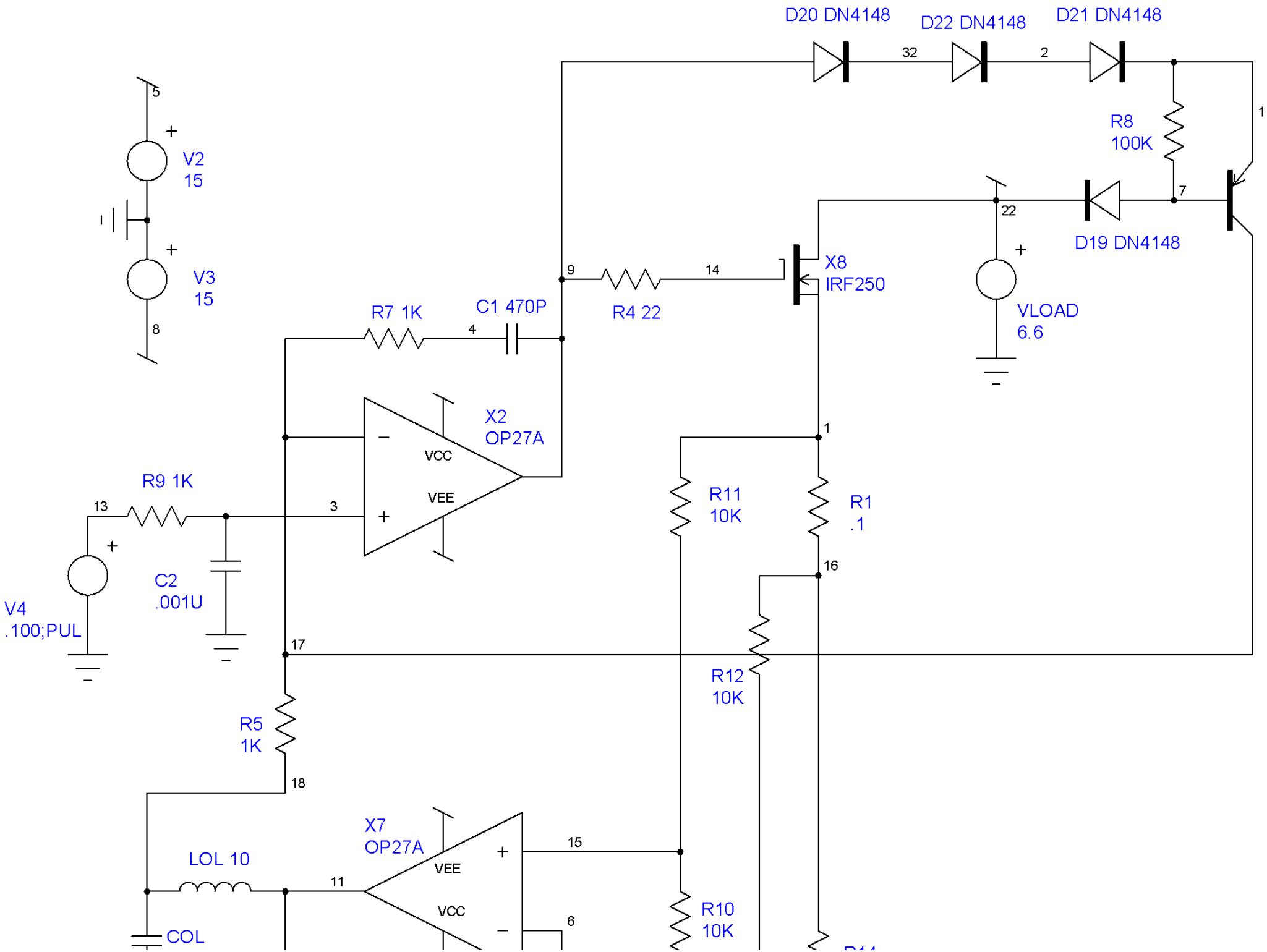
Filenames: pos2neg (IsSpice) pos2negp (Pspice) pos2negm (Microcap)


D20 DN4148
D22 DN4148
D21 DN4148
32
2
12
R8
100K
18
7
Q4
QN2907A
D19 DN4148
Q1
IRF250
9
14
R4 22
R7 1K
C1 470P
4
V(5)
VCC
5
VCC
VEE
8
V(8)
VEE
X2
OP27A
R9 1K
13
3
0-5 Volt Current Select Voltage
C2
.001U
1
R11
10K
R1
.1
16
17
R12
10K
R5
1K
11
V(8)
VEE
X7
OP27A
15
VEE
VCC
6
R10
10K
V(5)
VCC


R13 10K


5
V2
15
V3
15
8
R7 1K
C1 470P
4
9
R4 22
14
32
2
1
R8
100K
V(22)
VOUT
7
22
VCC
VEE
R9 1K
13
3
C2
.001U
R11
10K
R1
.1
16
17
R12
10K
R5
1K
11
VEE
VCC
15
6
R10
10K


R14
10M
R13 10K


D20 DN4148
D22 DN4148
D21 DN4148
32
2
1
R8
100K
7
D19 DN4148
22
X8
IRF250
VLOAD
6.6
5
V2
15
V3
15
8
9
14
R4 22
R7 1K
C1 470P
4
X2
OP27A
VCC
VEE
R9 1K
13
3
V4
.100;PUL
C2
.001U
R11
10K
R1
.1
16
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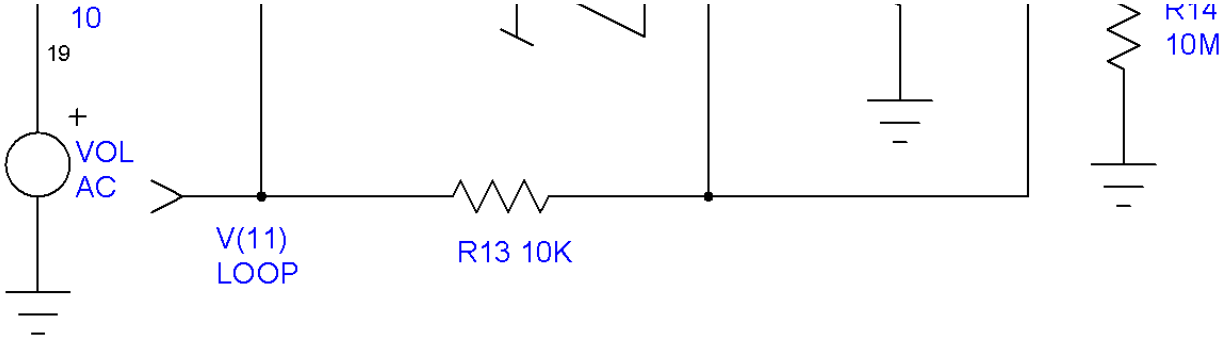
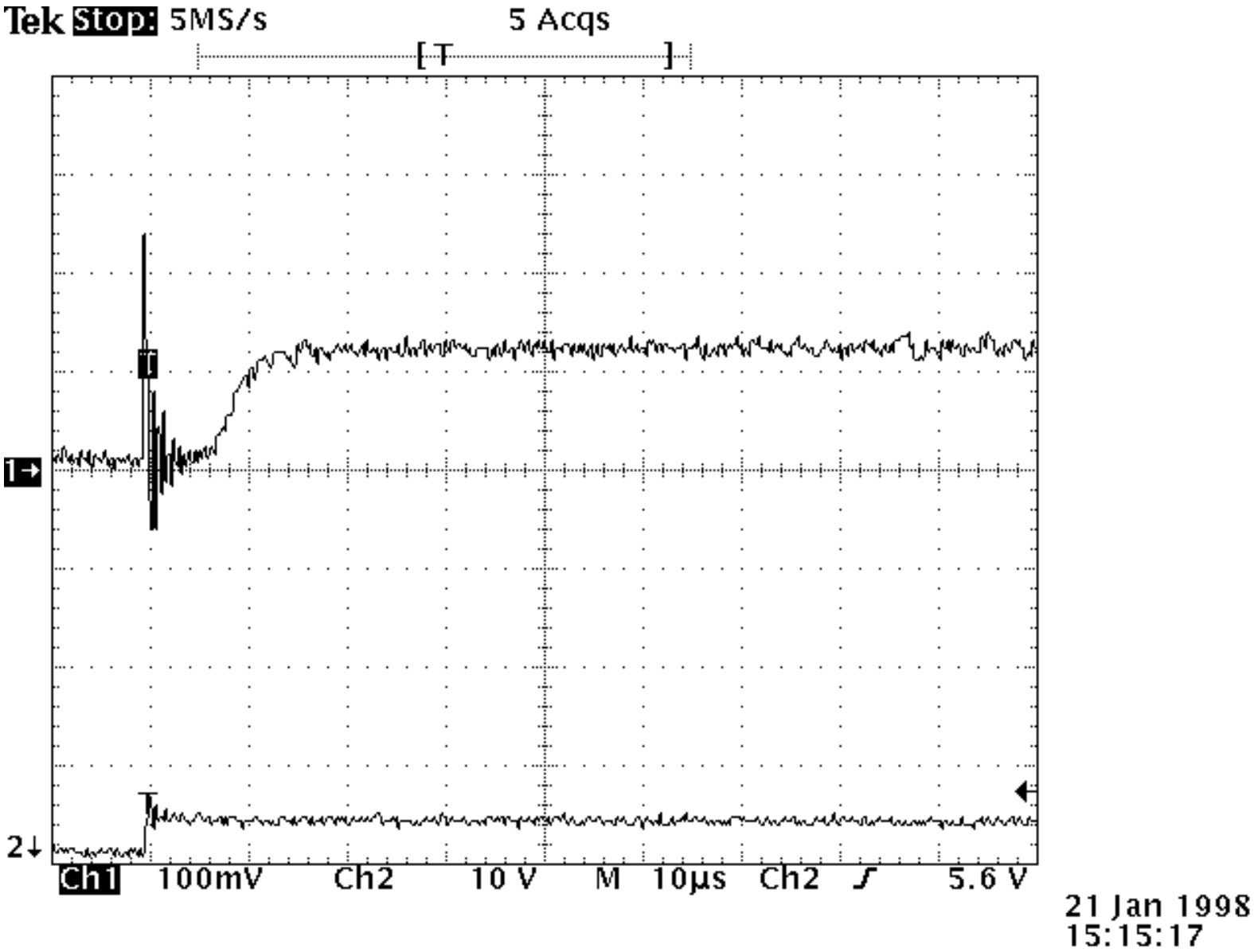
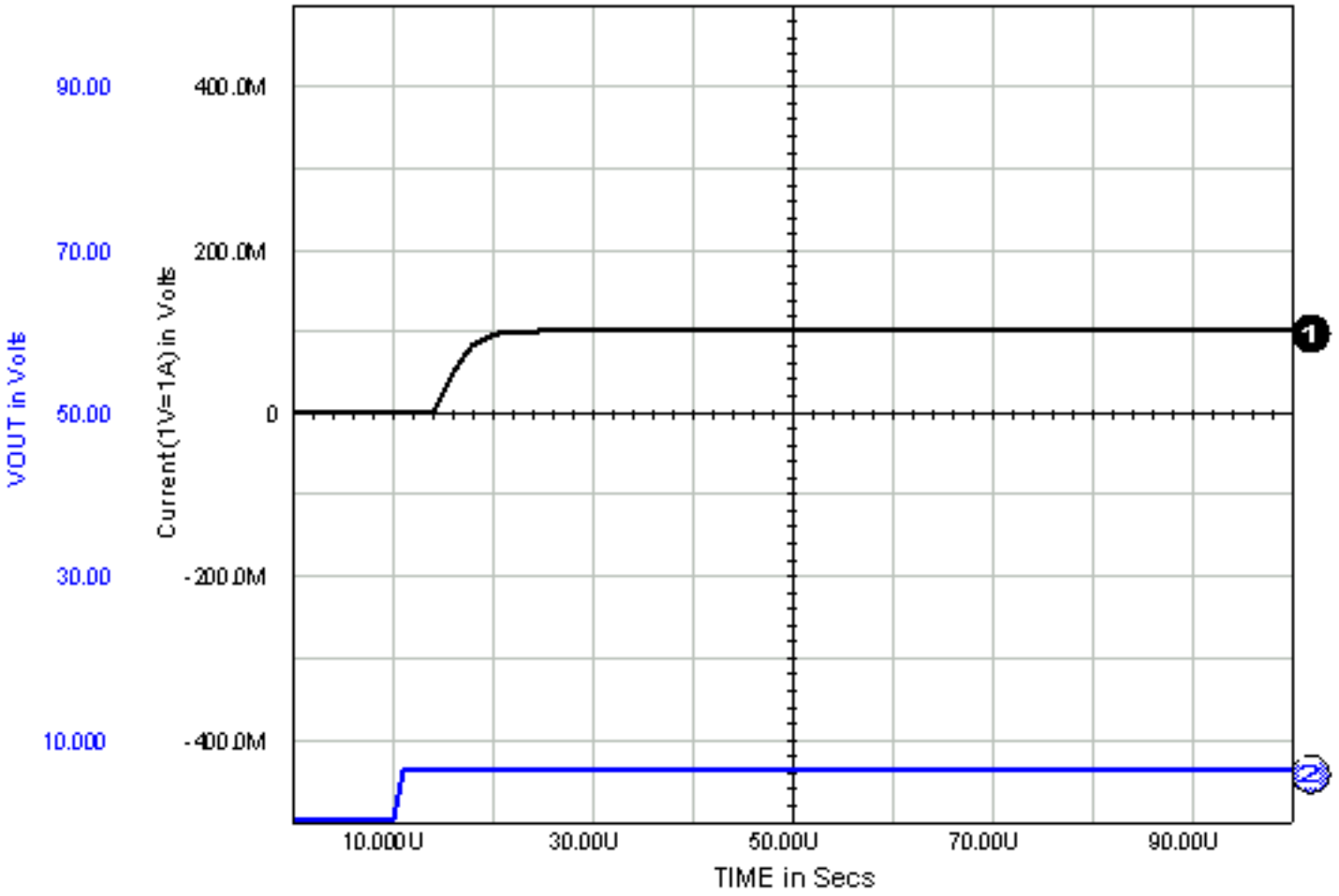
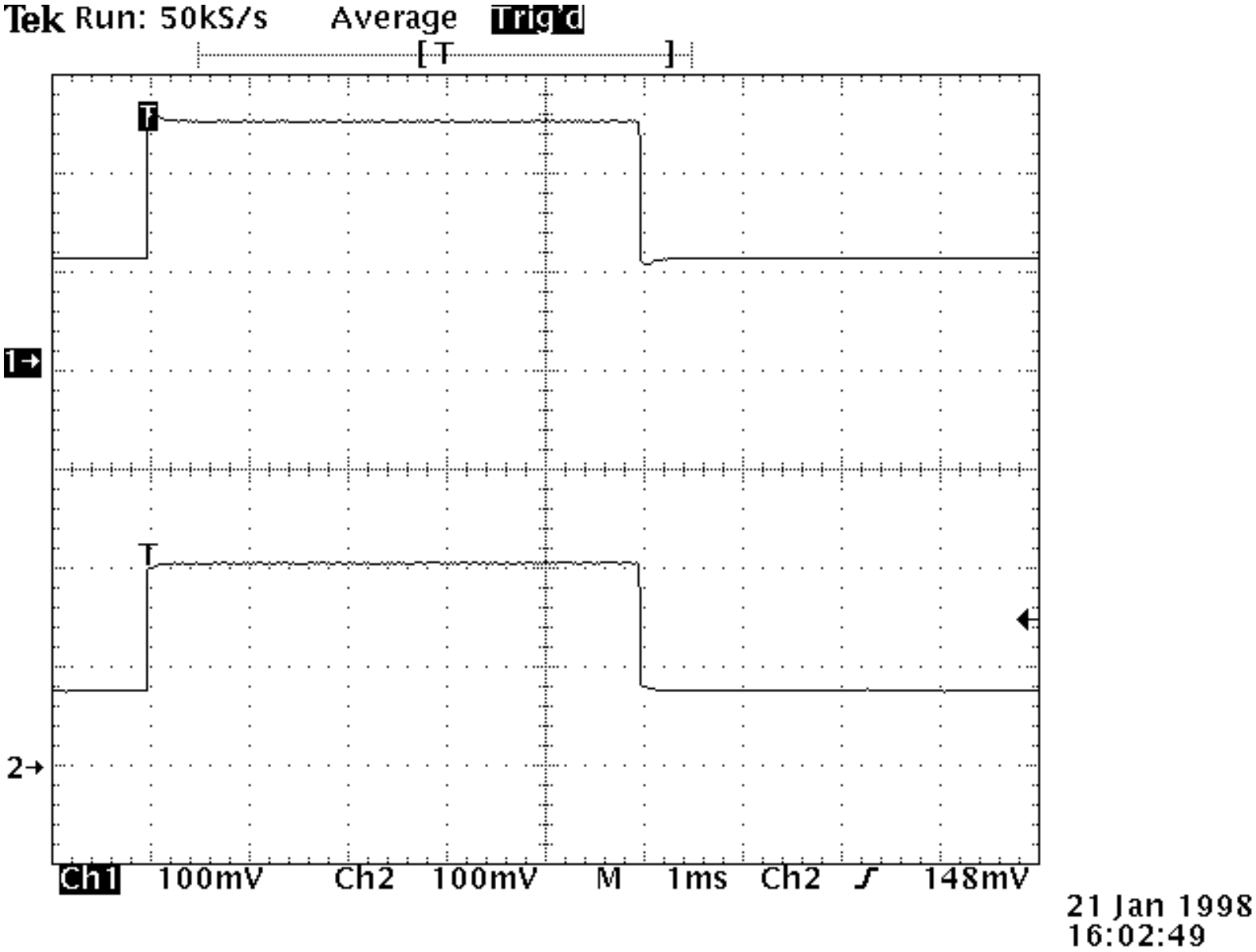
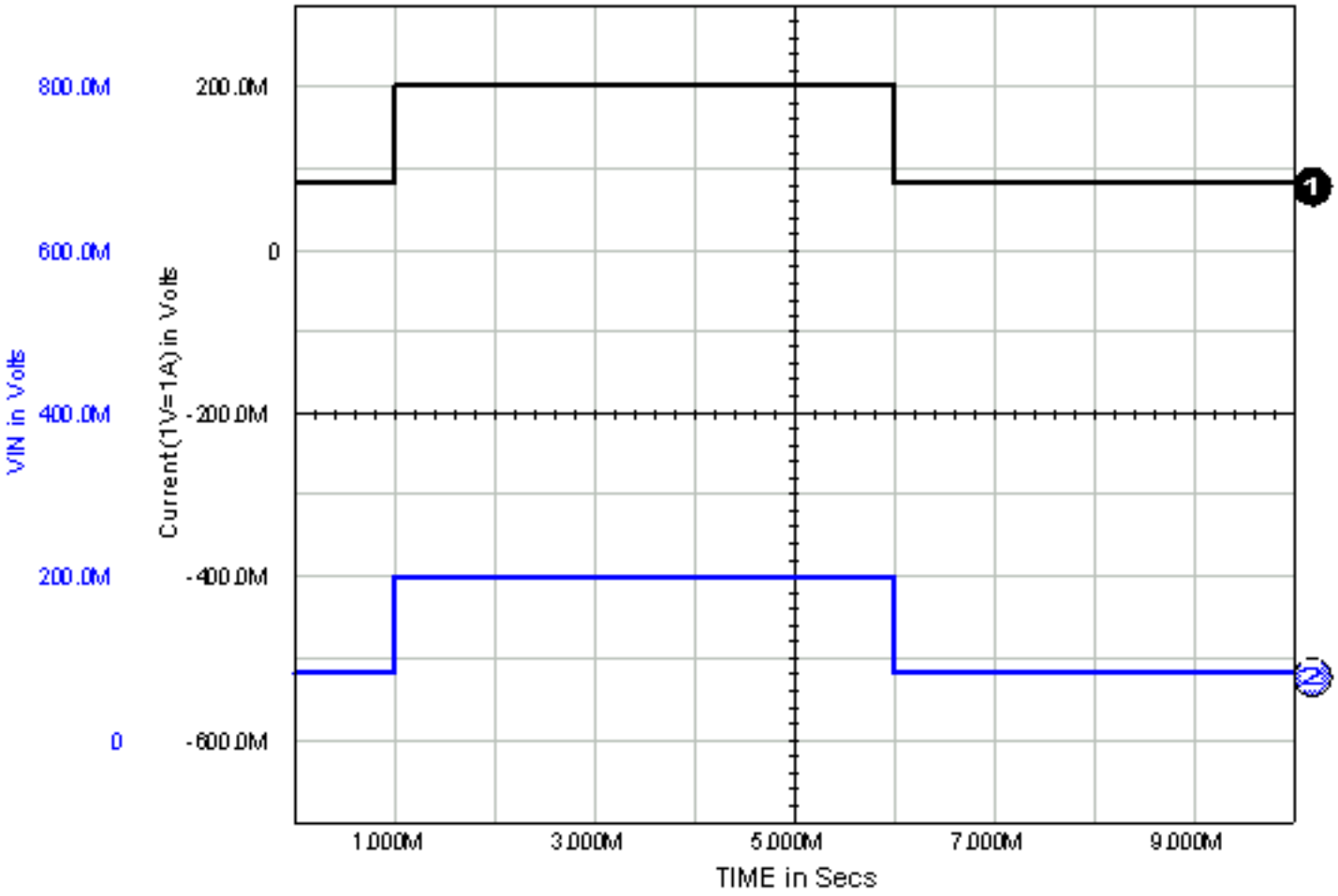
R5
1K
18
X7
OP27A
LOL 10
11
15
6
R10
10K
COL


10
19
+
VOL
AC
V(11)
LOOP
R13 10K
R14
10M


Tek Stop: 5MS/s
5 Acqs
Ch1 100mV Ch2 10 V M 10µs Ch2 ƒ 5.6 V
21 Jan 1998
15:15:17


90.00
70.00
50.00
30.00
10.000
VOUT in Volts
400.0M
200.0M
0
-200.0M
-400.0M
Current(1V=1A)in Volts
10.000U
30.00U
50.00U
70.00U
90.00U
TIME in Secs
1
2


Tek Run: 50kS/s Average Trig'd
Ch1 100mV Ch2 100mV M 1ms Ch2 ∫ 148mV
21 Jan 1998
16:02:49


800.0M
600.0M
400.0M
200.0M
0
VIN in Volts
200.0M
0
-200.0M
-400.0M
-600.0M
Current(1V=1A)in Volts
1.000M
3.000M
5.000M
7.000M
9.000M
TIME in Secs
1
2

1-22-98

PAGE 01

ANALYTICAL ENGRG

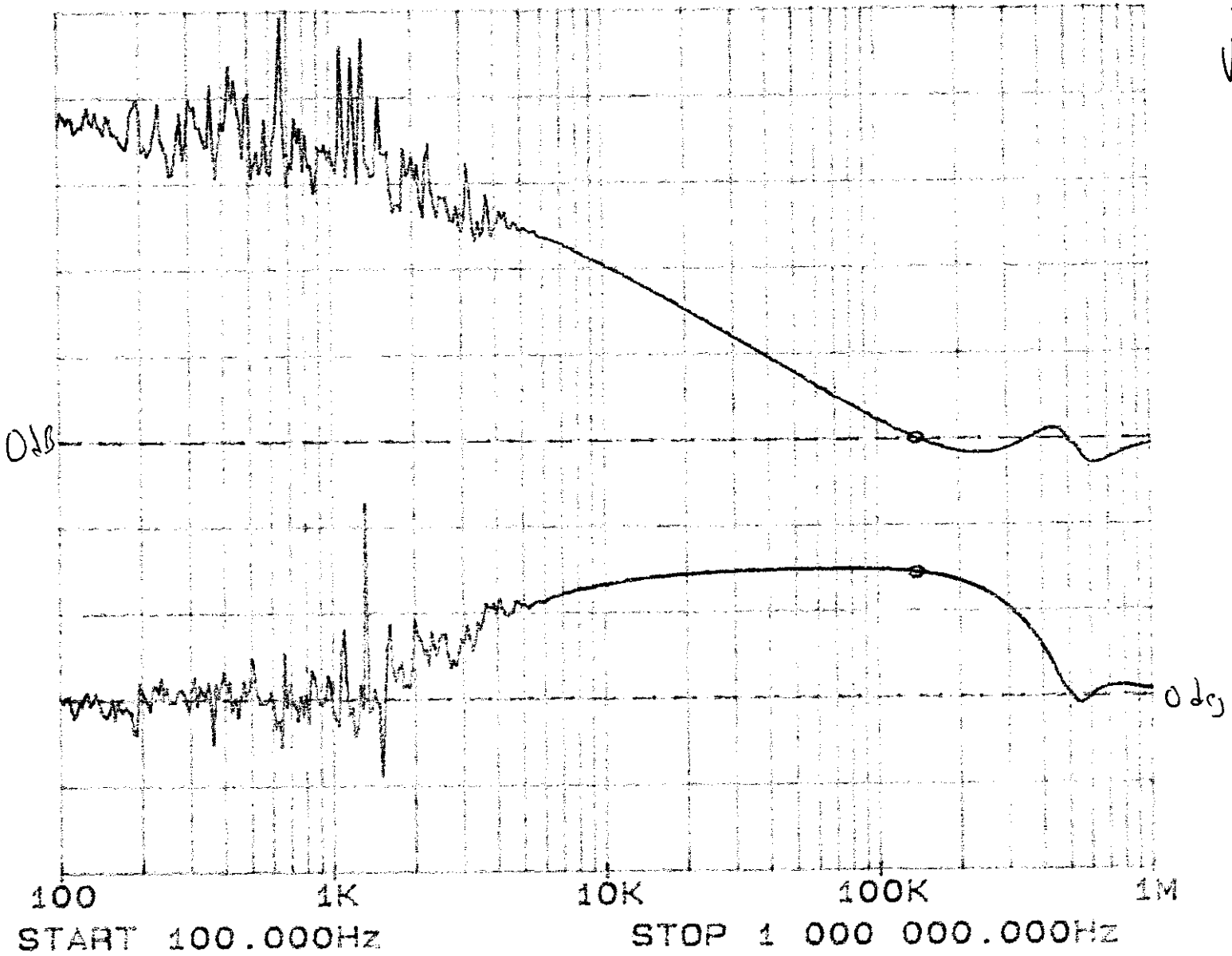
1/27/1998 09:13 6028907198

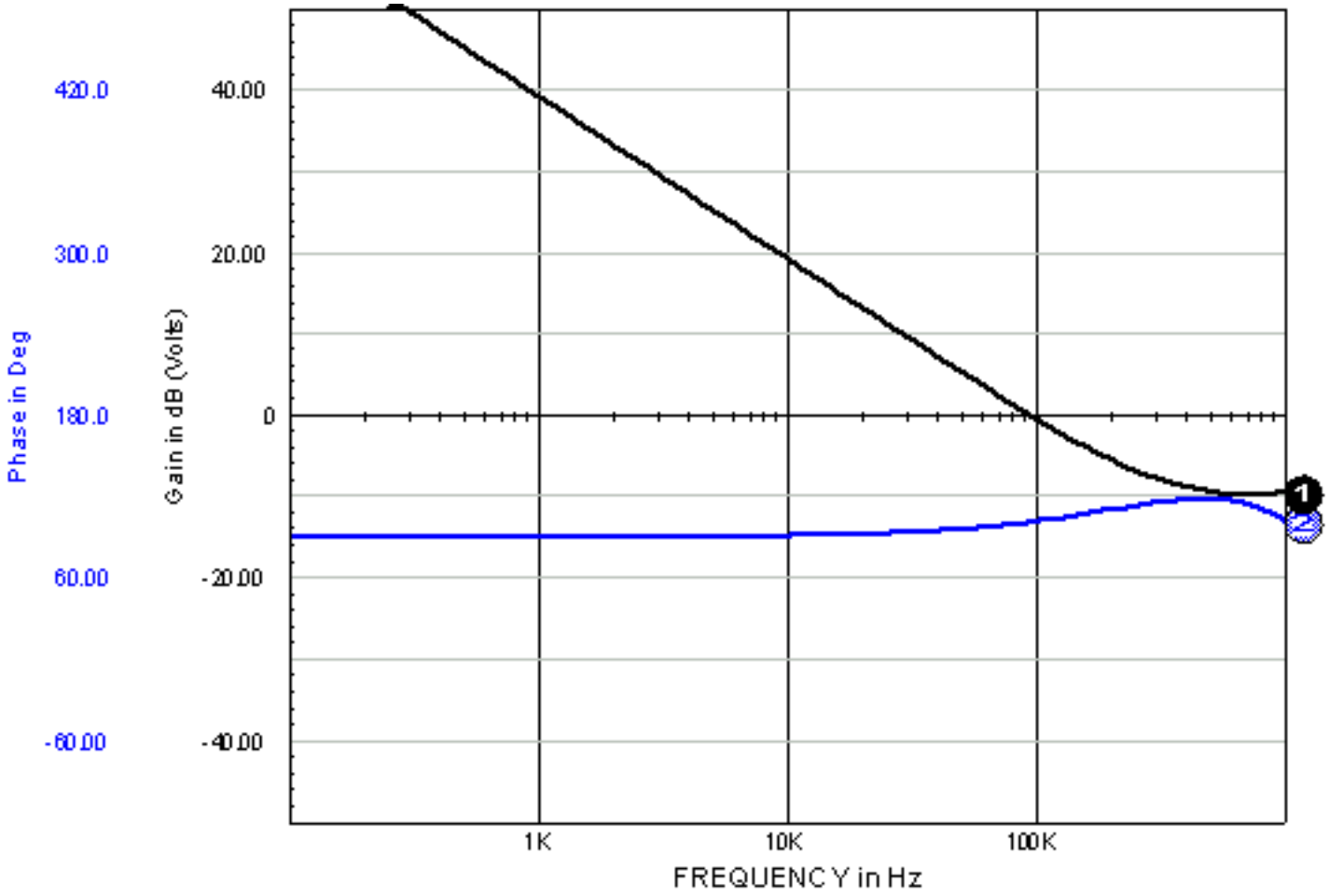
REF LEVEL	/DIV	MARKER 138 931.252Hz
0.000dB	10.000dB	MAG (A/R) 0.129dB
0.0deg	60.000deg	MARKER 138 931.252Hz
		PHASE (A/R) 86.932deg

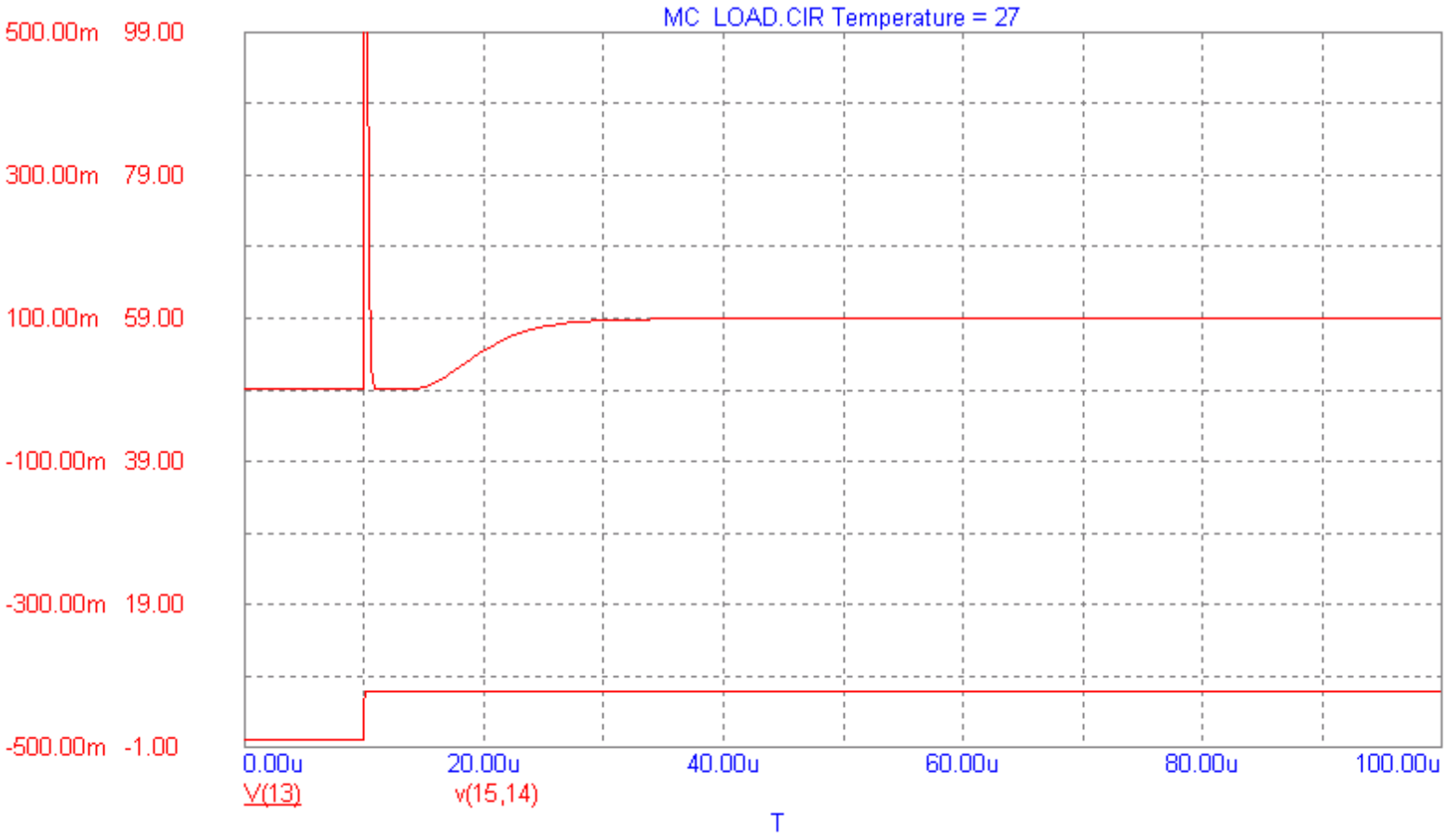
LOADING

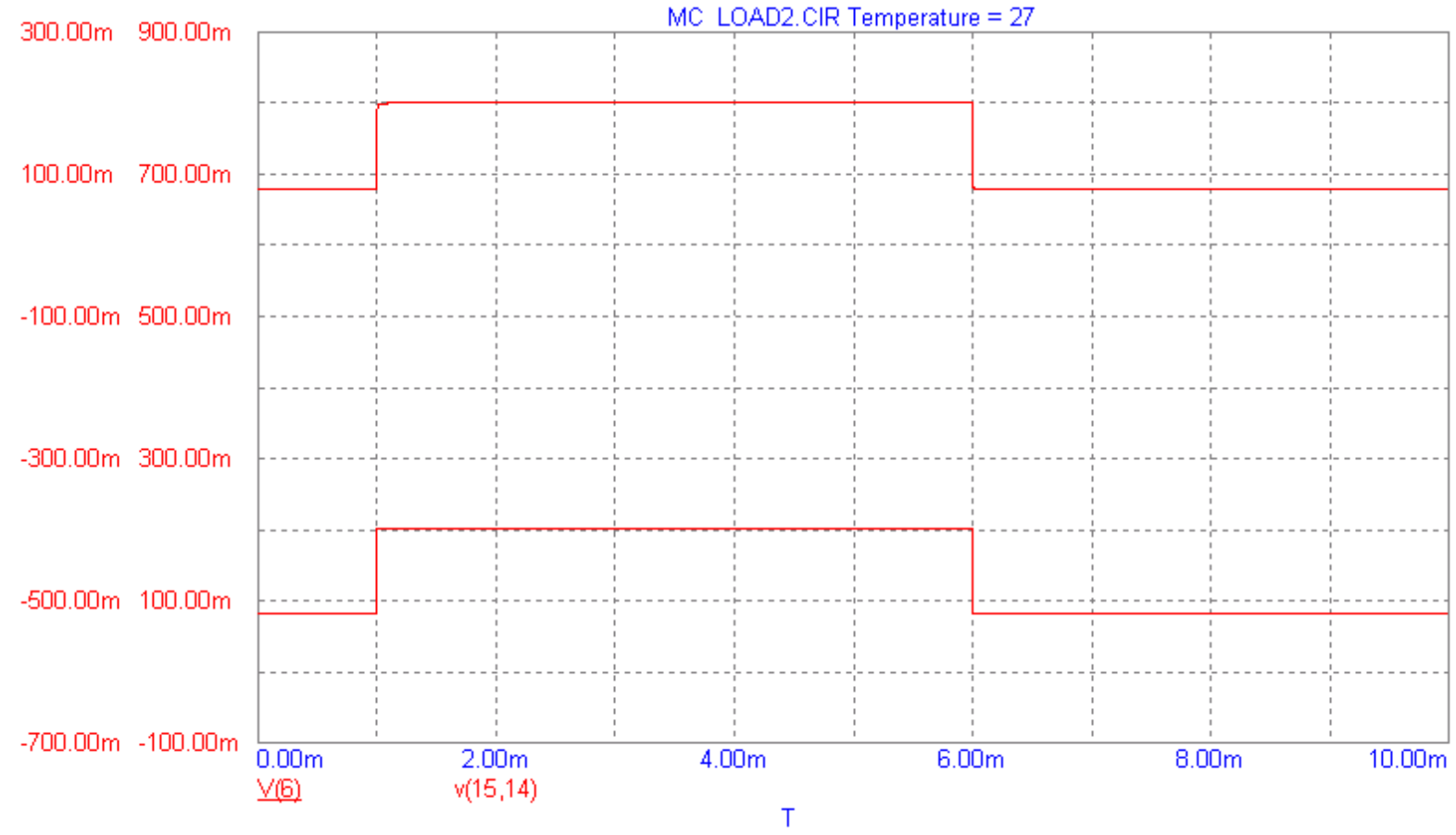
$I_{out} = 100mA$

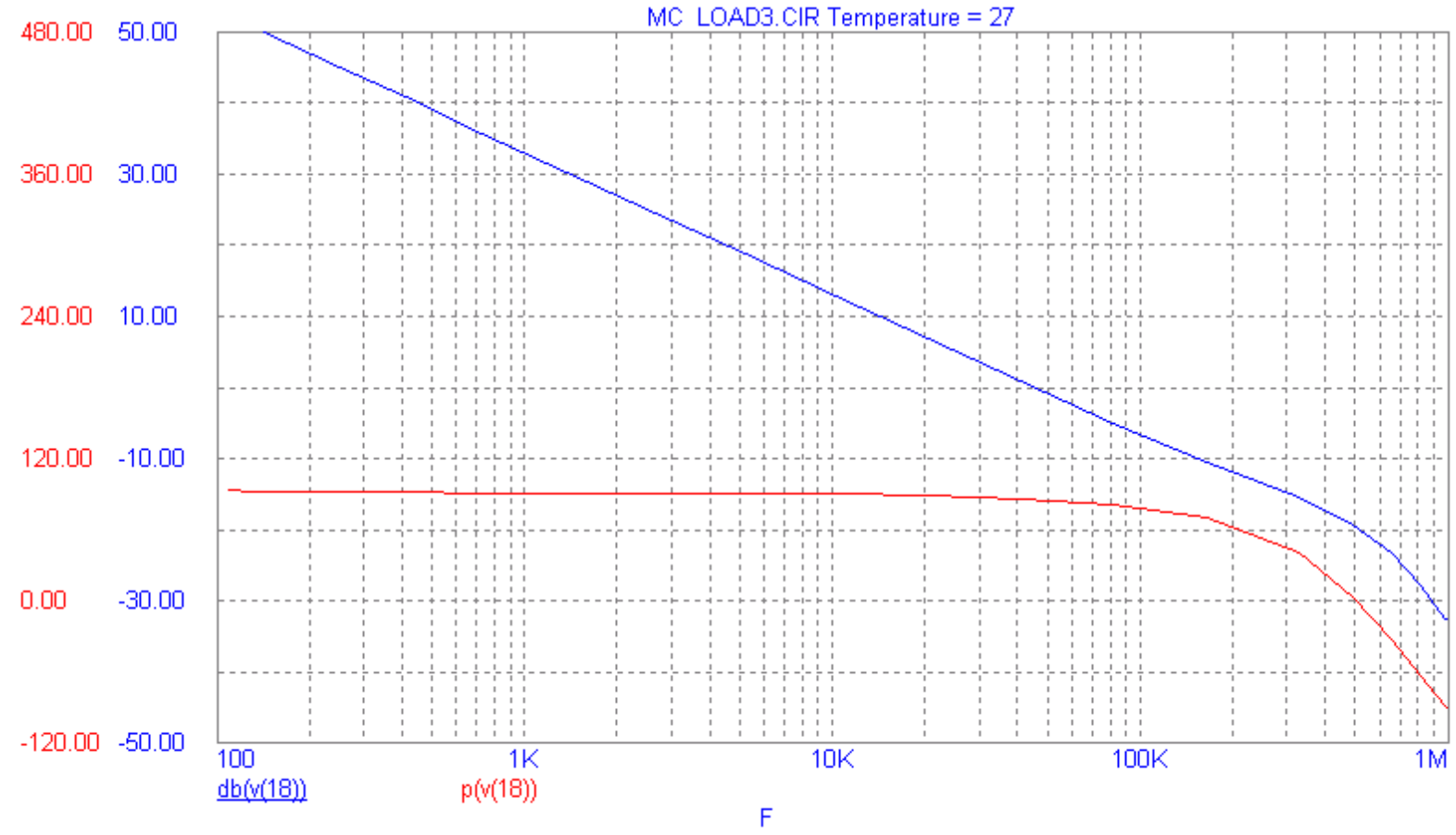
$V_{out} = 6.6V$

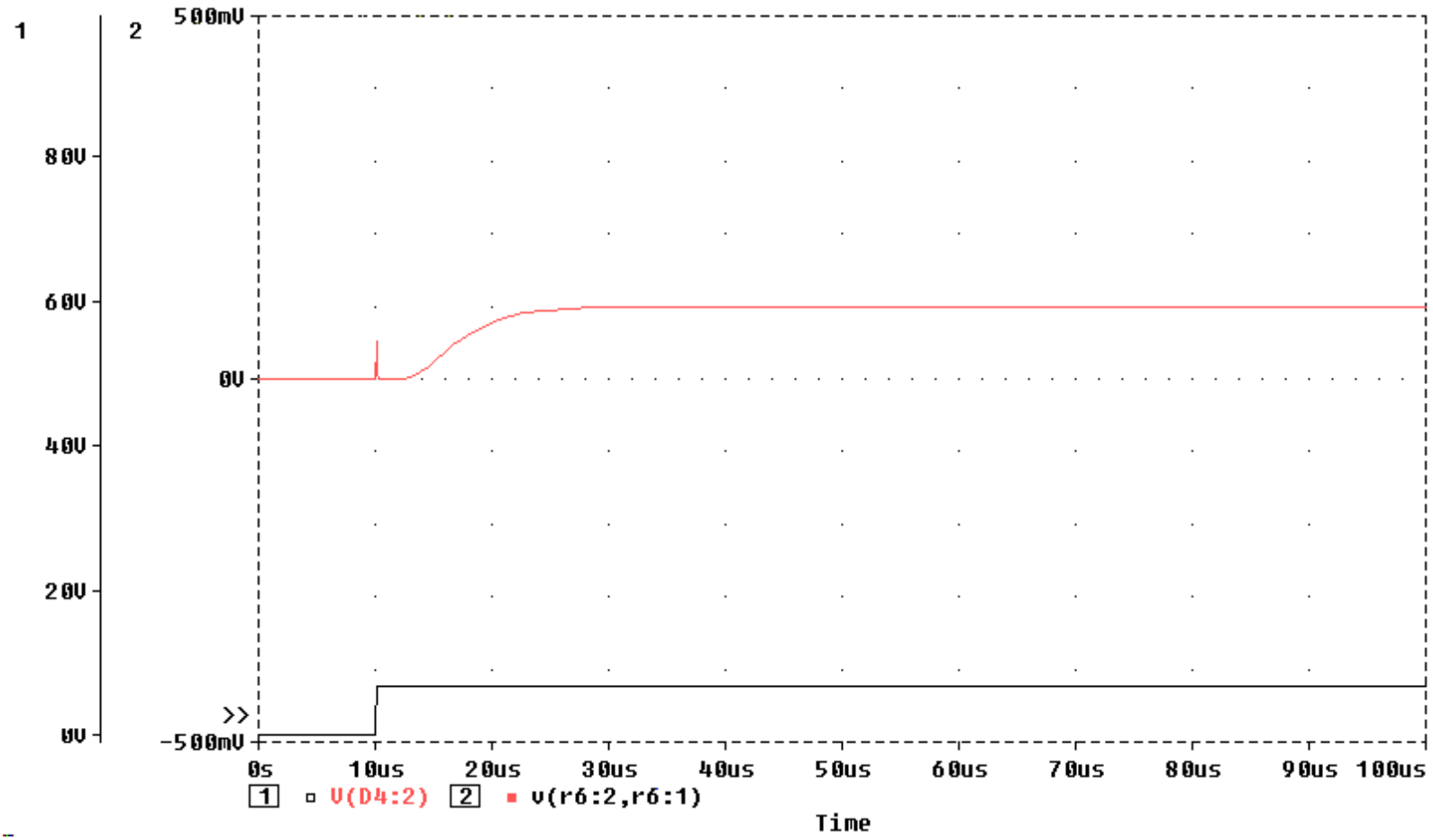


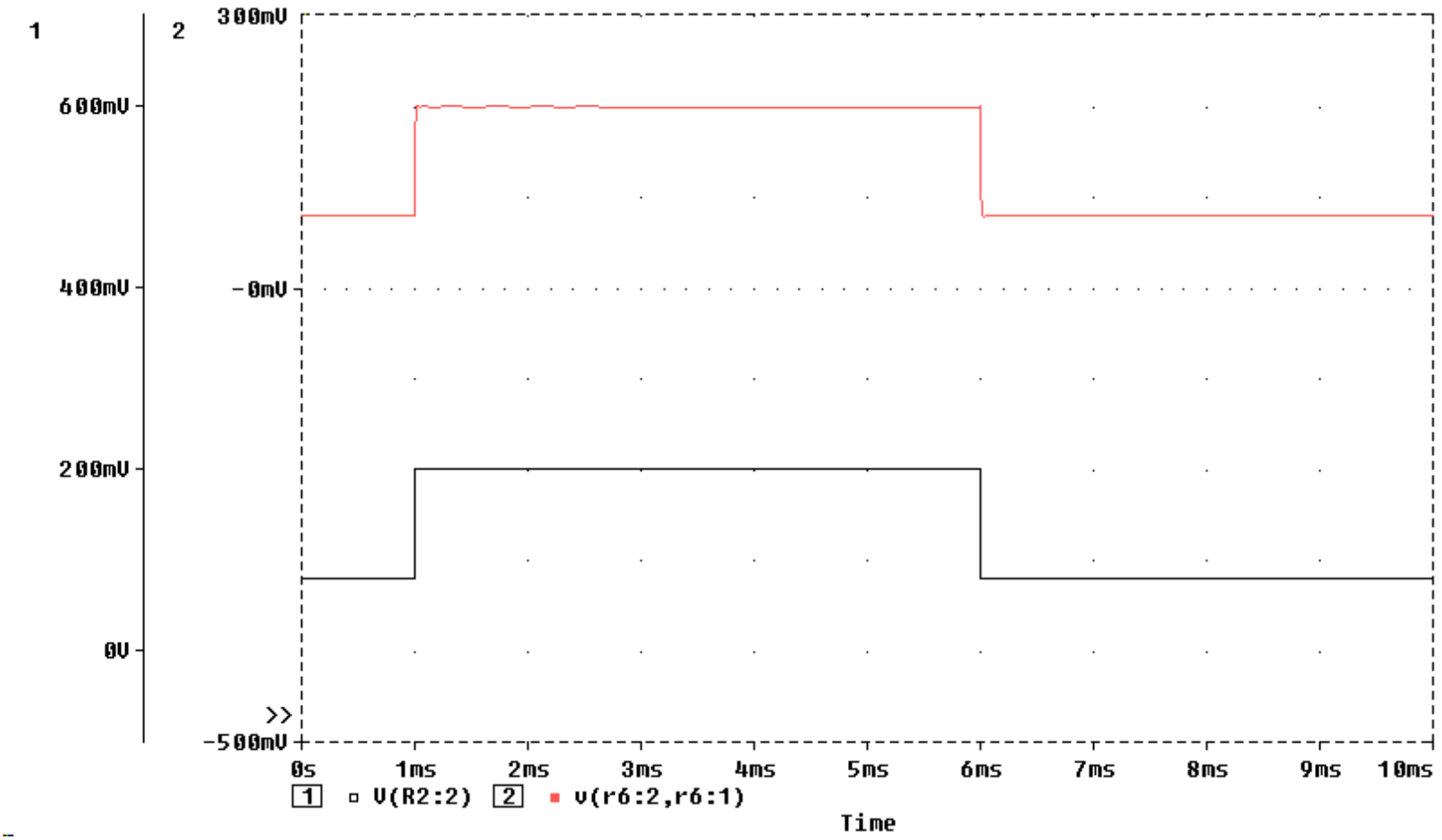

420.0
300.0
180.0
60.00
-60.00
Phase in Deg
40.00
20.00
0
-20.00
-40.00
Gain in dB (Volts)
1K
10K
100K
FREQUENCY in Hz
1
2

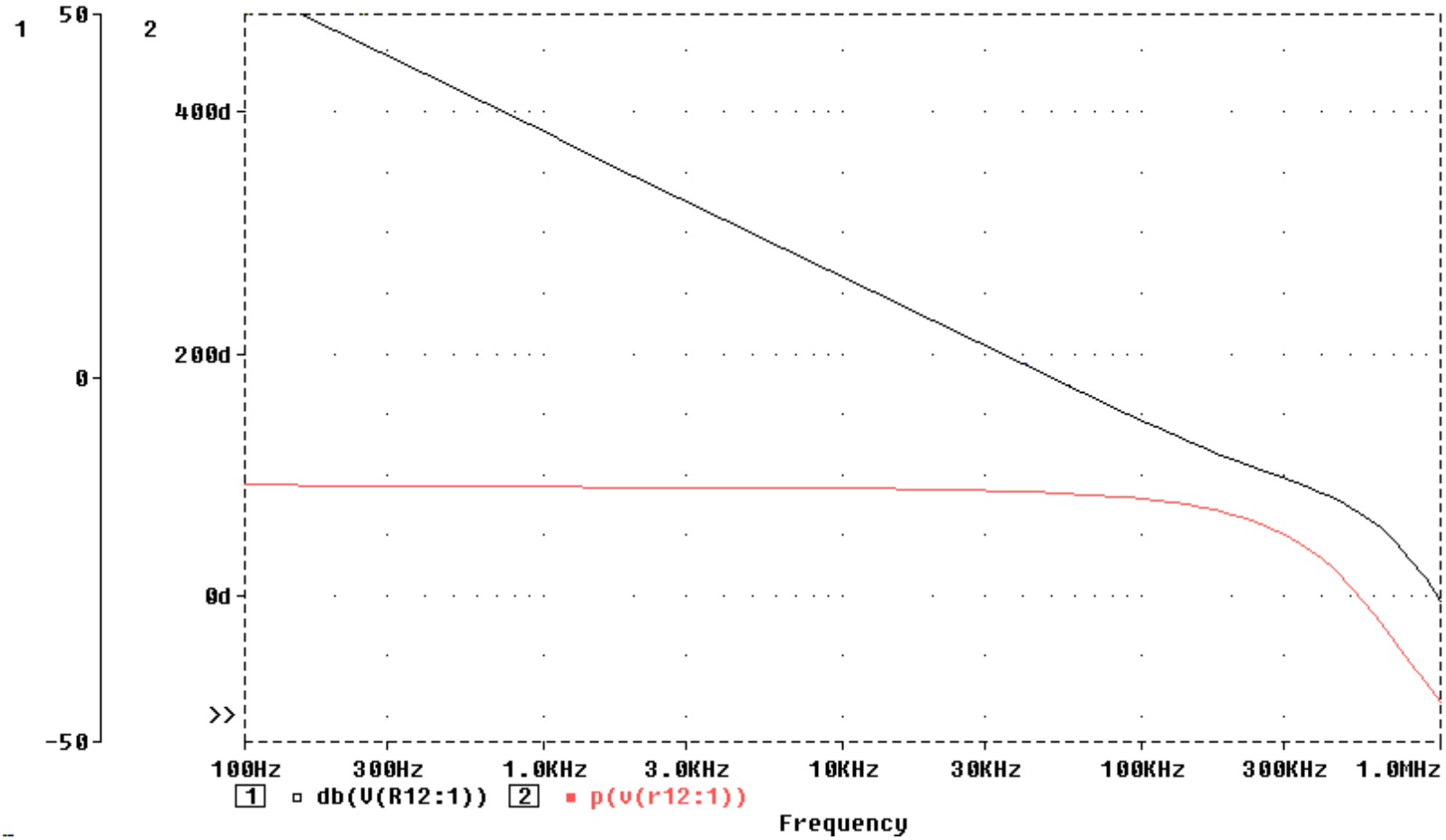

MC LOAD.CIR Temperature = 27
500.00m 99.00
300.00m 79.00
100.00m 59.00
-100.00m 39.00
-300.00m 19.00
-500.00m -1.00
0.00u
20.00u
40.00u
60.00u
80.00u
100.00u
V(13)
v(15,14)
T


MC LOAD2.CIR Temperature = 27
300.00m
900.00m
100.00m
700.00m
-100.00m
500.00m
-300.00m
300.00m
-500.00m
100.00m
-700.00m
-100.00m
0.00m
2.00m
4.00m
6.00m
8.00m
10.00m
V(6)
v(15,14)
T


MC LOAD3.CIR Temperature = 27
480.00
360.00
240.00
120.00
0.00
-120.00
50.00
30.00
10.00
-10.00
-30.00
-50.00
100
1K
10K
100K
1M
db(v(18))
p(v(18))
F


1
2
500mV
80V
60V
0V
40V
20V
0V
>>
-500mV
0s
10us
20us
30us
40us
50us
60us
70us
80us
90us
100us
1 V(D4:2) 2 v(r6:2,r6:1)
Time


1
2
300mV
600mV
400mV
-0mV
200mV
0V
>>
-500mV
0s
1ms
2ms
3ms
4ms
5ms
6ms
7ms
8ms
9ms
10ms
1 V(R2:2) 2 v(r6:2,r6:1)
Time


1
50
2
400d
200d
0
0d
>>
-50
100Hz
300Hz
1.0KHz
3.0KHz
10KHz
30KHz
100KHz
300KHz
1.0MHz
1 db(V(R12:1)) 2 p(v(r12:1))
Frequency

#19: Built-in Variable Electronic Load Adjustment

The final piece in the Mosfet Electronic load puzzle is a method of adjusting the current limit. A simplistic, yet flexible circuit to accomplish this is shown in Figure 19-1.

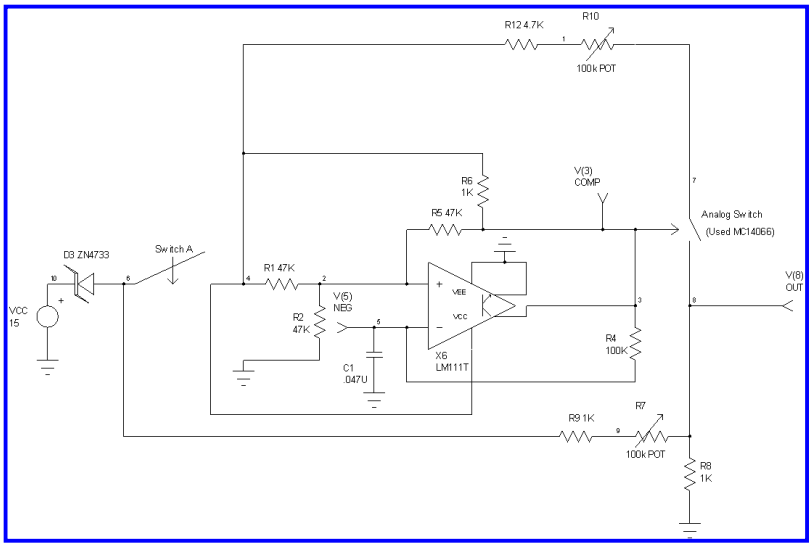


Figure 19-1: Electronic load reference and pulse load schematic

This circuit gives the user the option to use a DC current, or to use a pulsed current as a load (useful for checking load switching transients of power supplies). The 15 volt input signal is dropped to 10 volts by a 5 volt zener in series. Switch A selects between the simple potentiometer voltage divider circuit (limited to 5 volts maximum by the divider resistors), or the pulse load. The pulse is generated by the same basic circuit as in the positive to negative DC circuit in circuit #51. Capacitor C1 and resistor R4 are increased in order to slow the pulse down to 150 Hz. An analog switch is used to switch between the lower voltage level (set by R7-R9) and the upper voltage level (set by R10, R12). Potentiometers R7 and R10 set the lower and upper voltage levels from 0 to 5 volts. The equivalent simulation schematic is shown in Figure 19-2.

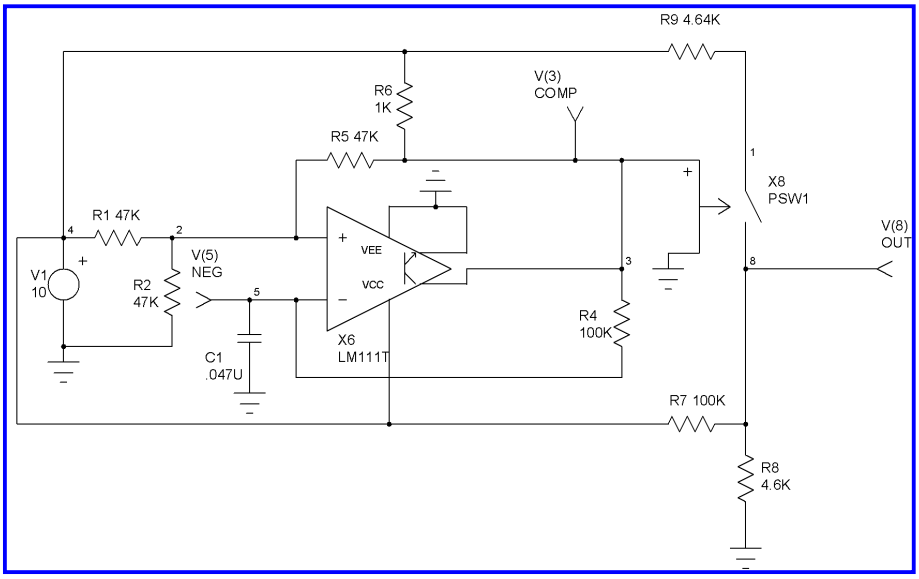


Figure 19-2: Electronic load reference and pulse load SPICE schematic

The breadboard pulse load waveform (from 300mA to 5 A) is shown in Figure 19-3. The IsSpice simulation results are shown in Figure 19-4. Microcap and Pspice results are shown in Figures 19-5 and 19-6. In Figures 19-3 through 19-6, the top waveform is the output of the comparator and the bottom waveform is the output of the analog switch (which would then be connected to the electronic load in Circuit #17.

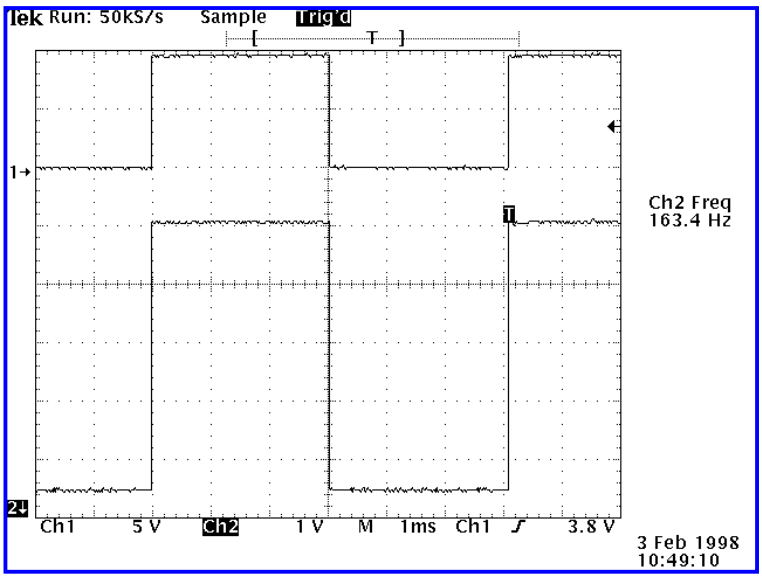


Figure 19-3: Electronic load reference pulse output waveforms

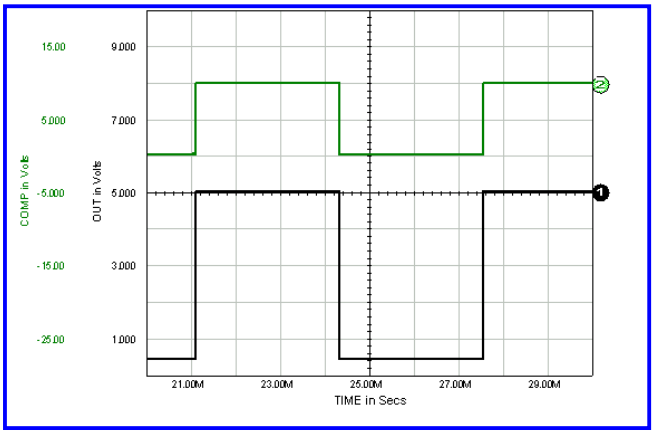


Figure 19-4: IsSpice simulation results: reference pulse output waveforms

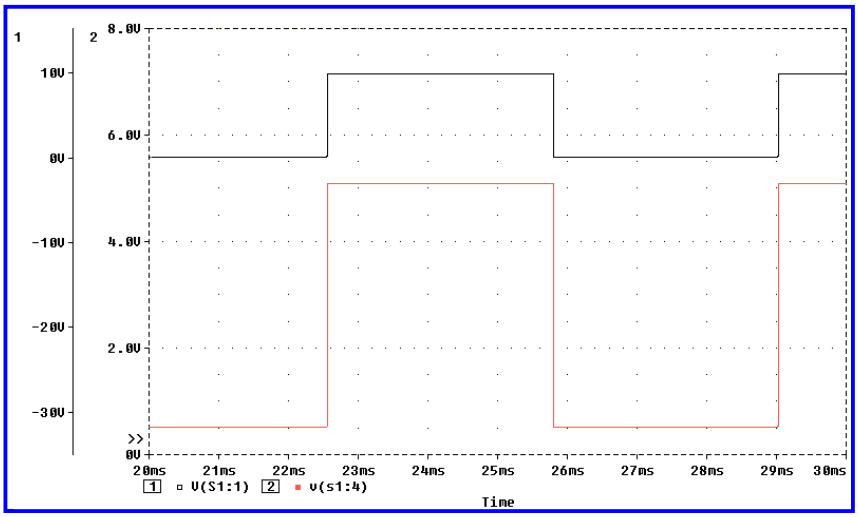


Figure 19-5: Ppice simulation results: reference pulse output waveforms

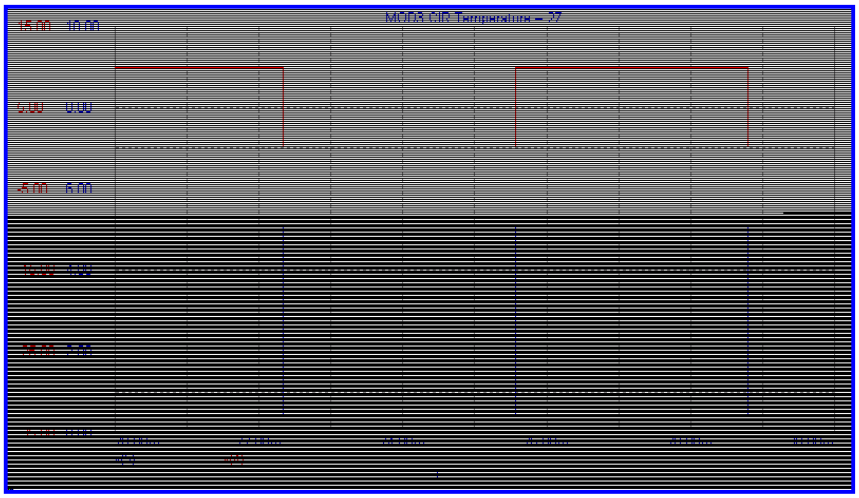
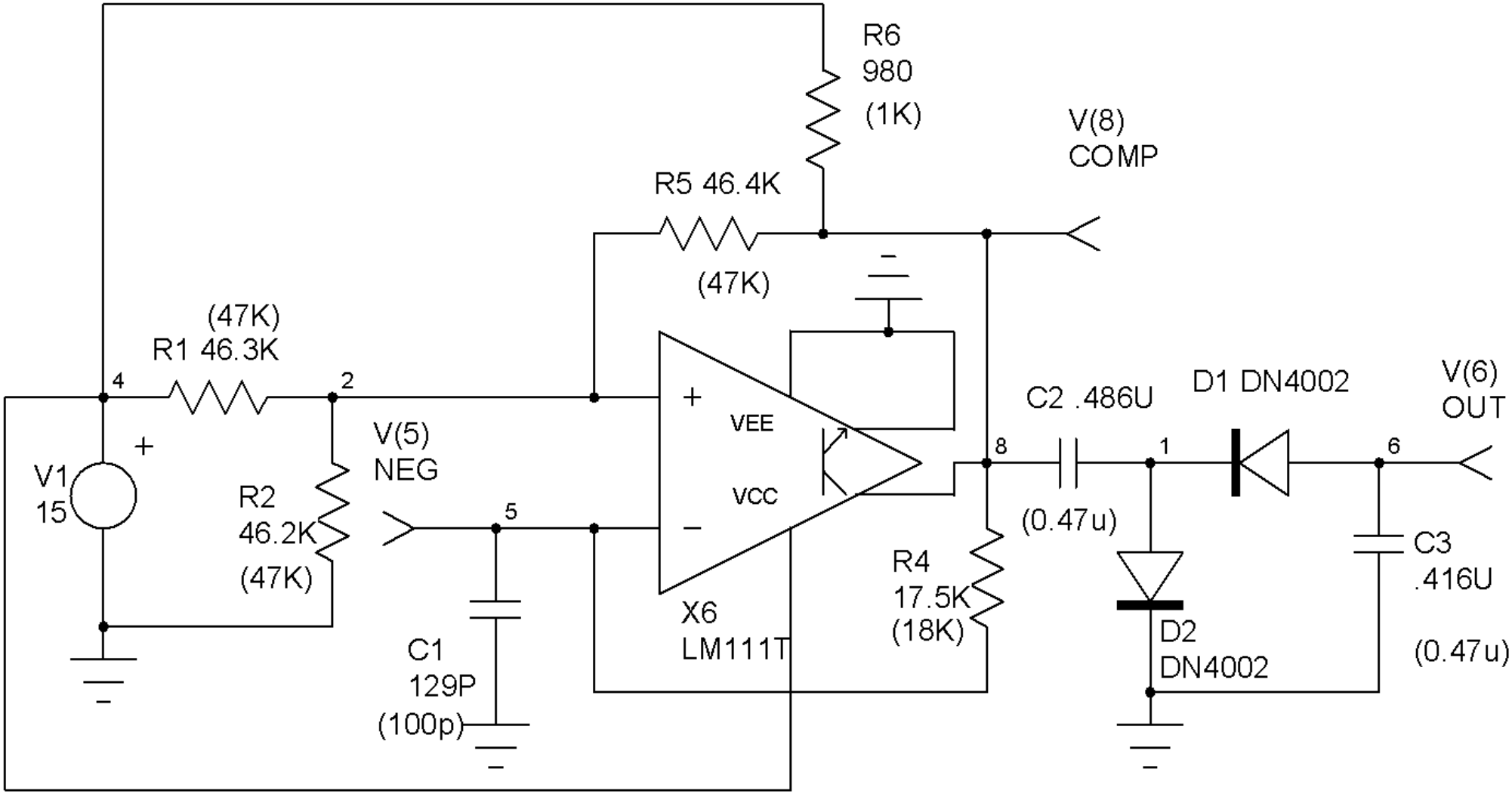


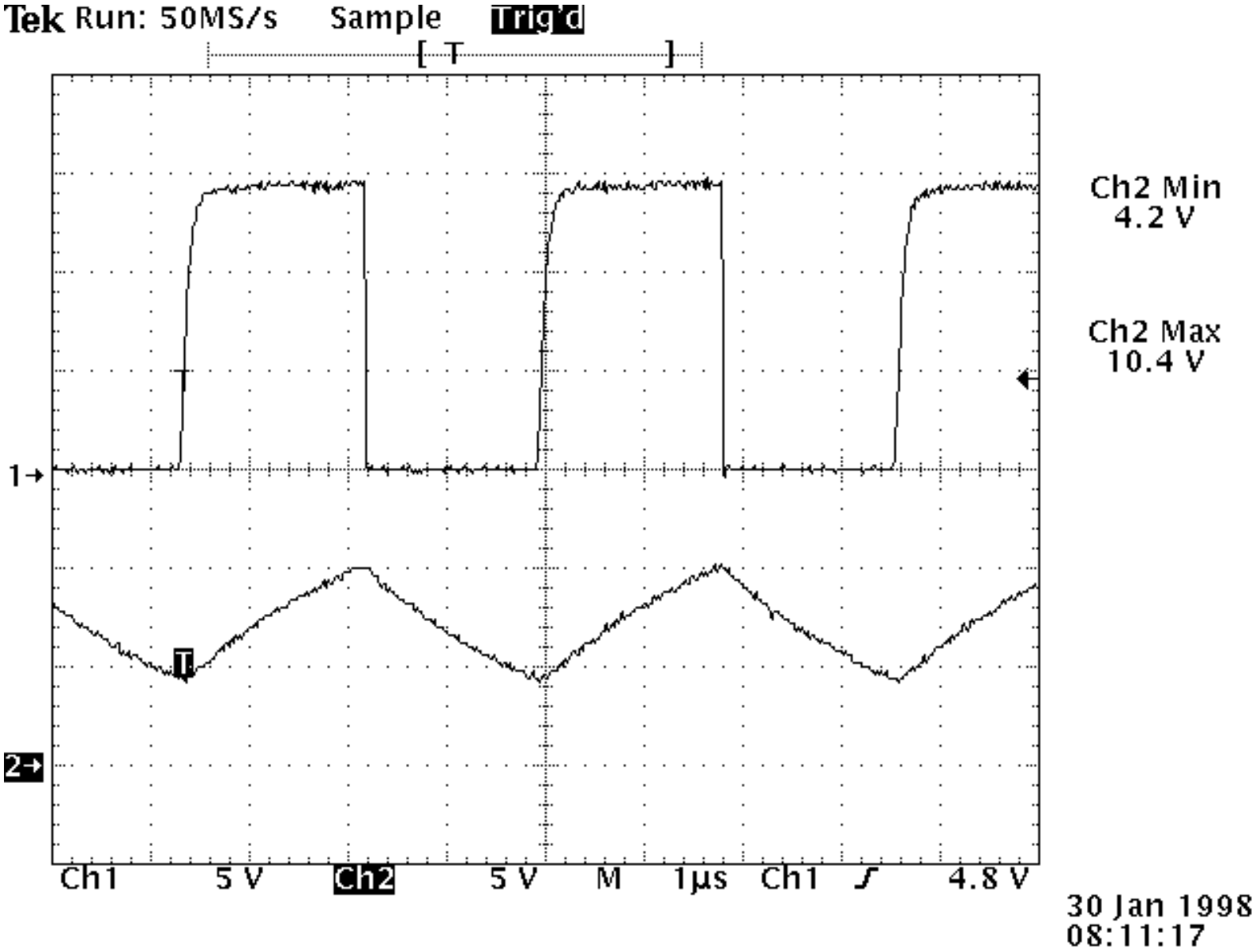
Figure 19-6: Microcap simulation results: reference pulse output waveforms

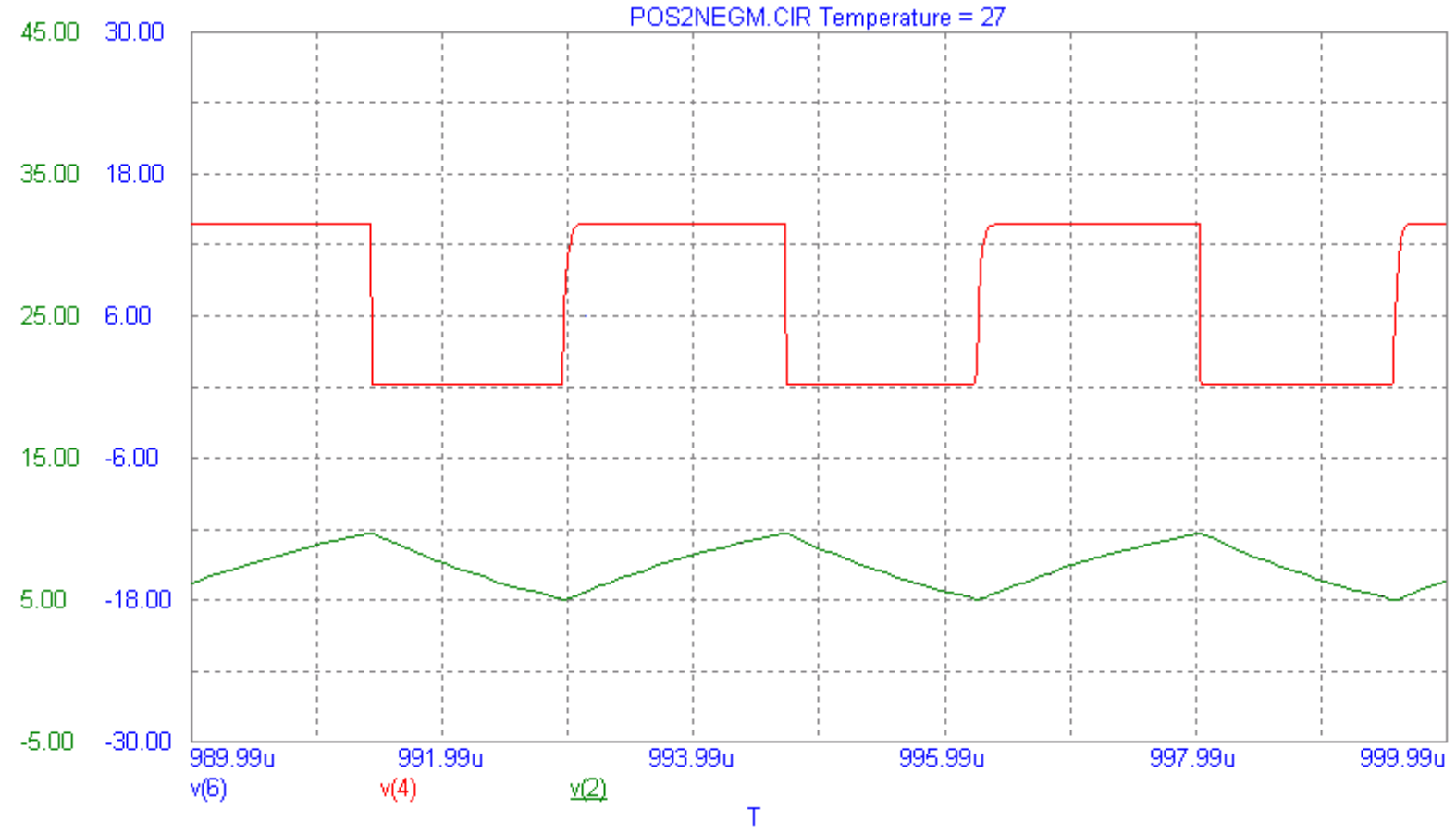
- SPICE Tip: The three simulators have slightly different switch models. The IsSpice model used is the **PSW1** switch. The parameters passed are VON=7 RON=100 VOFF=2 ROFF=100MEG. The Pspice simulation used a model called **Sbreak**. The Microcap simulation used the **Switch** model under the Analog Primitives>Miscellaneous menu. The parameters passed are V,2,15,100,100MEG.

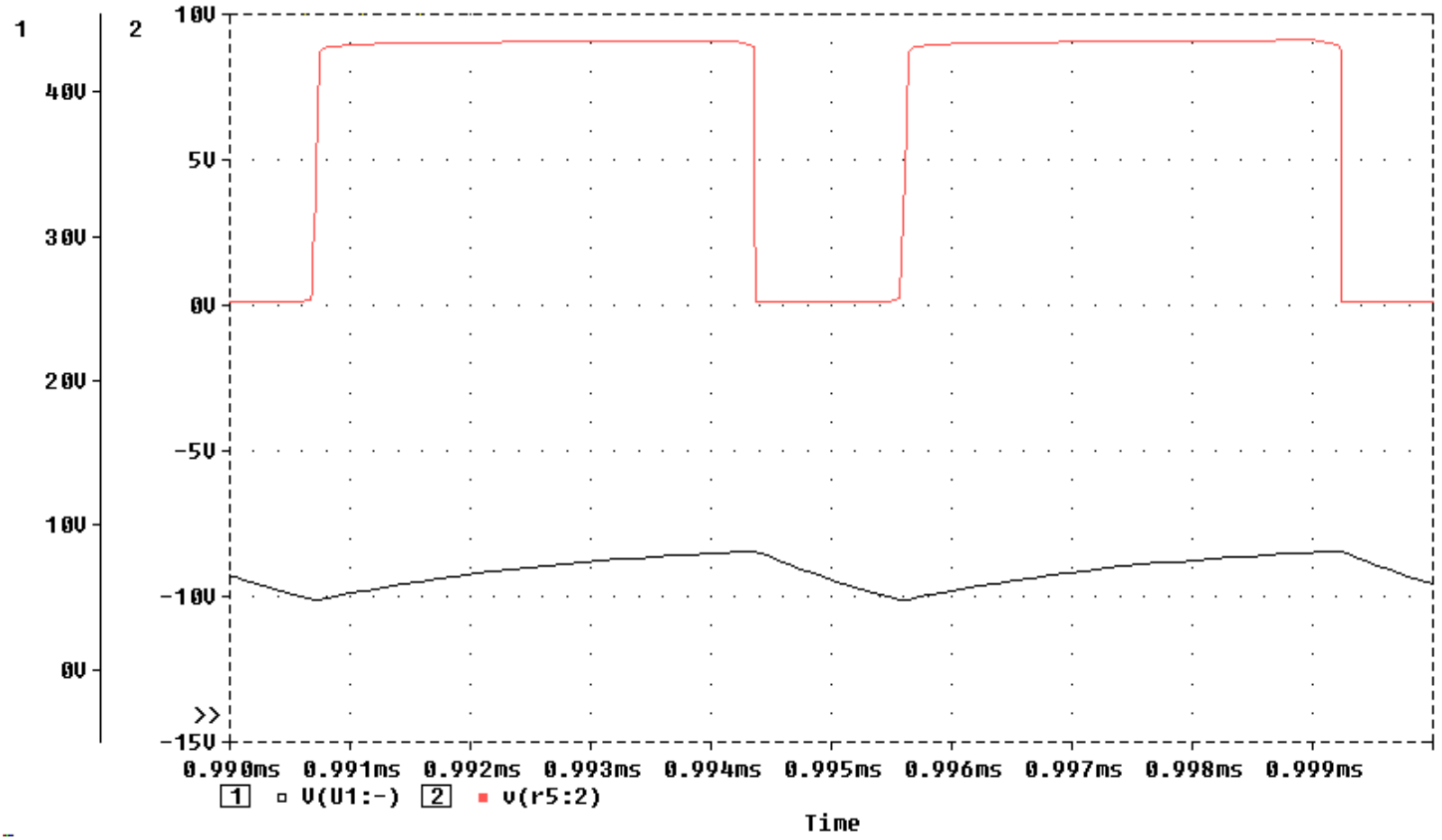
Run Time Summary		
IsSpice v 7.6	Pspice v 6.3	Micro-Cap V v2
6.483 Sec	23.33 Sec	24.448 Sec
Advantages: good pulse amplitude range (100 mV to 5V), runs from single supply		
Disadvantages: high parts count when compared to other solutions.		

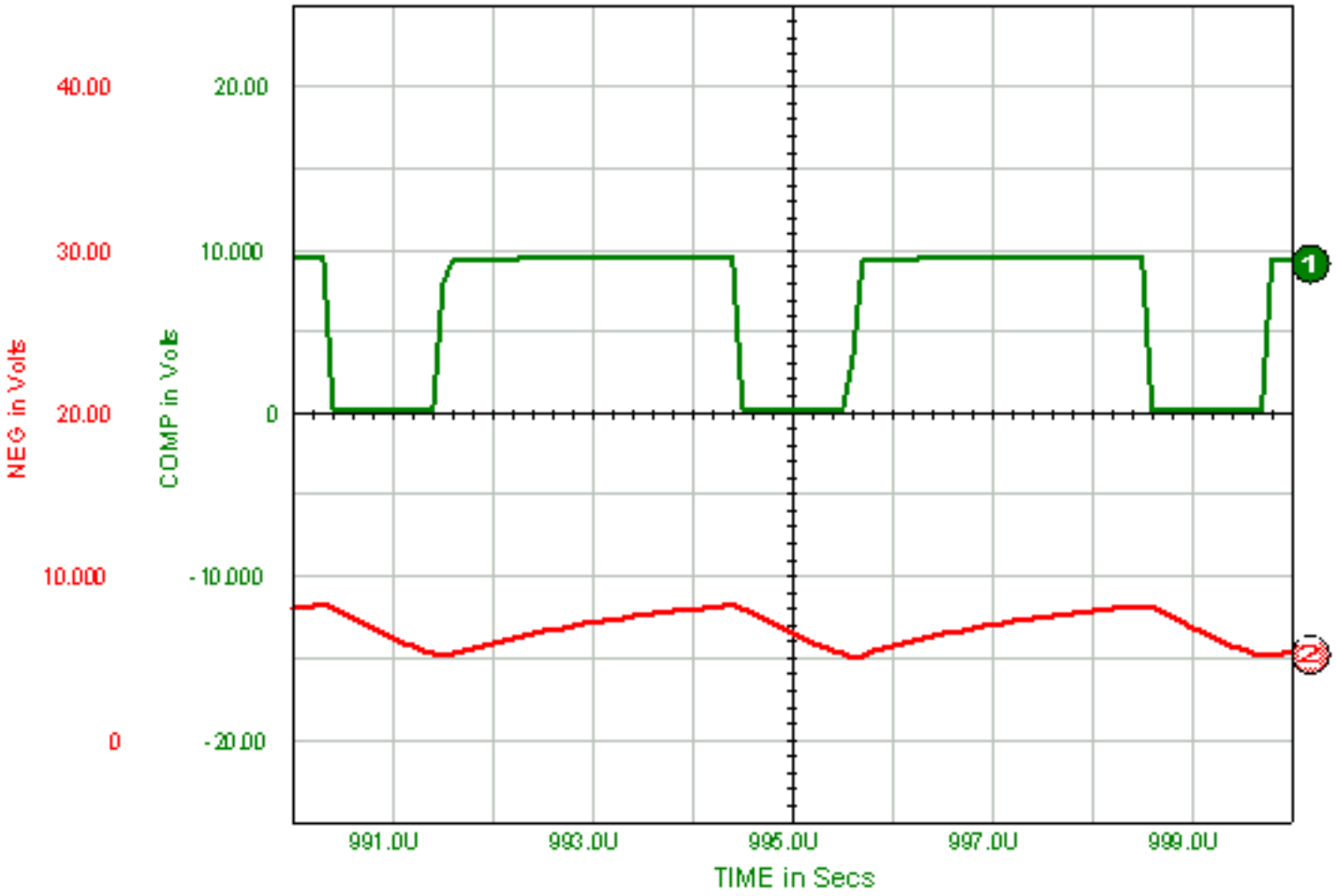
Filenames: mod1 (IsSpice) mod2 (Pspice) mod3 (Microcap)


R6
980
(1K)
V(8)
COMP
R5 46.4K
(47K)
(47K)
R1 46.3K
4
2
V1
15
R2
46.2K
(47K)
V(5)
NEG
5
C1
129P
(100p)
VEE
VCC
X6
LM111T
8
1
6
C2 .486U
(0.47u)
D1 DN4002
V(6)
OUT
R4
17.5K
(18K)
D2
DN4002
C3
.416U
(0.47u)


Tek Run: 50MS/s Sample Trig'd
Ch2 Min
4.2 V
Ch2 Max
10.4 V
1→
2→
Ch1 5 V Ch2 5 V M 1µs Ch1 ∫ 4.8 V
30 Jan 1998
08:11:17


POS2NEGM.CIR Temperature = 27
45.00
30.00
35.00
18.00
25.00
6.00
15.00
-6.00
5.00
-18.00
-5.00
-30.00
989.99u
991.99u
993.99u
995.99u
997.99u
999.99u
v(6)
v(4)
v(2)
T


1
2
10V
40V
5V
30V
0V
20V
-5V
10V
-10V
0V
>>
-15V
0.990ms
0.991ms
0.992ms
0.993ms
0.994ms
0.995ms
0.996ms
0.997ms
0.998ms
0.999ms
1 V(U1:-) 2 v(r5:2)
Time


40.00
30.00
20.00
10.000
0
NEG in Volts
20.00
10.000
0
-10.000
-20.00
COMP in Volts
991.0U
993.0U
995.0U
997.0U
999.0U
TIME in Secs
1
2

#20: Electronic Load using Power BJT Transistors

Figure 20-1 shows the power transistor and sensing circuitry. The entire assembly is powered by a 12 volt DC signal. The collector of transistor Q3 is connected to the +12 volt supply. The emitter of Q3 feeds two high power transistors (Q1 and Q2) connected in a Darlington configuration. The output of the converter that is being tested is connected to the + and - terminals of the assembly as shown in Figure 20-1. The current passes through Q2, through power resistor R5, through sensing resistor R6, and returns to the negative terminal of the converter. The voltage across sense resistor R6 is sensed through two 1K resistors (R7, R9) and fed into the input terminals of an TL084 operational amplifier. The 1K resistors are matched in resistance in order to minimize the effects of input offset currents of the TL084. The TL084 (X1) is configured in a differential mode configuration. This allows the floating signal across R6 to be referenced to the ground of the X2 amplifier for comparison to the fixed voltage reference. The sensed signal from the X1 operational amplifier is fed into the inverting terminal of the TL084 (X2)and compared to the fixed reference voltage being supplied at Vc. The output of X2 feeds the base of transistor Q3, thereby completing the loop and allowing exact control of the load current. Capacitor C1 ensures stability. Resistors R2-R4 provide noise immunity so stray currents do not turn on or off the transistors. Resistor R1 and R11 reduce switching spikes while still providing high slew rate.

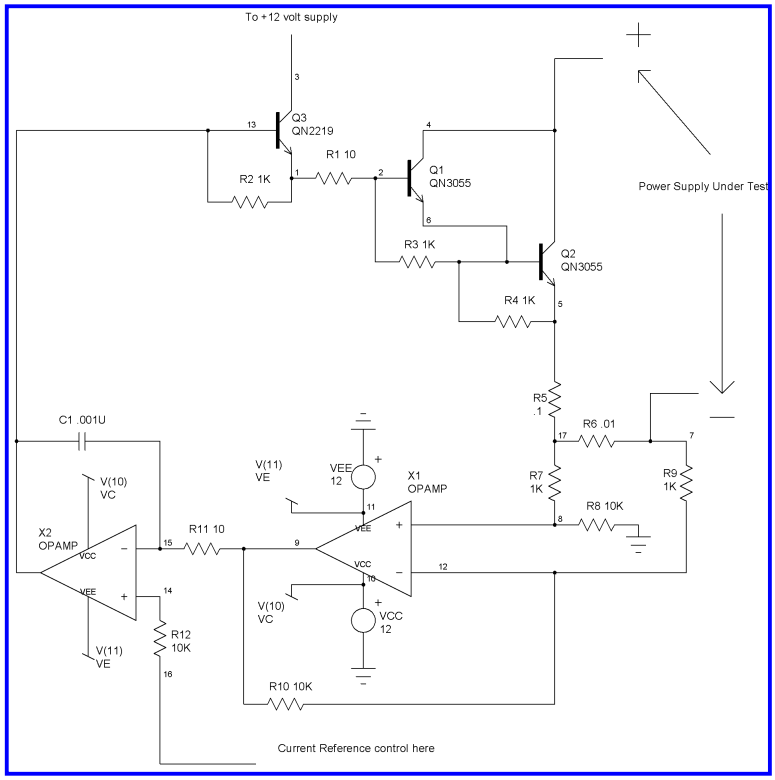


Figure 20-1: DC output comparison summary

One problem (or should we say challenge) of designing this type of circuit is to ensure the Darlington pair transistors are not overstressed by causing them to dissipate too much power. The maximum power the transistor can dissipate decreases with increasing collector-emitter voltage.

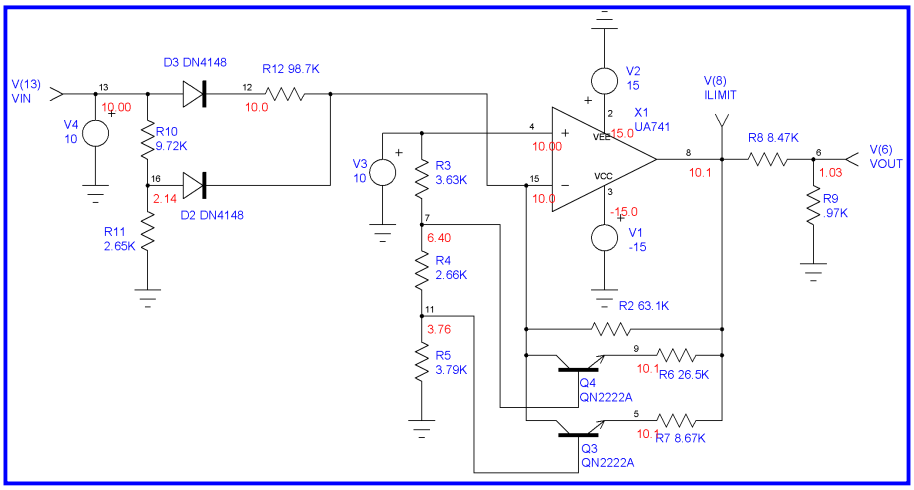


Figure 20-2: Current reference and power limiter schematic

A circuit was designed for this load which allows the electronic load to take full advantage of the power rating of the power transistor. This circuit is shown in Figure 20-2. The collector-emitter voltage is sensed through D3 and R12. The voltage signal is fed into the inverting terminal of the operational amplifier X1 (UA741). This voltage is compared to a reference voltage, generated by a ten volt precision reference IC. At collector-emitter voltages of less than 10 volts, the load is limited to 10 amps. As the collector-emitter voltage increases, transistors Q1 and Q2 turn on and, utilizing non linear feedback, allows the limiter circuit to approximate the 110/V load. Above 50 volts, a diode coupled divider substantially increases the slope to limit the transistor within the $I_{s/b}$ portion of the safe operating region. If the collector-emitter voltage exceeds that set by this circuit, the electronic load is current limited by pulling the control pin to ground via diode. The data book current limit of the transistor

used is shown in Figure 20-3. The resulting power curve as created by the IsSpice model is shown in Figure 20-4 and the curve created by the breadboard is shown in Figure 20-5. Microcap and Pspice results are shown in Figures 20-6 and 20-7 respectively.

Click Here to see the larger Image

Figure 20-3: Collector Current vs. Vce voltage for 2N3055 (reprinted with permission from Motorola Inc. ®)

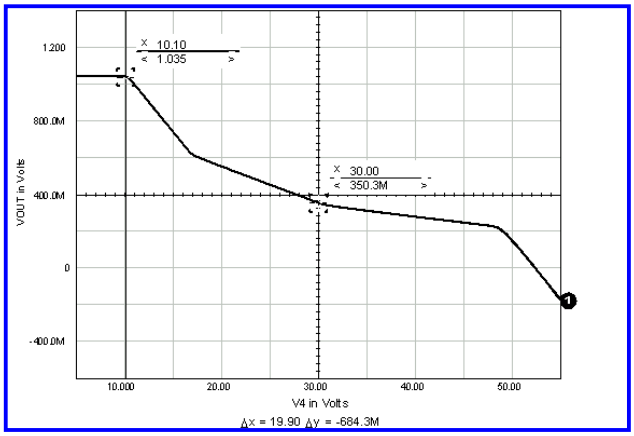


Figure 20-4: IsSpice results of safe operation region circuitry

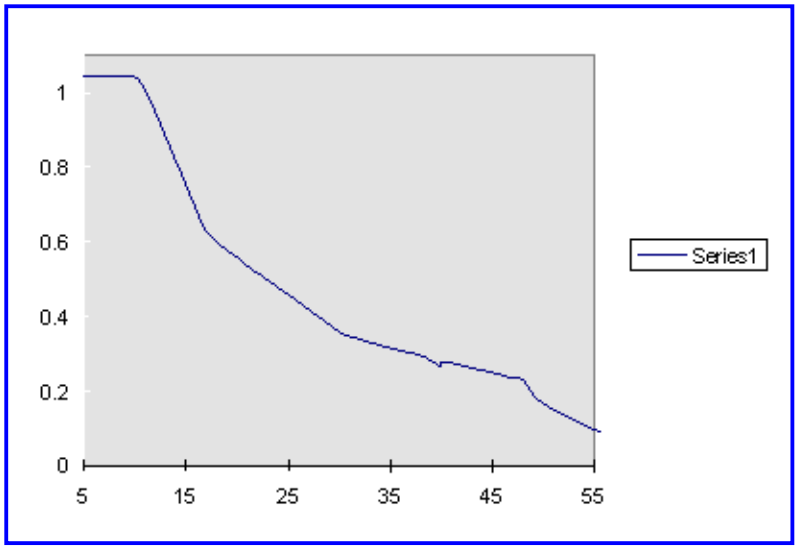


Figure 20-5: Breadboard results of safe operation region circuitry

Click Here to see the larger Image

Figure 20-6: Microcap results of safe operation region circuitry

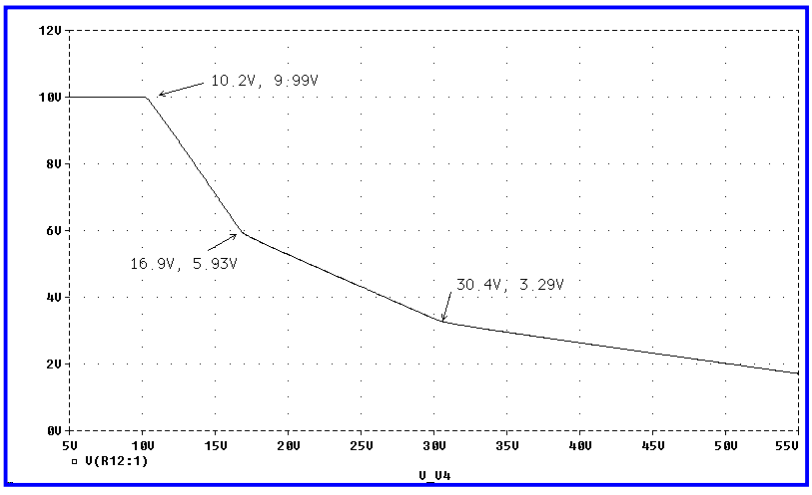


Figure 20-7: Pspice results of safe operation region circuitry

Run Time Summary

IsSpice v 7.6	Pspice v 6.3	Micro-Cap V v2
2.05 Sec	6.77 Sec	2.94 Sec
Advantages: BJT transistors less expensive (typically) than Mosfet transistors		
Disadvantages: Extra circuitry required to create power limiting of transistors		

Filenames: Load (IsSpice) Load_mc (Microcap) PS_Load (Pspice)

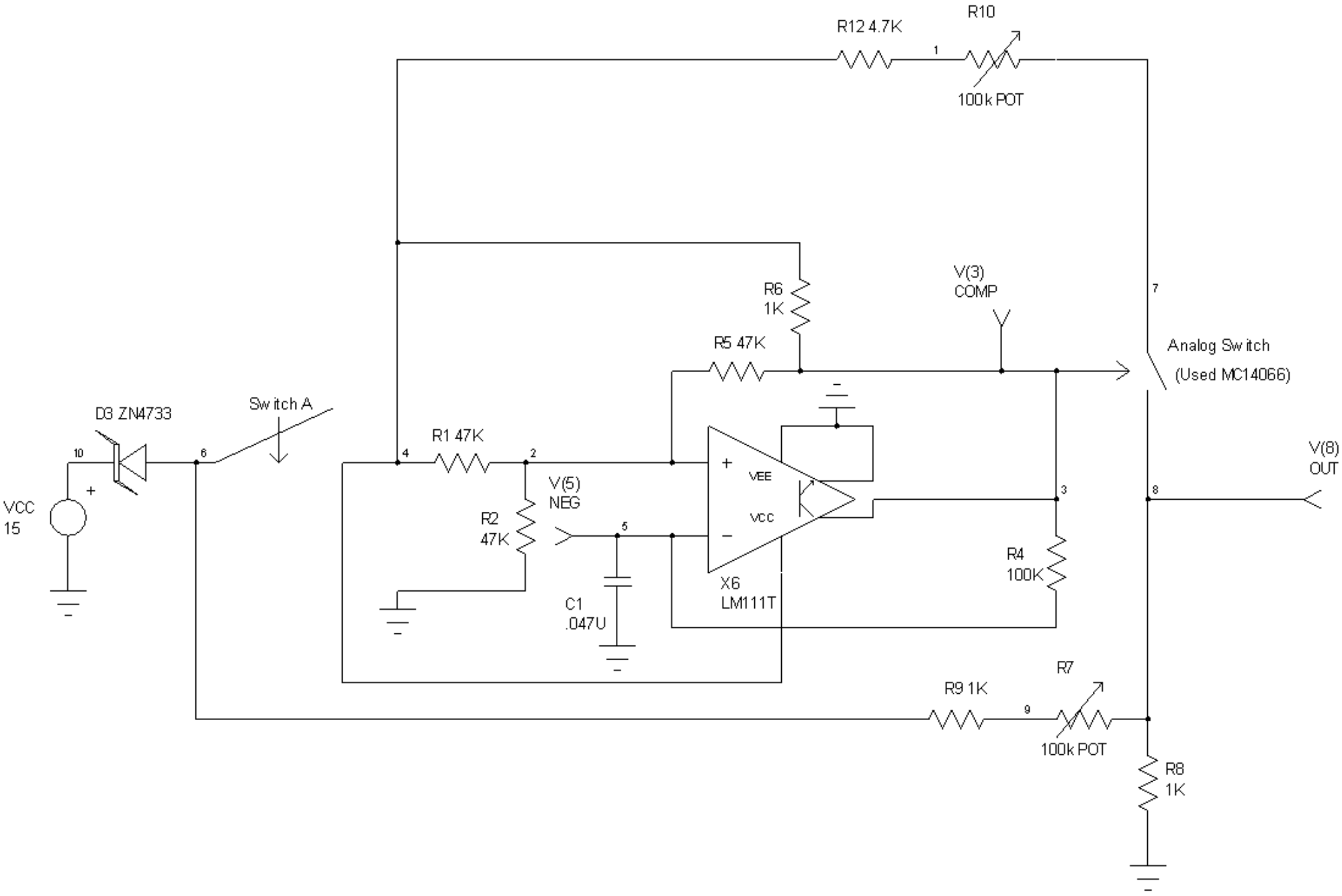
References

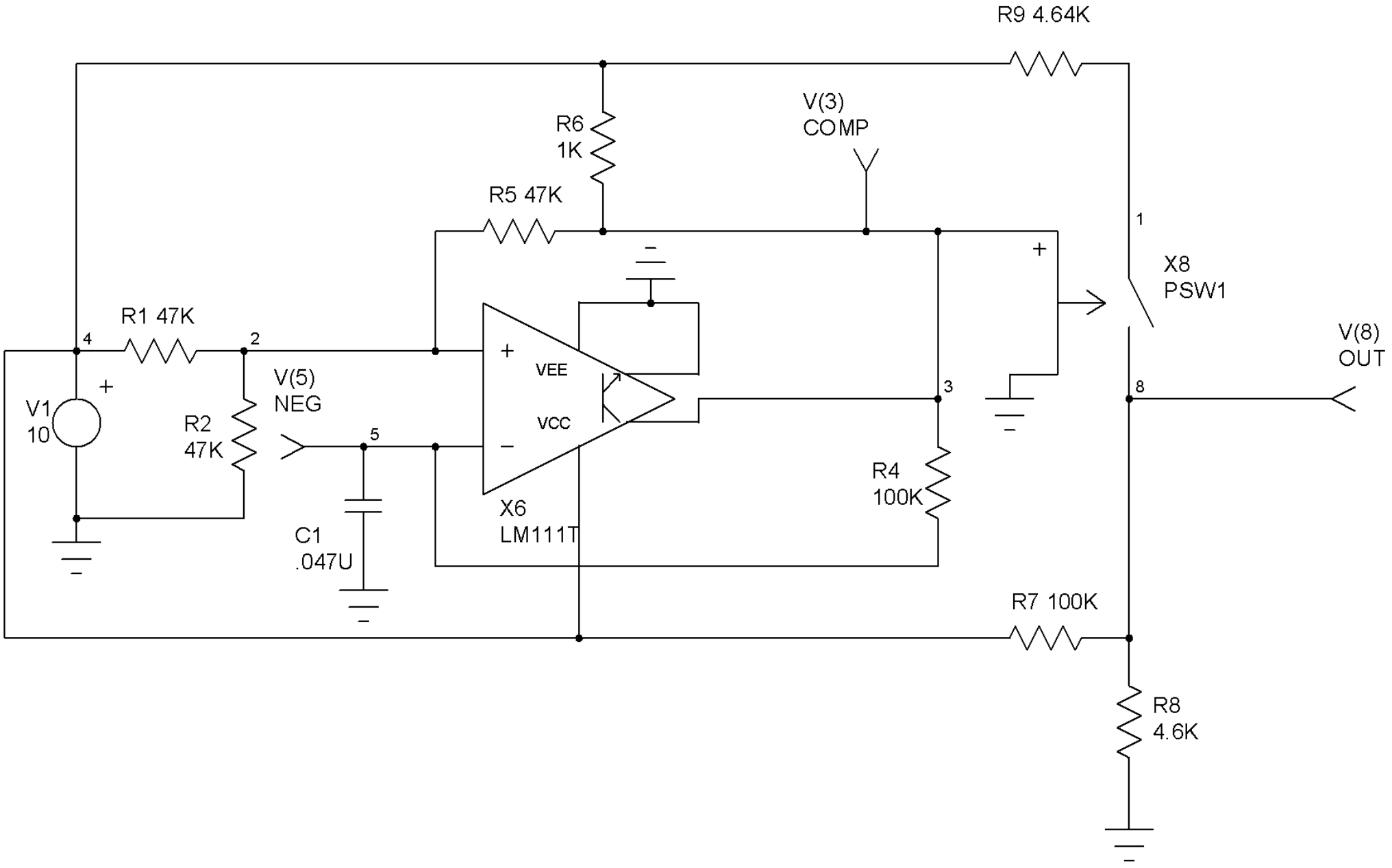
Motorola, 1982. Motorola Power Data Book. Third Edition.

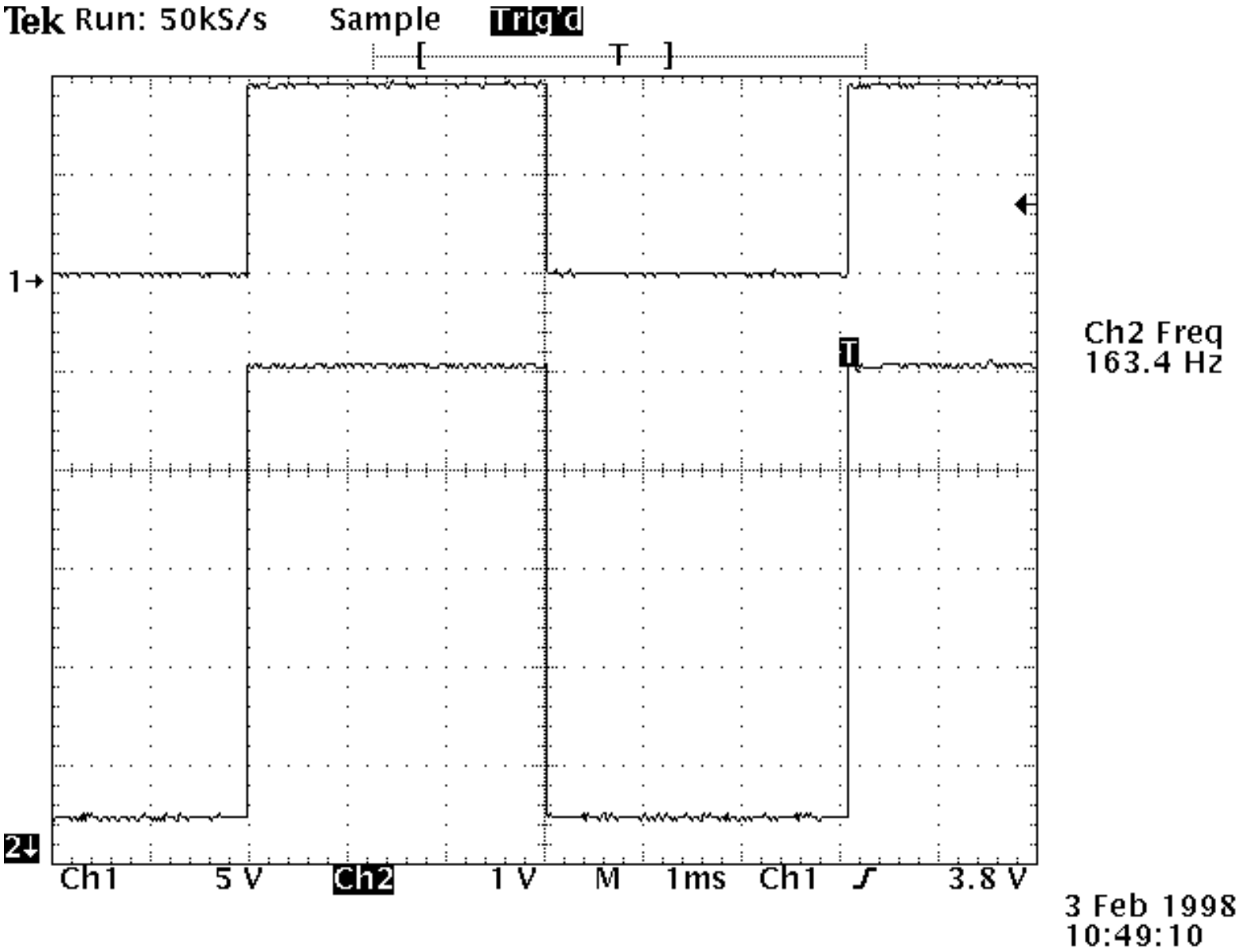
Parker, Sybil, ed. 1984. Concise Encyclopedia of Science and Technology. New York: McGraw Hill

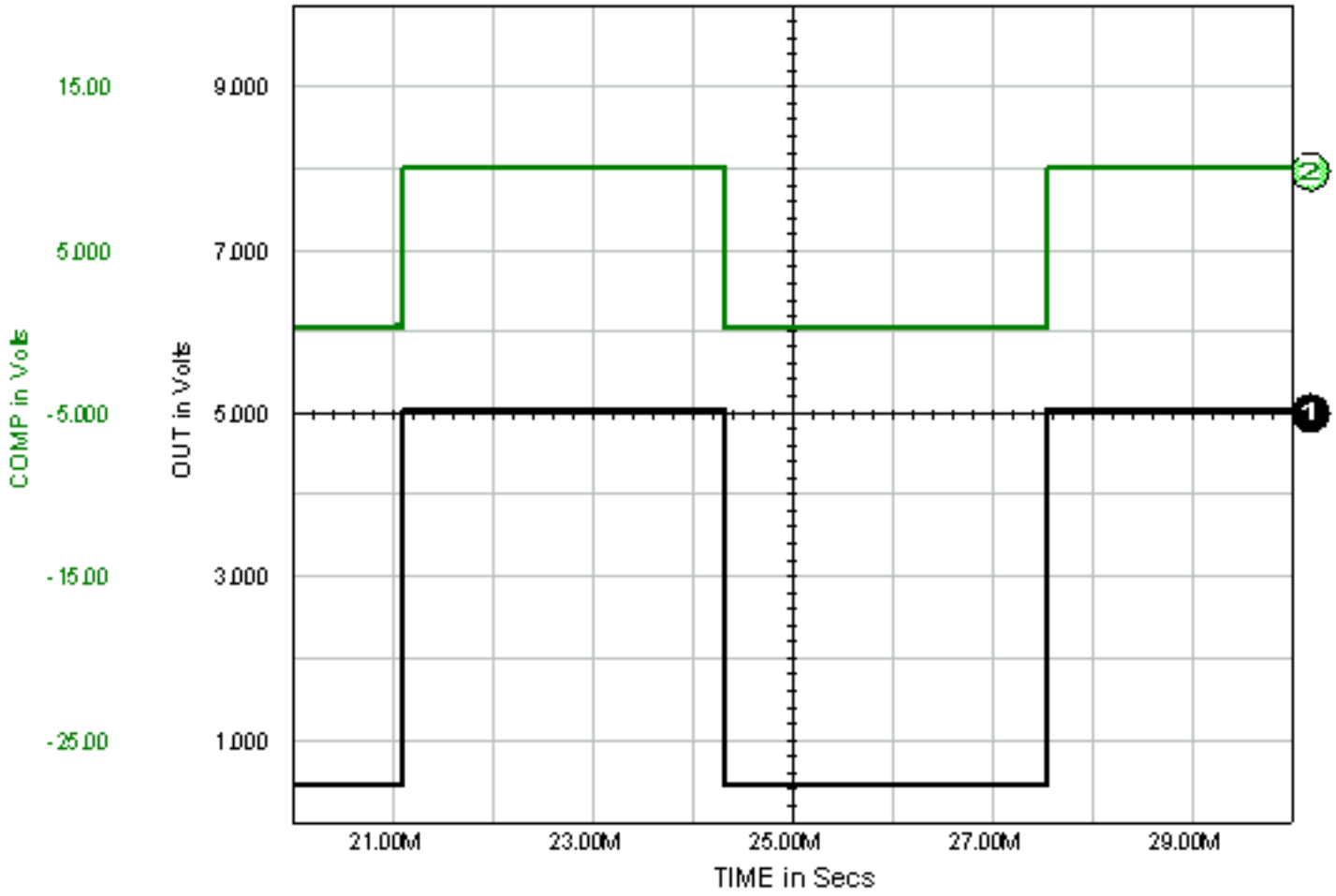
Texas Instruments, 1992. Linear Circuits Data Book Volume 3.

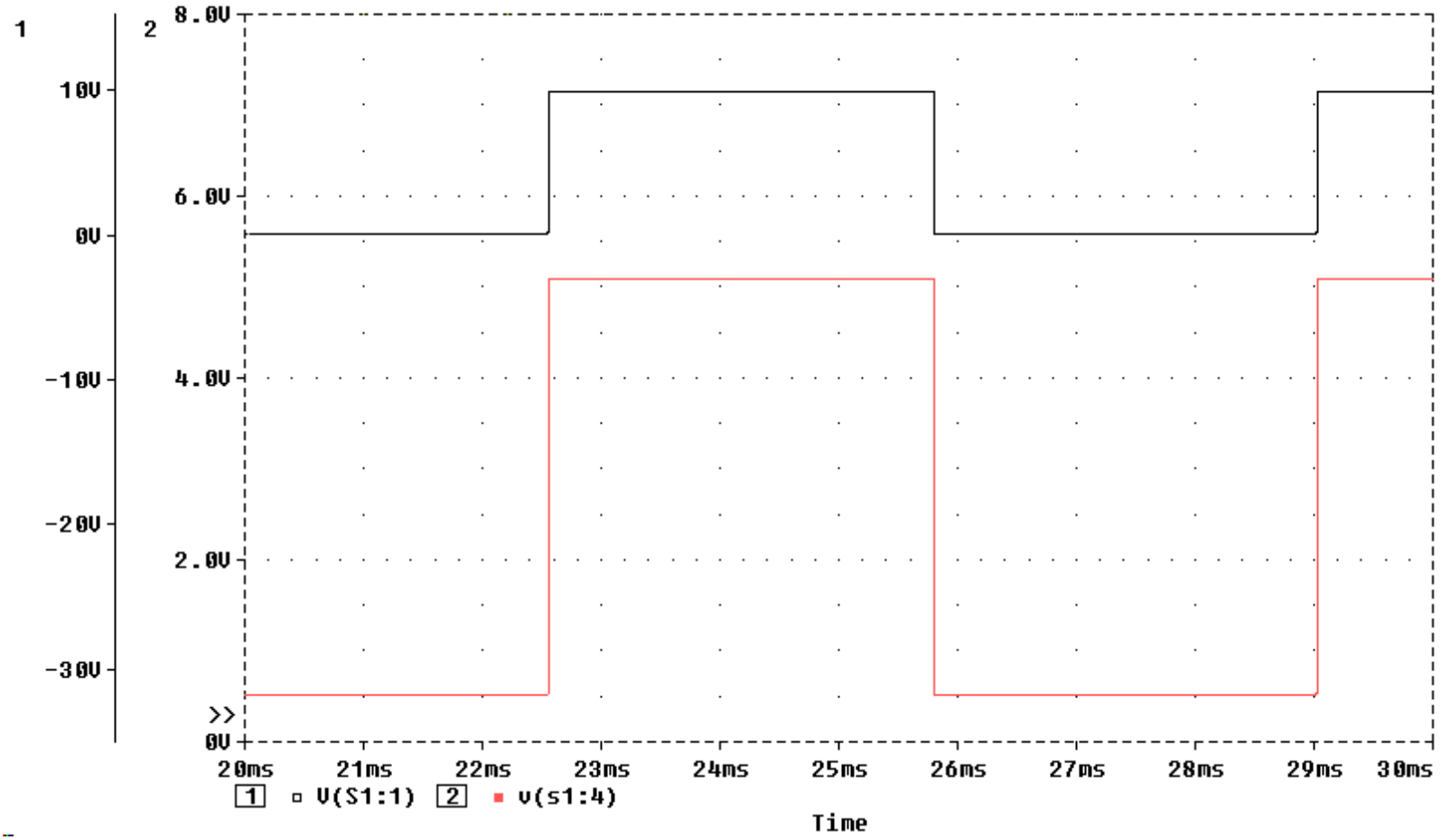
Van Valkenburg, M.E. 1982. Analog Filter Design. New York: Harcort Brace Jovanovich College Publishers.

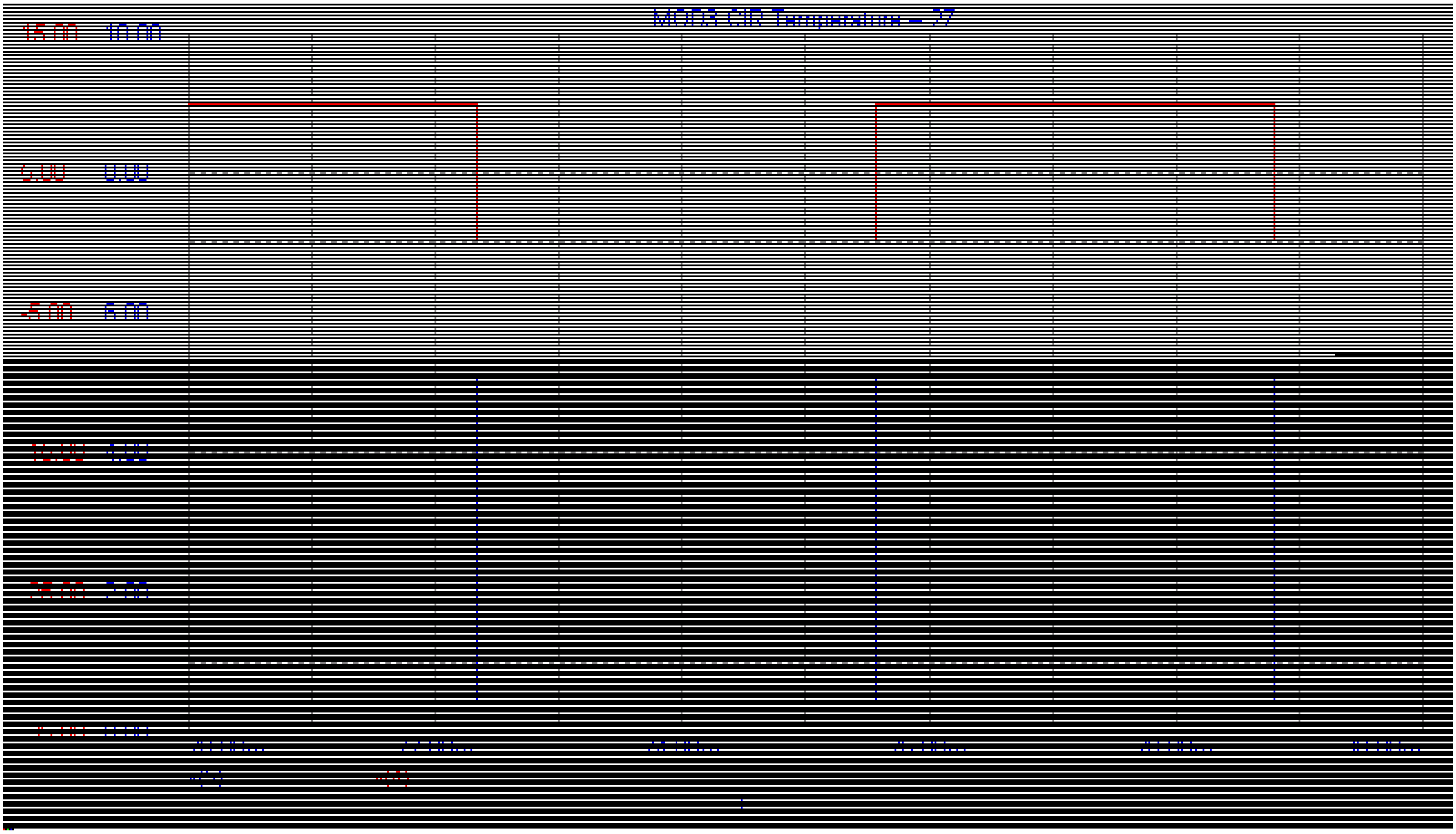

R12 4.7K
R10
1
100k POT
R6
1K
R5 47K
V(3)
COMP
7
Analog Switch
(Used MC14066)
D3 ZN4733
Switch A
10
6
4
R1 47K
2
V(5)
NEG
R2
47K
5
C1
.047U
VEE
VCC
X6
LM111T
3
R4
100K
8
V(8)
OUT
VCC
15
R9 1K
9
R7
100k POT
R8
1K


R9 4.64K
R6
1K
V(3)
COMP
R5 47K
1
X8
PSW1
V(8)
OUT
R1 47K
4
2
V(5)
NEG
V1
10
R2
47K
5
C1
.047U
VEE
VCC
X6
LM111T
3
8
R4
100K
R7 100K
R8
4.6K


Tek Run: 50kS/s Sample Trig'd
Ch2 Freq
163.4 Hz
Ch1 5 V Ch2 1 V M 1ms Ch1 3.8 V
3 Feb 1998
10:49:10


15.00
5.000
-5.000
-15.00
-25.00
COMP in Volts
9.000
7.000
5.000
3.000
1.000
OUT in Volts
21.00M
23.00M
25.00M
27.00M
29.00M
TIME in Secs
2
1

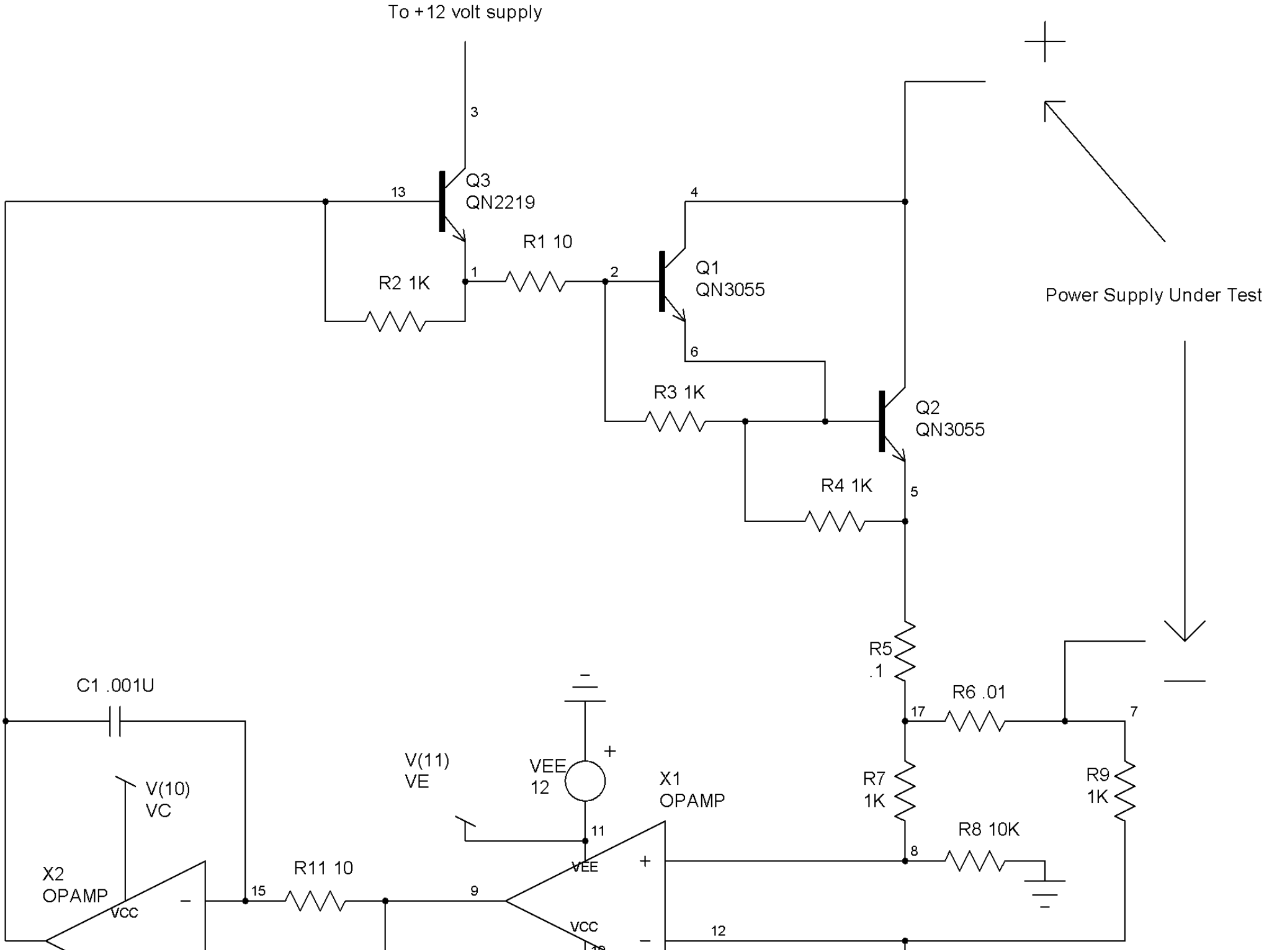

1
2
8.0V
10V
6.0V
0V
-10V
4.0V
-20V
2.0V
-30V
>>
0V
20ms
21ms
22ms
23ms
24ms
25ms
26ms
27ms
28ms
29ms
30ms
1 V(S1:1) 2 v(s1:4)
Time

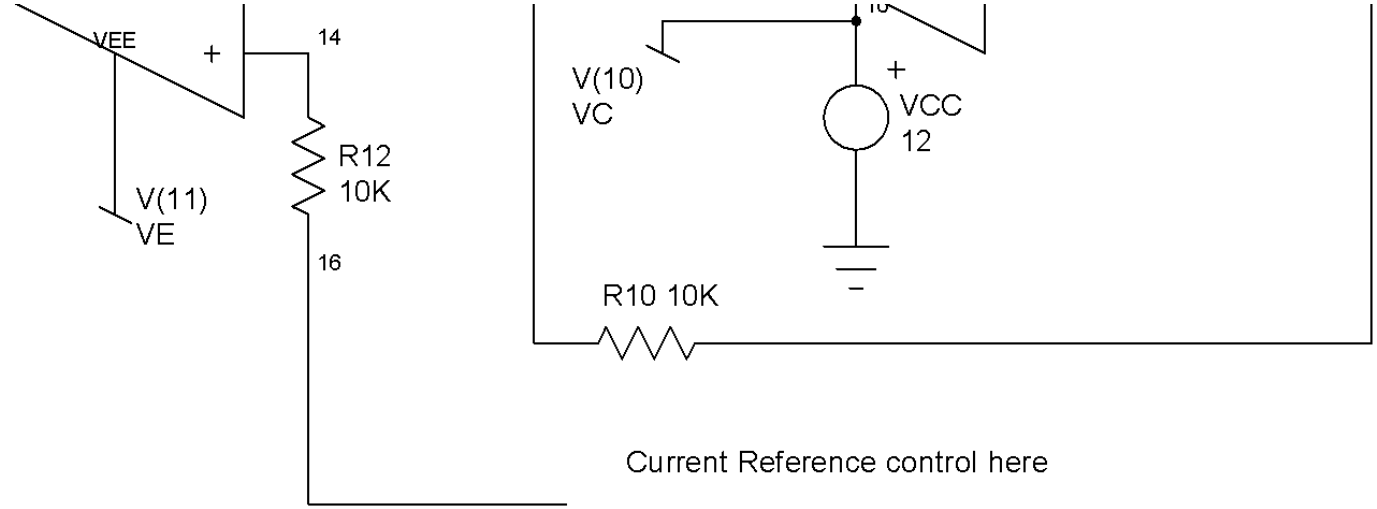

MOD3 CIR Temperature = 27
15.00
10.00
5.00
0.00
-5.00
6.00

6
Instrumentation Circuits

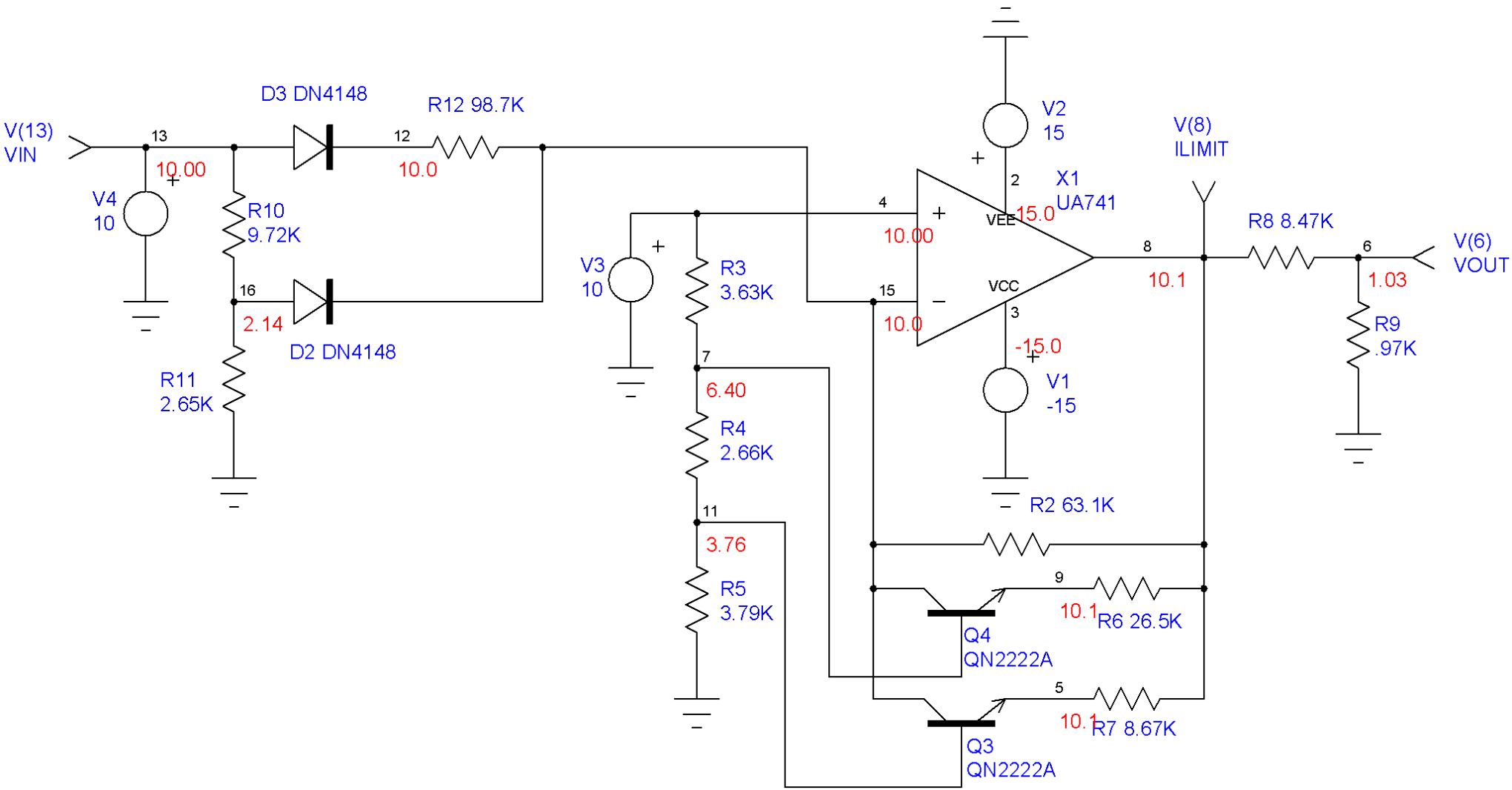
Instrumentation circuits are unique. The wide definition of "instrumentation" suggests these are circuits that are not central to the operation of the system, but are critical to the testing and implementation of that system. These circuits act as telemetry signals, allowing remote users to monitor the inner workings of the system without it's disassembly. Other applications include internal test points, which provide the same function to the test technician who would like to monitor signals internal to the system without opening the system up or disrupting the operation of the system

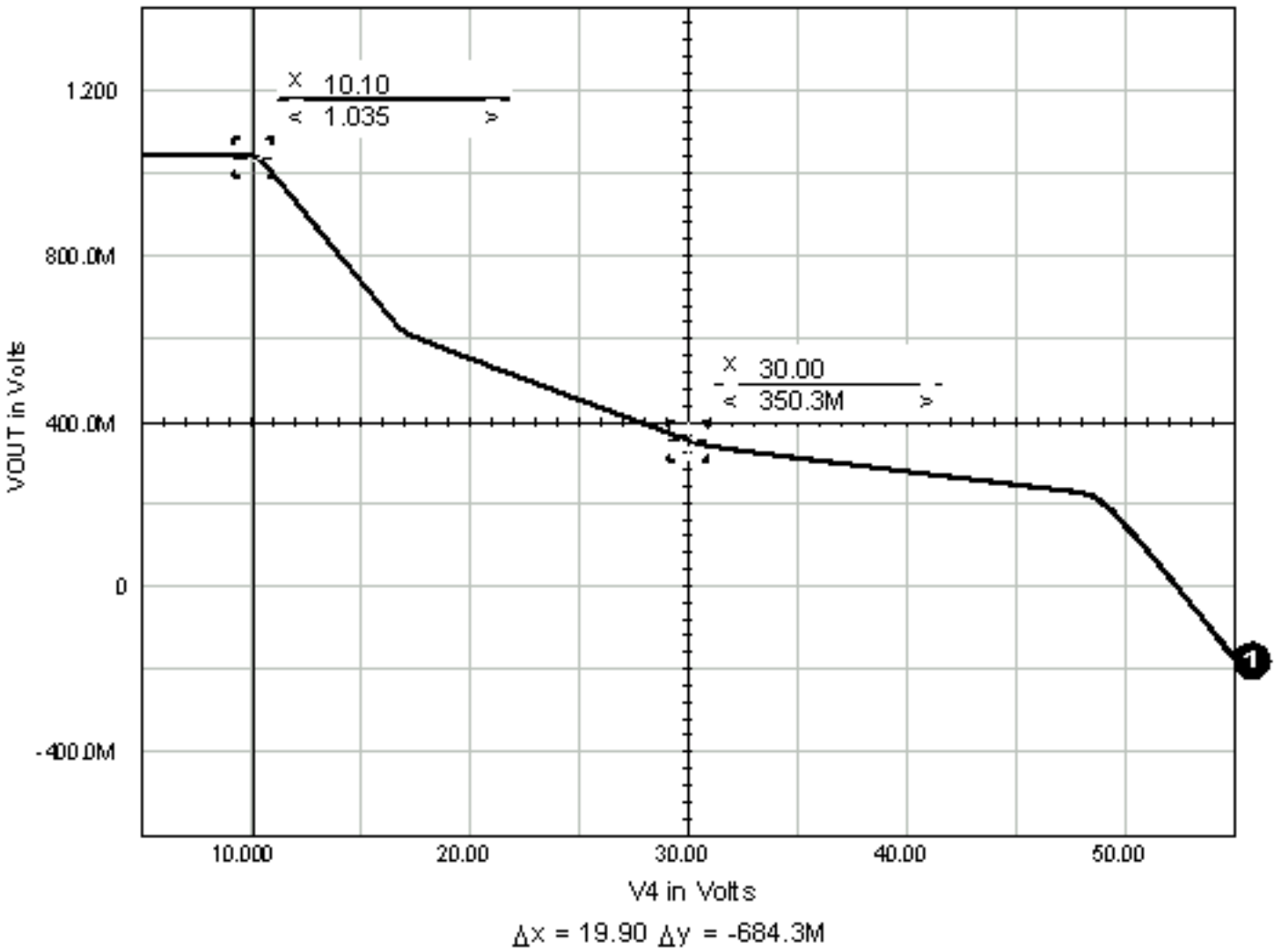
The wide variety of applications and circuits that fit under this category also suggests individual and unique obstacles to the proper operation and simulation of these circuits. This chapter will allow the designer to identify those obstacles and avoid them.

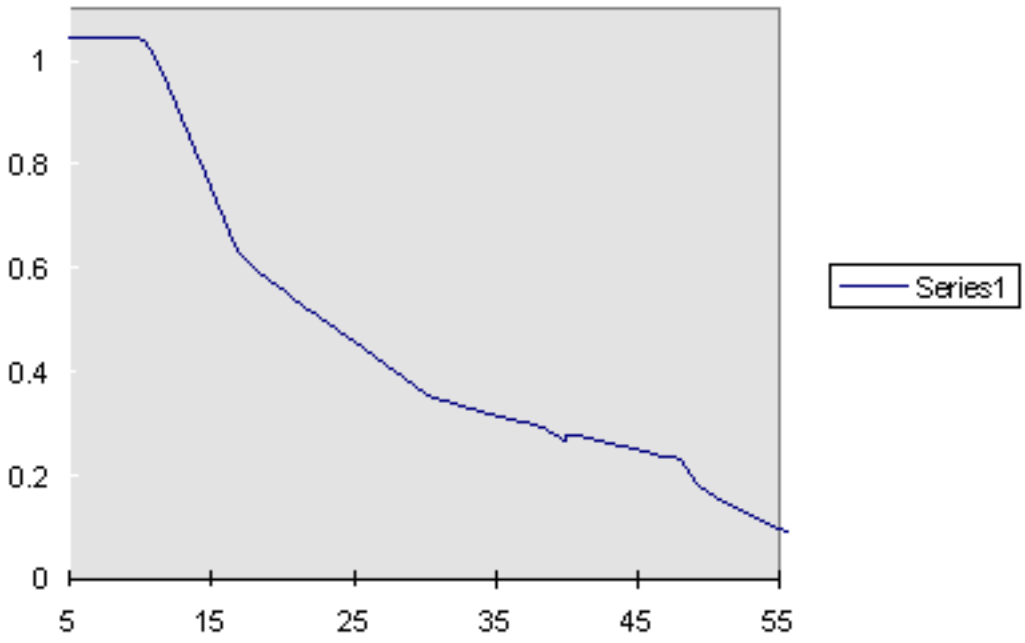

To +12 volt supply
3
Q3
QN2219
13
4
R1 10
1
2
Q1
QN3055
R2 1K
Power Supply Under Test
6
R3 1K
Q2
QN3055
R4 1K
5
R5
.1
C1 .001U
R6 .01
17
7
V(11)
VE
VEE
12
+
X1
OPAMP
R7
1K
R9
1K
V(10)
VC
11
R8 10K
X2
OPAMP
VEE
8
R11 10
15
9
VCC
VCC
12

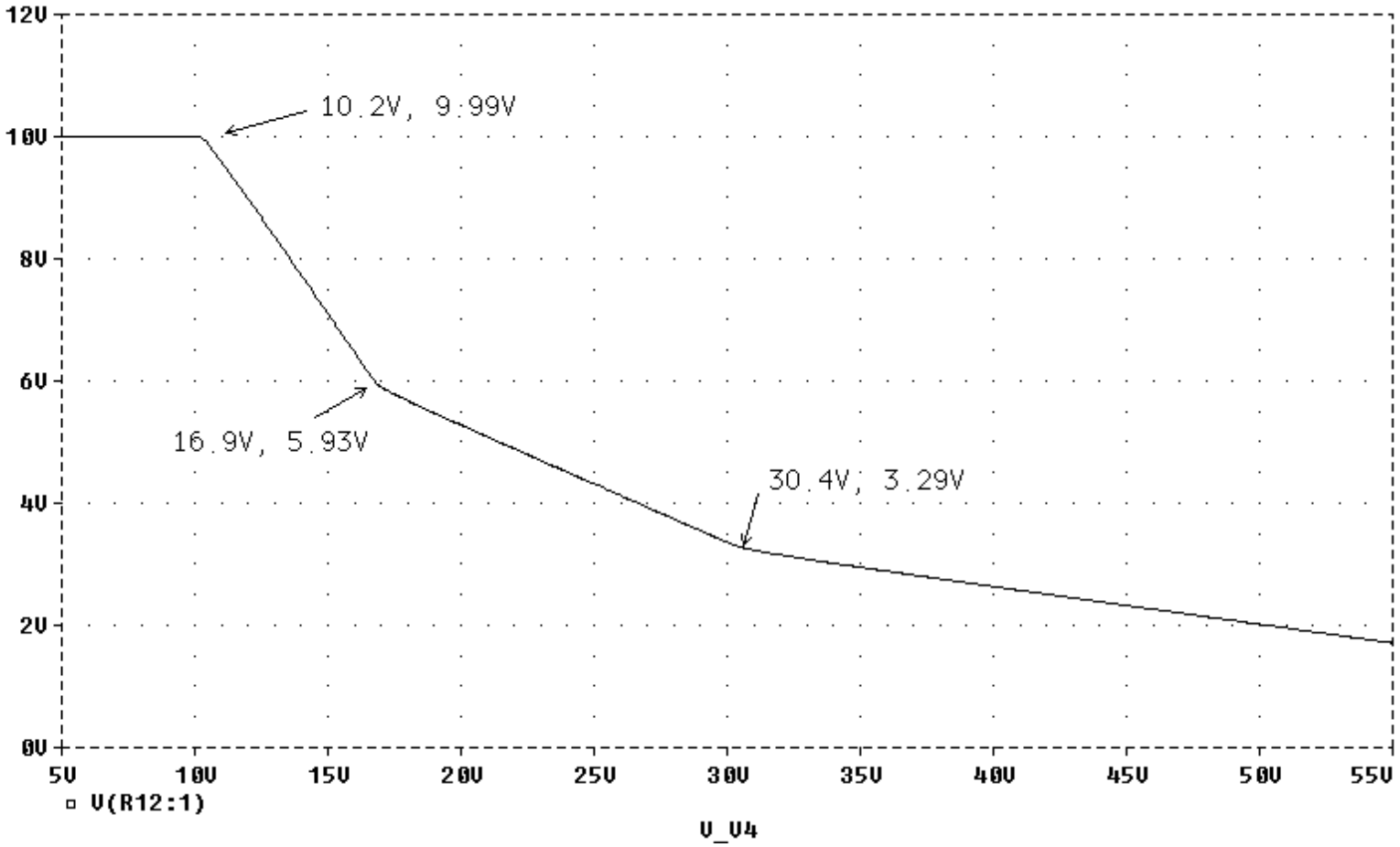


Current Reference control here


V(13)
VIN
13
10.00
V4
10
R10
9.72K
16
2.14
R11
2.65K
D3 DN4148
D2 DN4148
12
10.0
R12 98.7K
V3
10
R3
3.63K
7
6.40
R4
2.66K
11
3.76
R5
3.79K
V2
15
2
X1
UA741
4
10.00
15.0
VEE
15
10.0
VCC
3
-15.0
V1
-15
R2 63.1K
V(8)
ILIMIT
8
10.1
R8 8.47K
6
1.03
R9
.97K
V(6)
VOUT
9
10.1
R6 26.5K
Q4
QN2222A
5
10.1
R7 8.67K
Q3
QN2222A


X 10.10
< 1.035 >
X 30.00
< 350.3M >
1.200
800.0M
400.0M
0
-400.0M
VOUT in Volts
10.000
20.00
30.00
40.00
50.00
V4 in Volts
Δx = 19.90 Δy = -684.3M


1
0.8
0.6
0.4
0.2
0
5
15
25
35
45
55
Series1


12V
10V
8V
6V
4V
2V
0V
10.2V, 9.99V
16.9V, 5.93V
30.4V, 3.29V
5V
10V
15V
20V
25V
30V
35V
40V
45V
50V
55V
V(R12:1)
V_V4

#21: 555 Timer

The versatility of the 555 Timer Integrated circuit is shown time and again in the number of circuit requirements that can be satisfied with this IC.

The original purpose of this IC was to provide a one shot timer. A schematic for this circuit is shown in Figure 21-1.

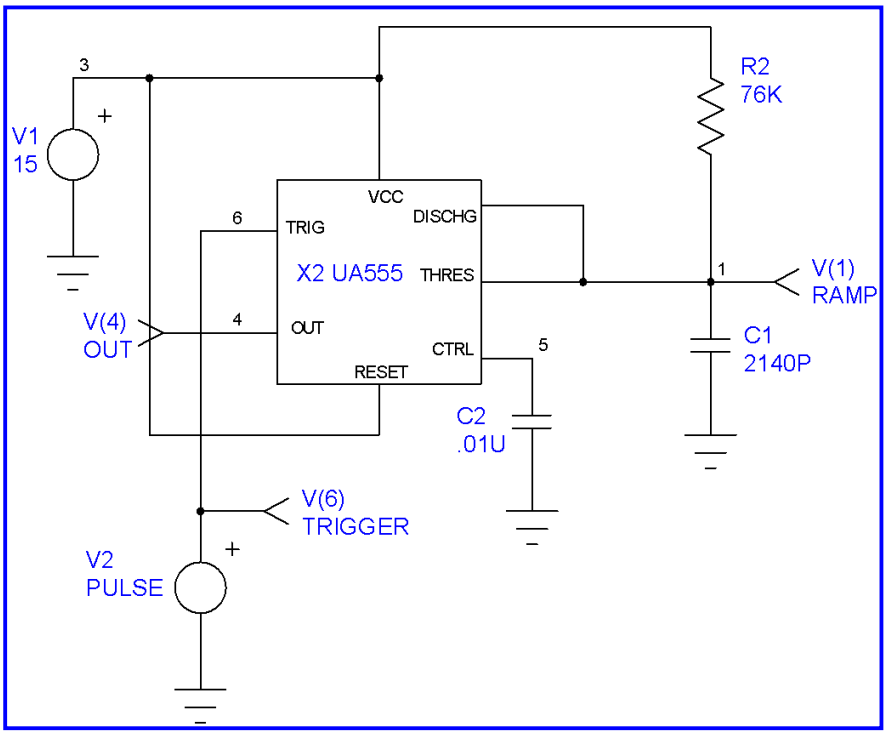


Figure 21-1: Schematic of 555 One Shot Timer Circuit

When the pulse V2 transitions low, the timer is started. Capacitor C1 begins to charge through resistor R2. During the charging time, the output of the 555 is high. When the voltage at the threshold pin reaches 2/3 of the Vcc voltage (in this example, the Vcc is 15 volts, so the trip point of the threshold pin is 10 volts), the output transistions low. The V2 source uses a PULSE statement of the following syntax:

PULSE 0 15 0 100N 100N 900U 1M

The above PULSE statement translates to a square wave pulse with an

amplitude from 0 to 15 volts, 100 nSec rise and fall times, and a 1mSec period with a 90 % duty cycle.

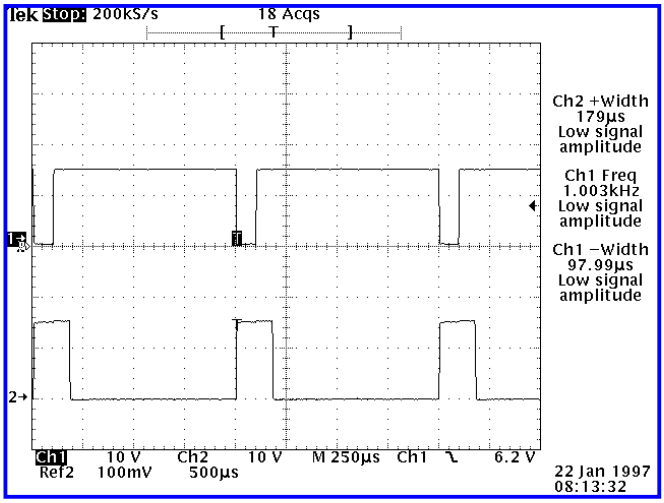


Figure 21-2: Breadboard input and output signal waveforms

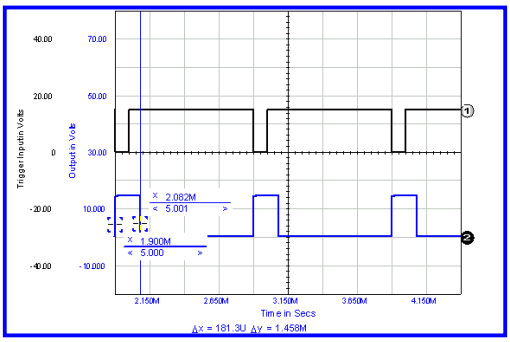


Figure 21-3: IsSpice input and output signal waveforms

Examining the results of Figure 21-2 and 21-3, the operation of the 555 IC is apparent. When the input (trigger) voltage transistions low, the clock function is started and ends 181 uSec later (in this example).

One other interesting waveform is the threshold pin voltage. This is shown in Figure 21-4. When the input (trigger) voltage transitions low, the capacitance of C1 begins to charge through R2 until reaching the 2/3 Vcc voltage.

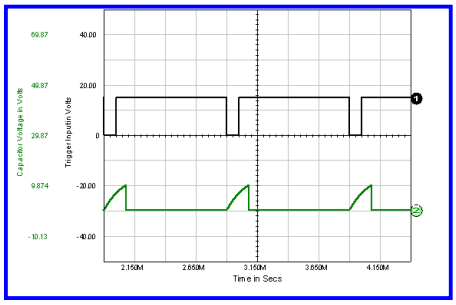


Figure 21-4: IsSpice input and threshold signal waveforms

This circuit was also constructed in Pspice, and Microcap. The resulting waveforms are shown in Figures 21-5 through 21-6.

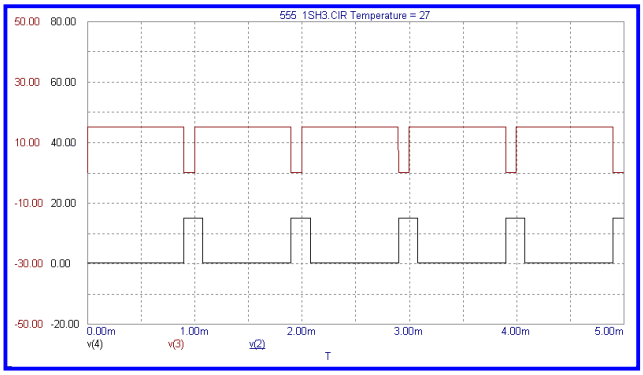


Figure 21-5A: Microcap input and output waveforms

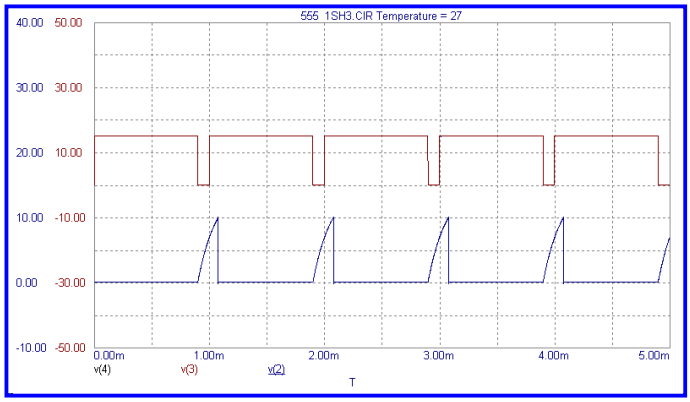


Figure 21-5B: Microcap input and Threshold waveforms

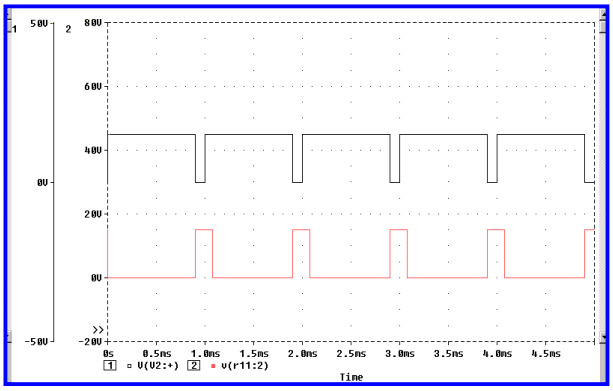


Figure 21-6A: Pspice input and output waveforms

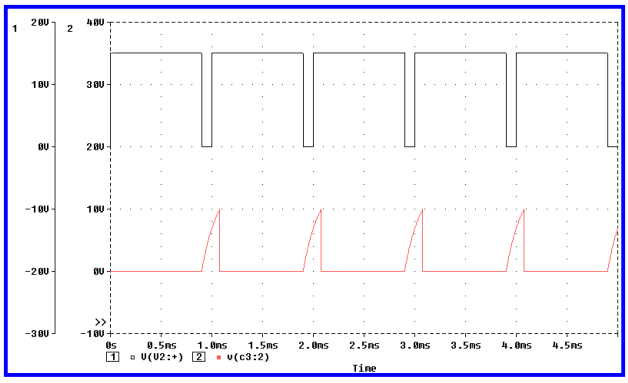


Figure 21-6B: Pspice input and trigger waveforms

Run Time Summary		
IsSpice v 7.6	PsPice v 6.3	Micro-Cap V v2
17.783 Sec	4.11 Sec	84.8 Sec
Advantages: Low parts count		
Disadvantages:		

Filenames: 555_1sht (IsSpice) 555_1sh3 (Micro-cap) 555_1sh2 (Pspice)

#22: 555 Missing Pulse Detector

With a few components, the 555 timer can be configured to detect missing pulses in a data stream. The schematic configuration for this type of configuration is shown in Figure 22-1.

Figure 22-1: 555 Configured as a missing pulse detection circuit

This circuit is actually a clever use of the timer characteristic of the 555. As long as the pulse spacing is less than the timing interval generated by R2 and C1. Therefore, this circuit not only detects missing pulses, but variations in duty cycle, variations in frequency, even a terminated pulse stream. Figure 22-2 shows the breadboard in detection mode, with the output pulse high (no missing pulses detected) and the input pulse train on top. Figure 22-3 shows the result when the input pulse (top) terminates.

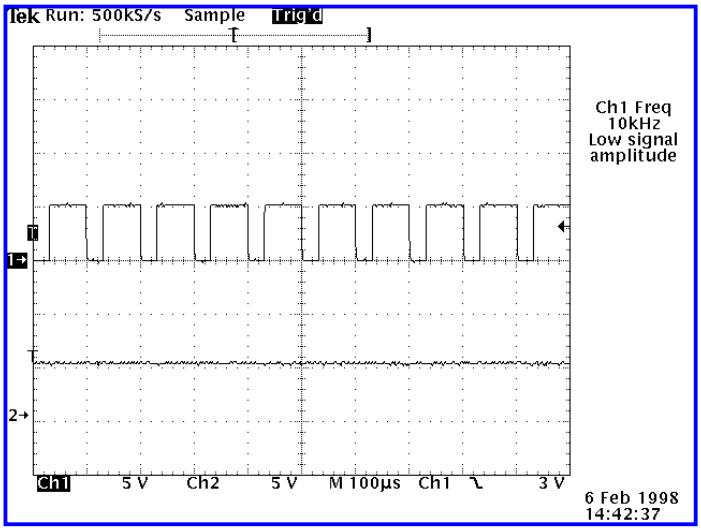


Figure 22-2: Normal operation, no pulses skipped

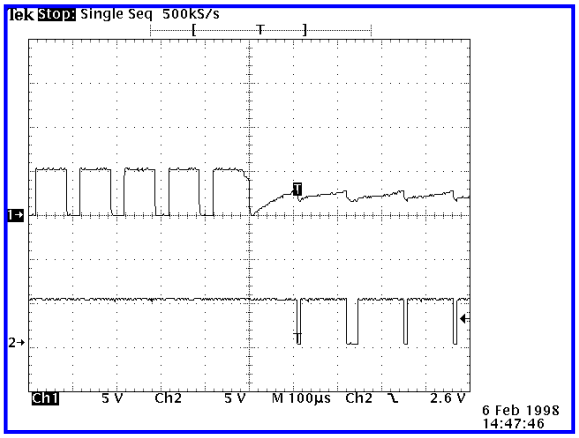


Figure 22-3: Pulse stream terminated, detection pulse triggered

In Figure 22-4, the effect of the frequency increasing also triggers the detection pulses.

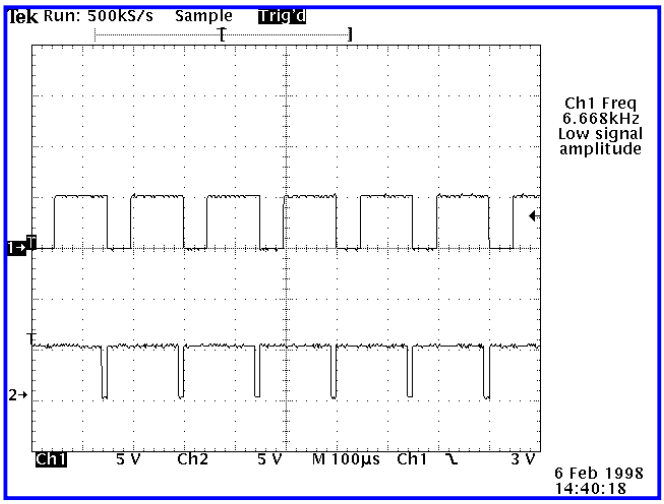


Figure 22-4: Frequency increased, detection pulse triggered

The SPICE models were tested slightly differently than the breadboard. The SPICE test schematic is shown in Figure 22-5.

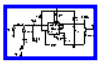


Figure 22-5: SPICE circuit test schematic

Voltage source V2 used a command of PULSE 0 5 0 100N 100N 80U 100U while the voltage source V3 used a command of PULSE 0 7 500U 100N 100N 200U 1. The resulting input and output waveforms are shown in Figure 22-6A. The threshold waveform is also measured and shown in Figure 22-6B.

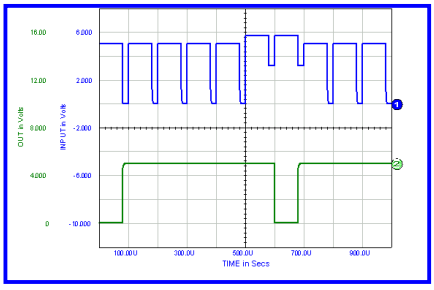


Figure 22-6A: IsSpice Input and Output waveforms

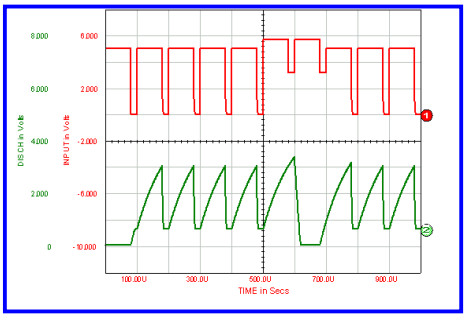


Figure 22-6B: IsSpice Input and Threshold waveforms

The results of the Pspice and Microcap simulations of this circuit are shown in Figures 22-7 and 22-8.

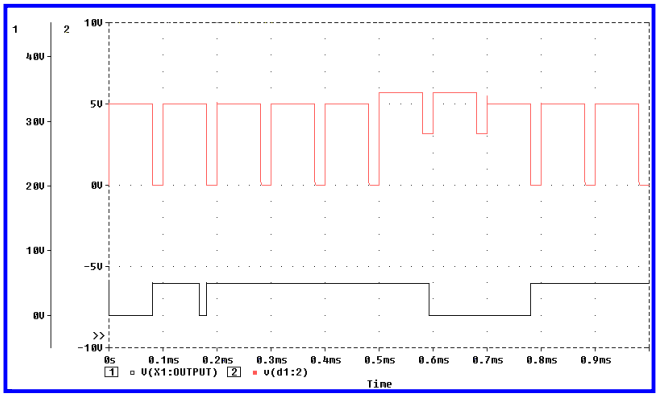


Figure 22-7A: Pspice Input and Output waveforms

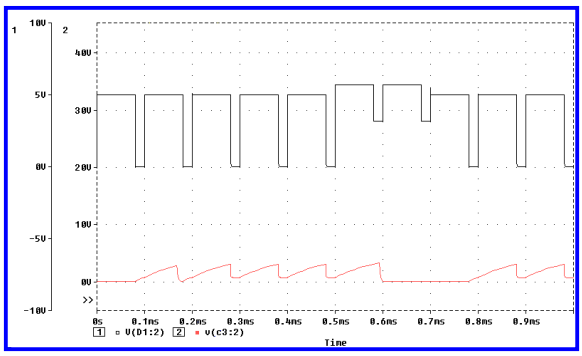


Figure 22-7B: Pspice Input and Threshold waveforms

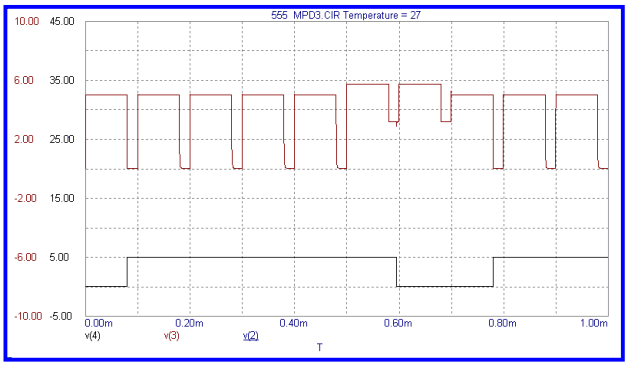


Figure 22-8A: Microcap Input and Output waveforms

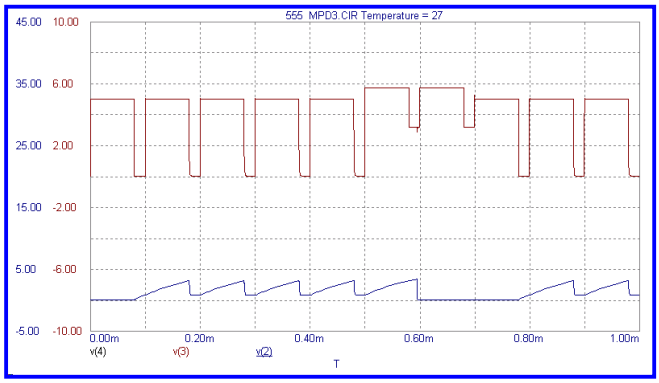
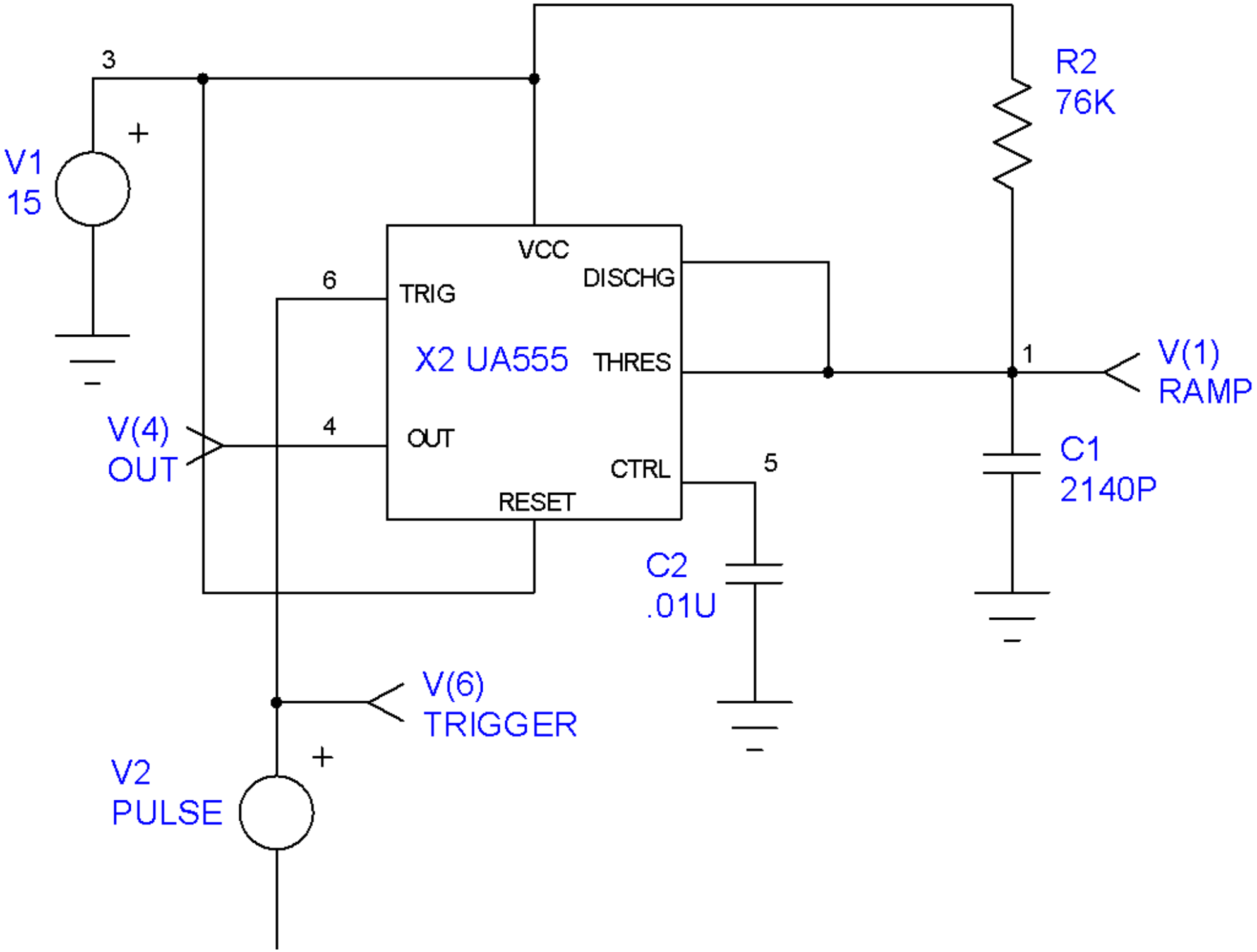
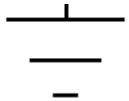


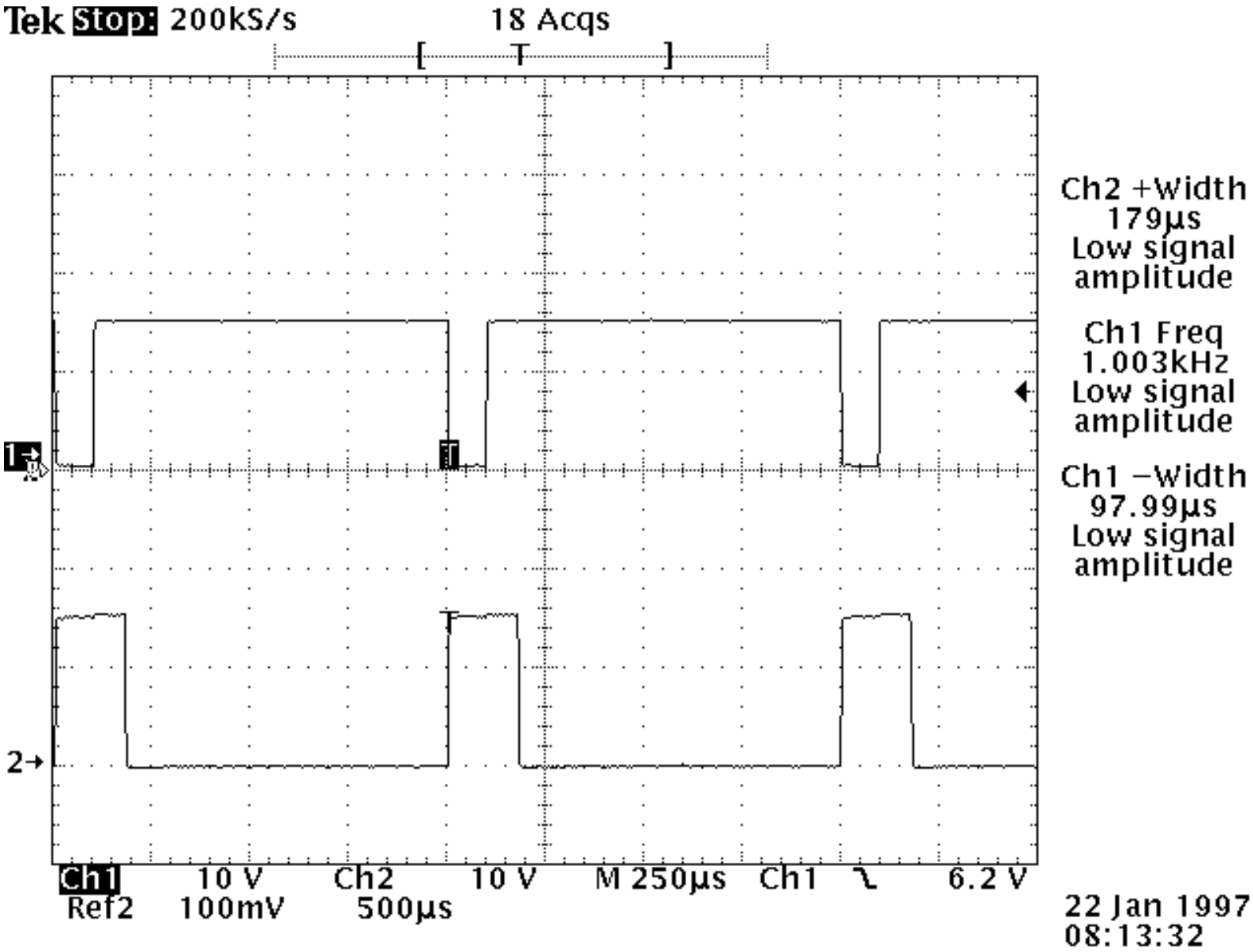
Figure 22-8B: Microcap Input and Threshold waveforms

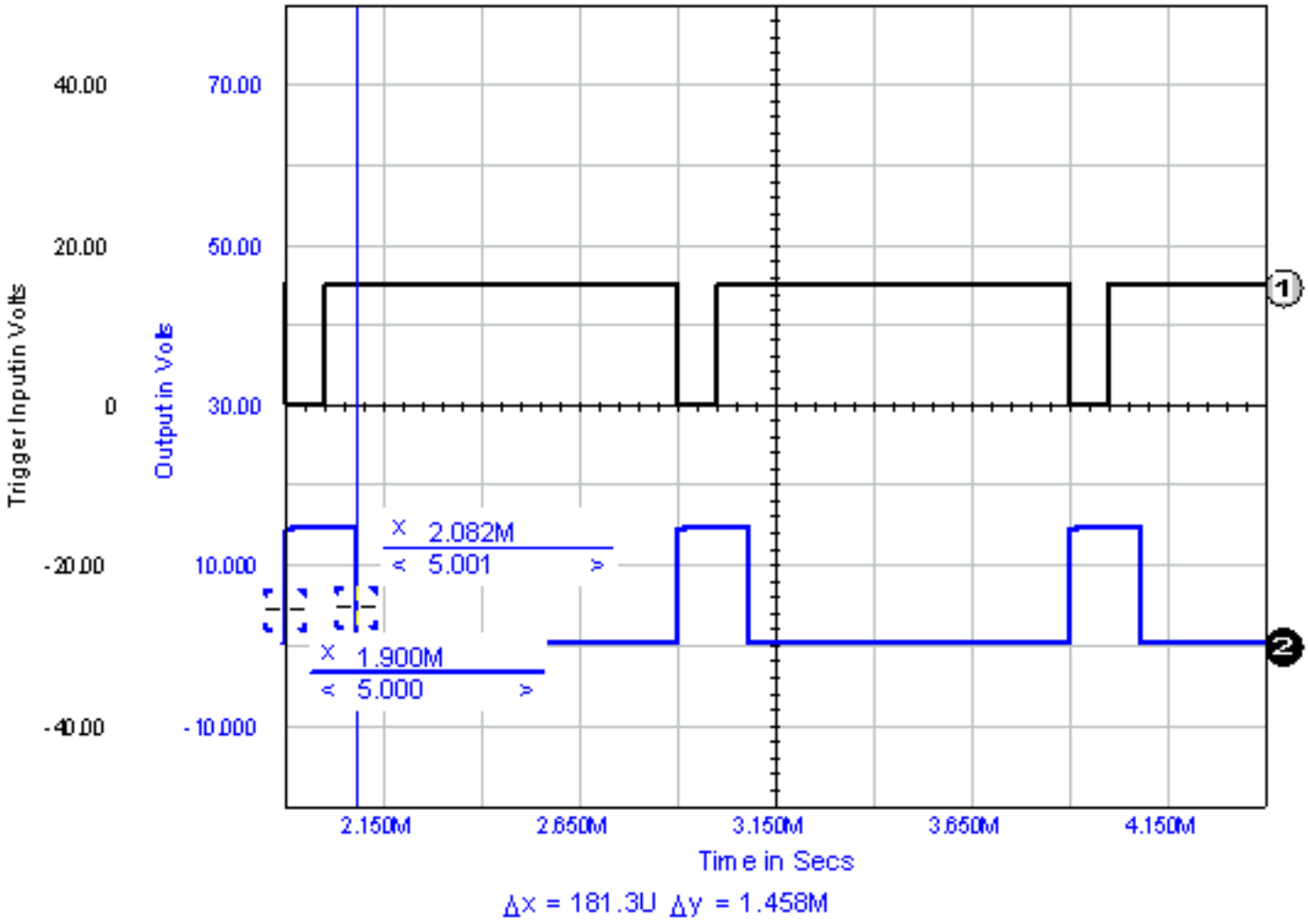
Run Time Summary		
IsSpice v 7.6	PsPice v 6.3	Micro-Cap V v2
20.65 Sec	3.05 Sec	17.664 Sec
Advantages: Low parts count		
Disadvantages: Not a true missing pulse detection circuit, actually a timer circuit		

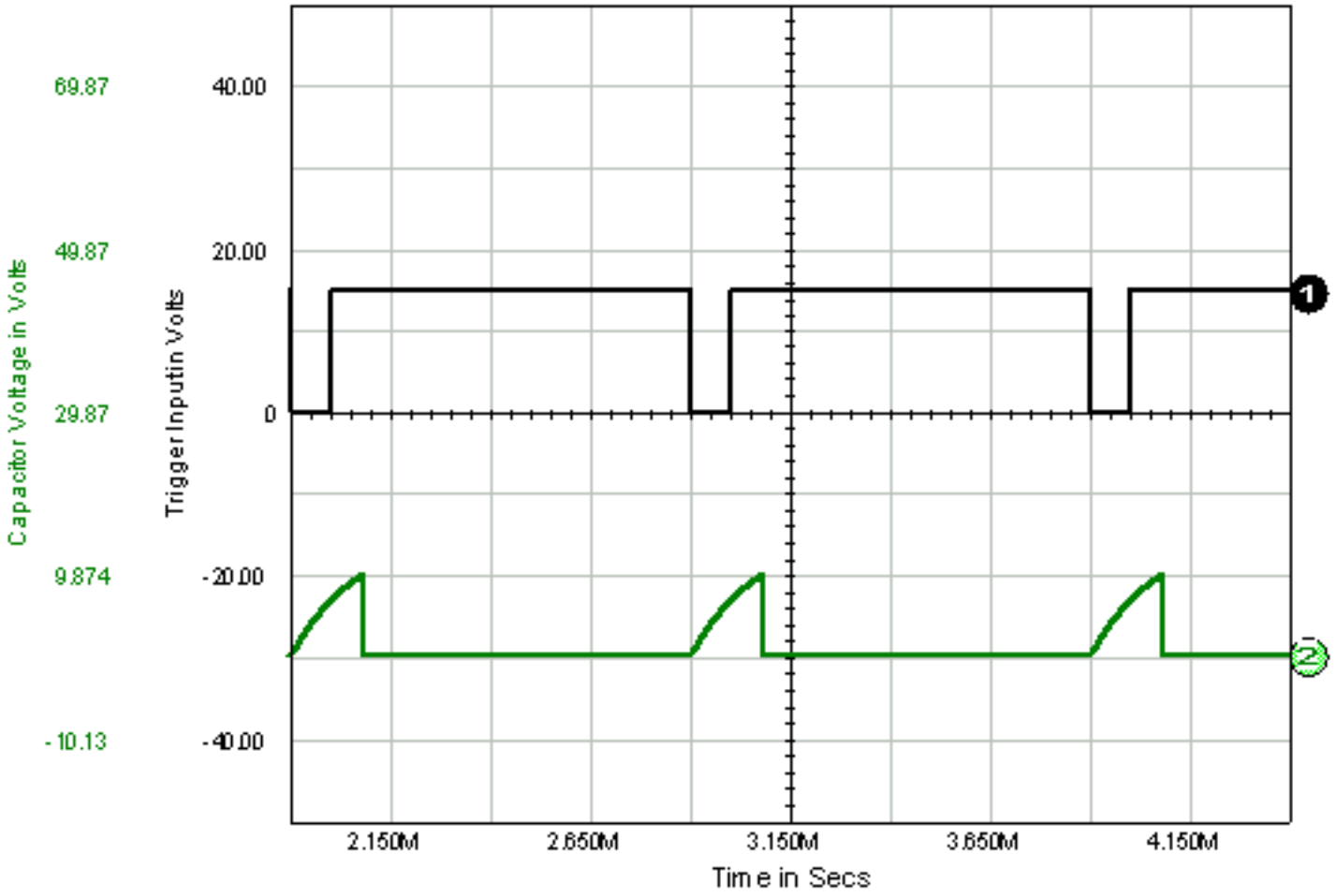
Filenames: 555_mpd (IsSpice) 555_mpd2 (Pspice) 555_mpd3 (Microcap)

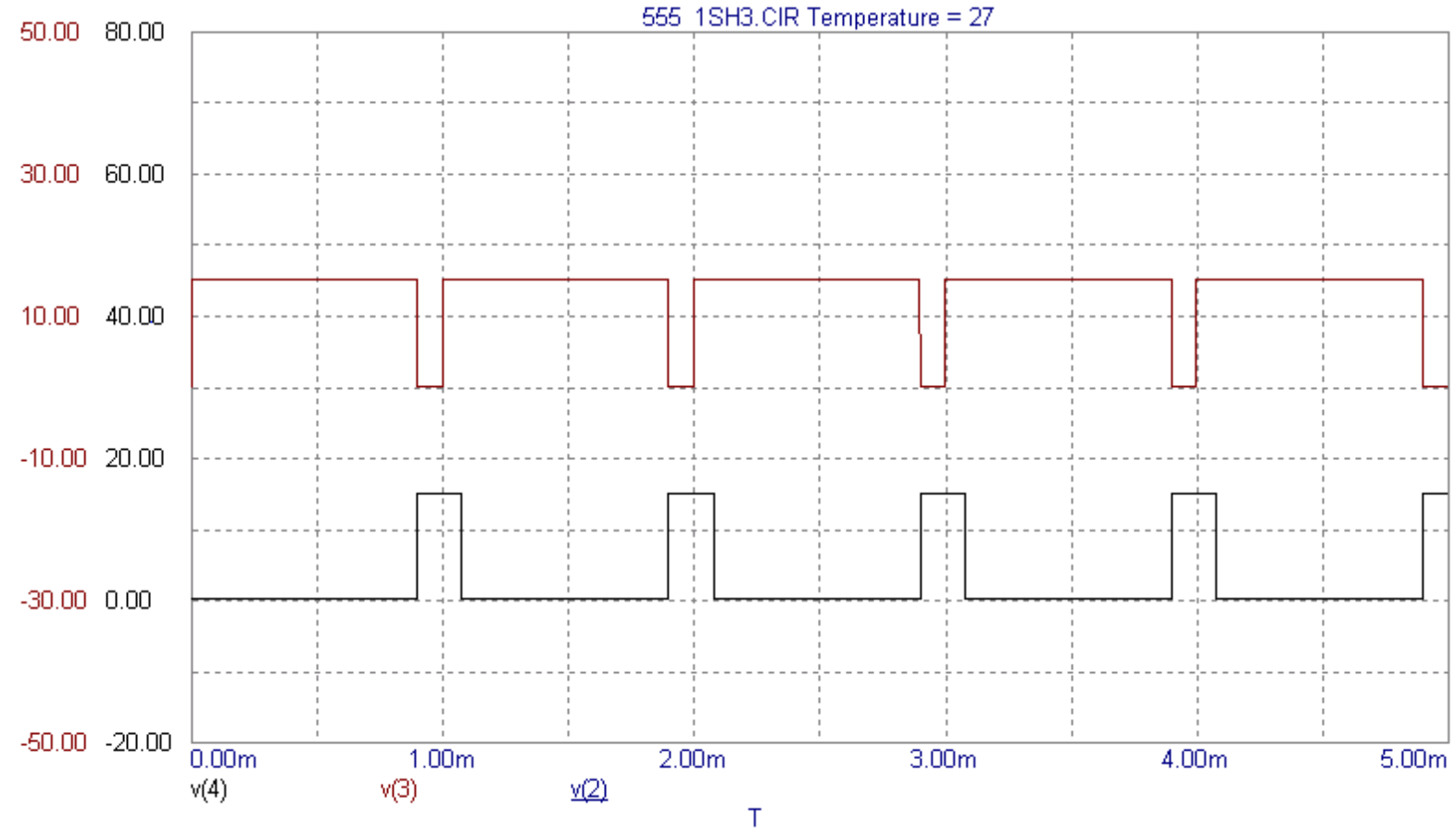

3
V1
15
+
–
R2
76K
VCC
DISCHG
6
TRIG
X2 UA555
THRES
1
V(1)
RAMP
V(4)
OUT
4
OUT
C1
2140P
5
CTRL
RESET
C2
.01U
V(6)
TRIGGER
V2
PULSE
+

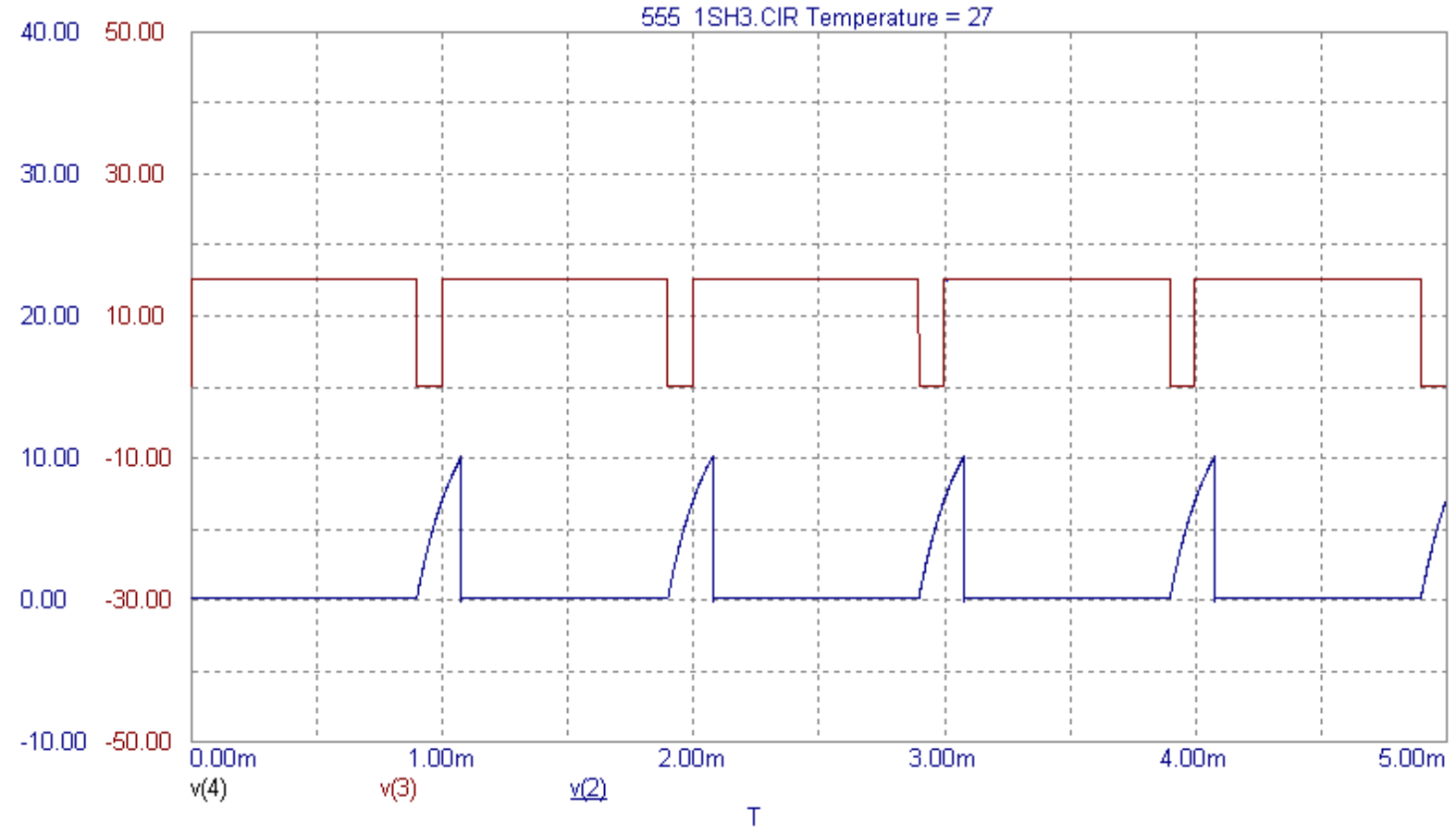


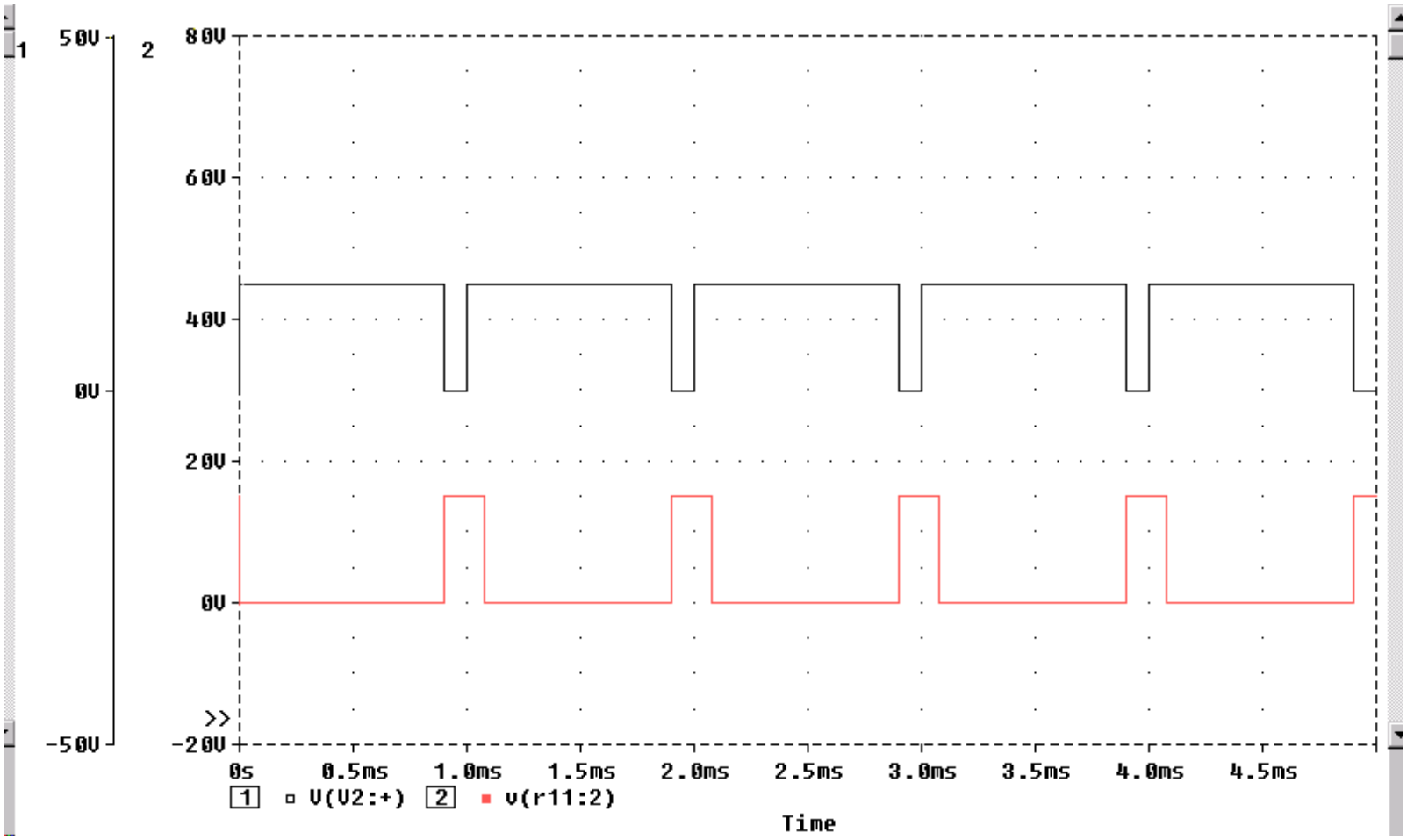

Tek Stop: 200kS/s
18 Acqs
Ch2 +Width
179µs
Low signal
amplitude
Ch1 Freq
1.003kHz
Low signal
amplitude
Ch1 −Width
97.99µs
Low signal
amplitude
1→
2→
Ch1 10 V Ch2 10 V M 250µs Ch1 ⌊ 6.2 V
Ref2 100mV 500µs
22 Jan 1997
08:13:32

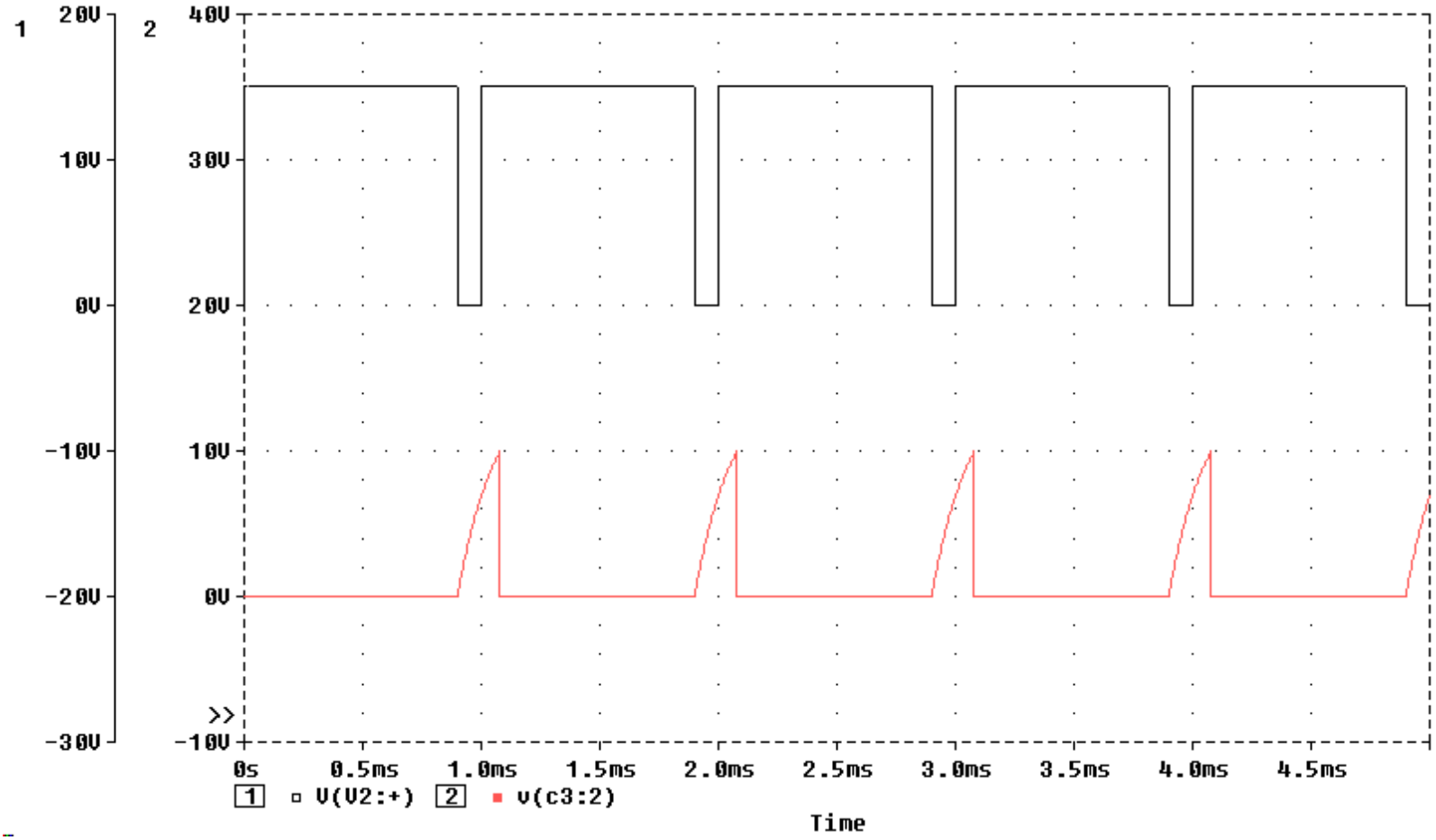

40.00
20.00
0
-20.00
-40.00
Trigger Inputin Volts
70.00
50.00
30.00
10.000
-10.000
Output in Volts
X 2.082M
< 5.001 >
X 1.900M
< 5.000 >
1
2
2.150M
2.650M
3.150M
3.650M
4.150M
Time in Secs
Δx = 181.3U Δy = 1.458M


69.87
49.87
29.87
9.874
-10.13
Capacitor Voltage in Volts
40.00
20.00
0
-20.00
-40.00
Trigger Inputin Volts
2.150M
2.650M
3.150M
3.650M
4.150M
Time in Secs
1
2


555 1SH3.CIR Temperature = 27
50.00
80.00
30.00
60.00
10.00
40.00
-10.00
20.00
-30.00
0.00
-50.00
-20.00
0.00m
1.00m
2.00m
3.00m
4.00m
5.00m
v(4)
v(3)
v(2)
T


555 1SH3.CIR Temperature = 27
40.00
50.00
30.00
30.00
20.00
10.00
10.00
-10.00
0.00
-30.00
-10.00
-50.00
0.00m
1.00m
2.00m
3.00m
4.00m
5.00m
v(4)
v(3)
v(2)
T


1
50V
0V
-50V
2
80V
60V
40V
20V
0V
-20V
>>
0s
0.5ms
1.0ms
1.5ms
2.0ms
2.5ms
3.0ms
3.5ms
4.0ms
4.5ms
1 V(V2:+) 2 v(r11:2)
Time


1
20V
10V
0V
-10V
-20V
-30V
2
40V
30V
20V
10V
0V
>>
-10V
0s
0.5ms
1.0ms
1.5ms
2.0ms
2.5ms
3.0ms
3.5ms
4.0ms
4.5ms
1 V(V2:+) 2 v(c3:2)
Time

#23: Operational Amplifier Adder

The original mission of the Operational Amplifier integrated circuit is to perform operations (just like the name suggests). The Op-amp is versatile enough to perform integrations, differentiations, summing, subtracting, multiplication, and a multitude of other mathematical operations. Although the functions performed by the circuits may be complex, the circuits themselves are usually relatively easy to build and easy to design.

One example of these truisms is the Operational Amplifier Adder circuit, shown in Figure 23-1. The signal at Input A is summed with the signal at Input B. This circuit has a variety of uses in communications circuitry.

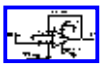


Figure 23-1: Schematic of Op-Amp Adder Circuit

Our equivalent SPICE model of this circuit is shown in Figure 23-2, where the inputs have been replaced by voltage sources.

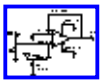


Figure 23-2: SPICE equivalent Schematic of Op-Amp Adder Circuit

The Breadboard was constructed and two sets of waveforms were measured. The first two waveforms are the two input signals. The breadboard results are shown in Figure 23-3, with the top waveform being a $\pm$ 1 volt signal at 1 Khz and the bottom waveform being a 0v to 1 volt pulsed square wave with a 50 % duty cycle at 10 Khz. The breadboard result of the addition of these two waveforms is shown in Figure 23-4.

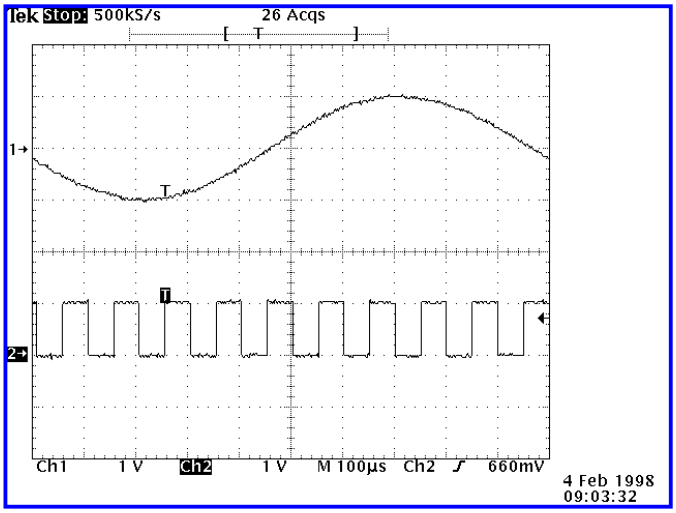


Figure 23-3: Breadboard input signal waveforms

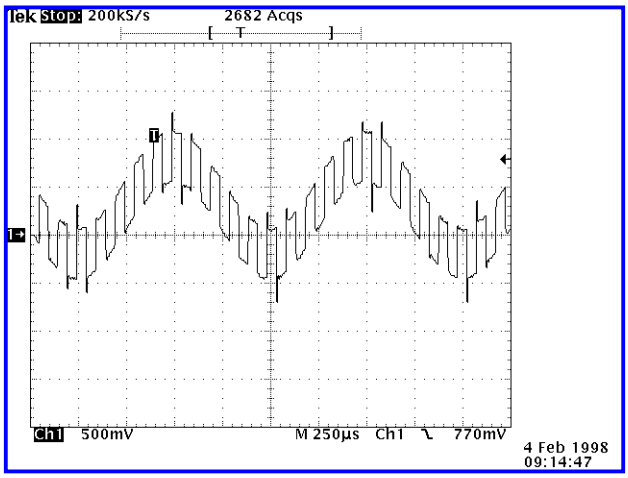


Figure 23-4: Breadboard output signal result

This circuit was also constructed in IsSpice, Pspice, and Microcap. The resulting waveforms are shown in Figures 23-5 through 23-7.

- Spice tip: The IsSpice model used the Intusoft created generic op-amp model. The passed parameters used were VOS=1U IOS=1N IBIAS=1N FT=5MEG DVDT=5MEG GAIN=100K. The Microcap and Pspice simulators used the UA741 model for the Operational amplifier. The breadboard used a LM324. As the results show, high performance is not required from the op-amp to get acceptable results from this circuit.

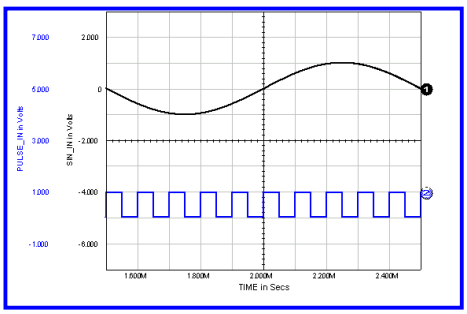


Figure 23-5A: IsSpice input waveforms

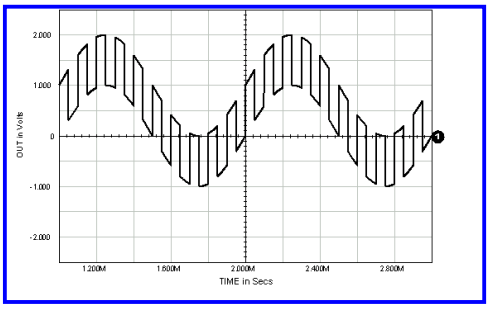


Figure 23-5B: IsSpice output waveform result

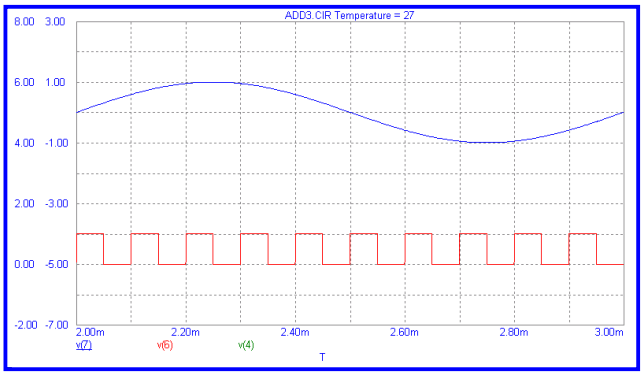


Figure 23-6A: Microcap input waveforms

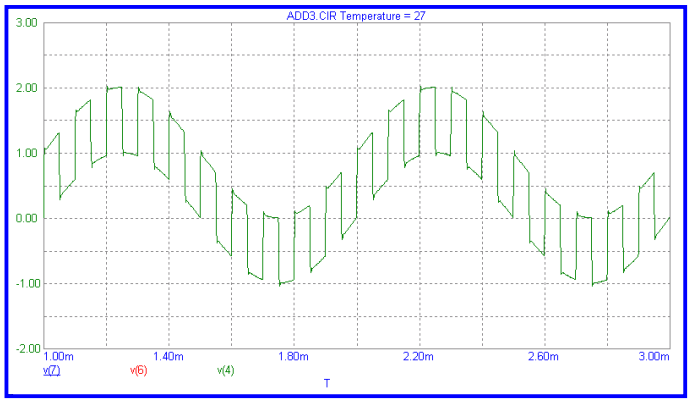


Figure 23-6B: Microcap output results

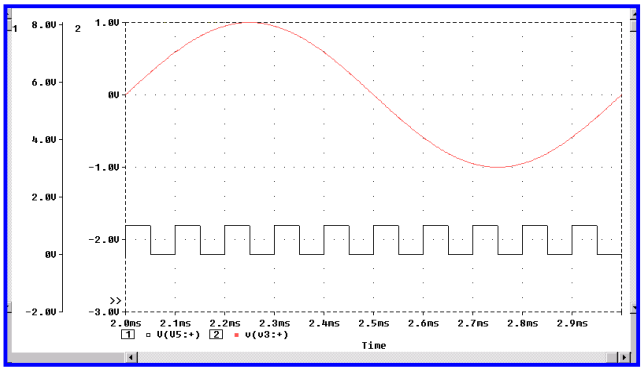


Figure 23-7A: Pspice input waveforms

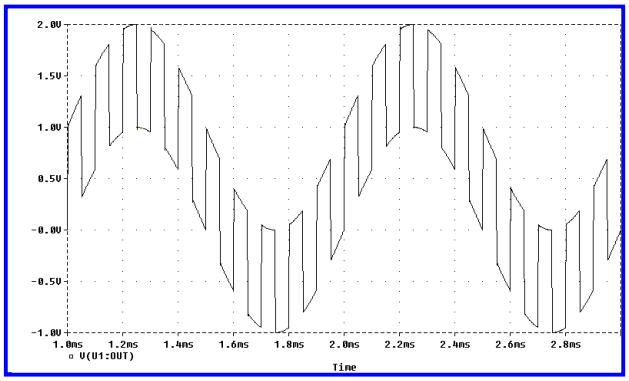


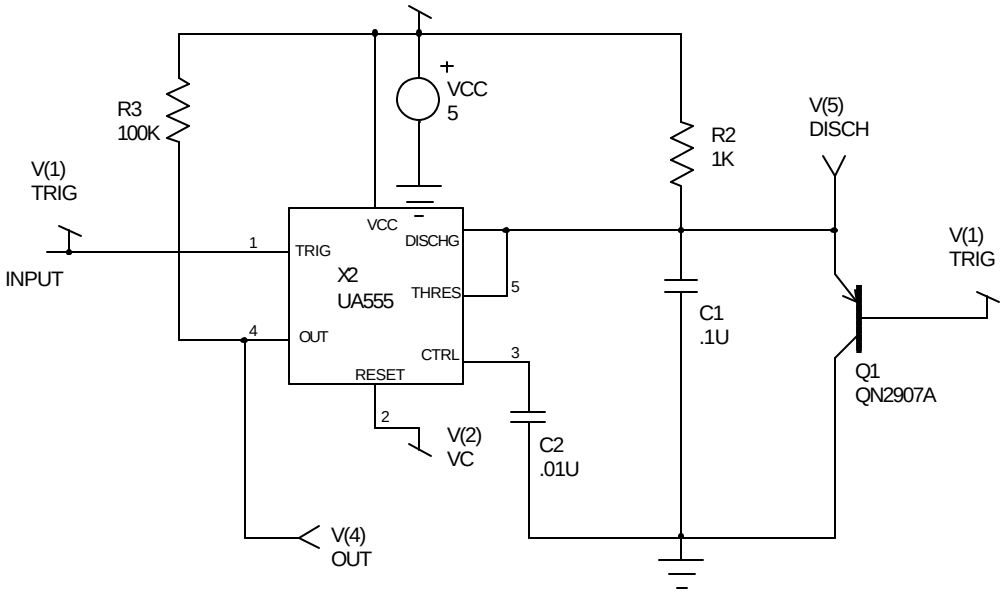
Figure 23-7B: Pspice output result

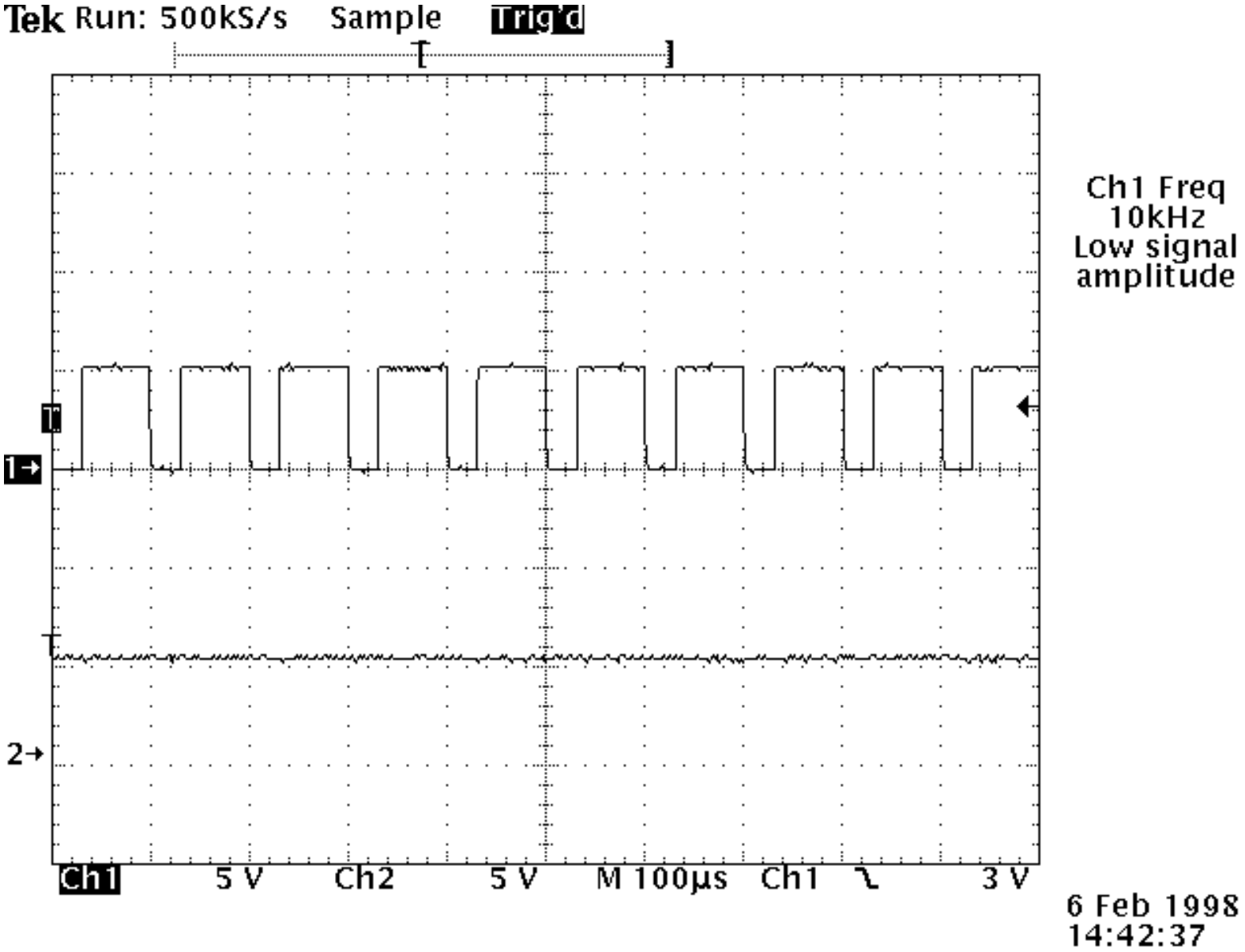
Run Time Summary		
IsSpice v 7.6	PsPice v 6.3	Micro-Cap V v2
4.25 Sec	11.55 Sec	11.456 Sec
Advantages: Low parts count		
Disadvantages:		

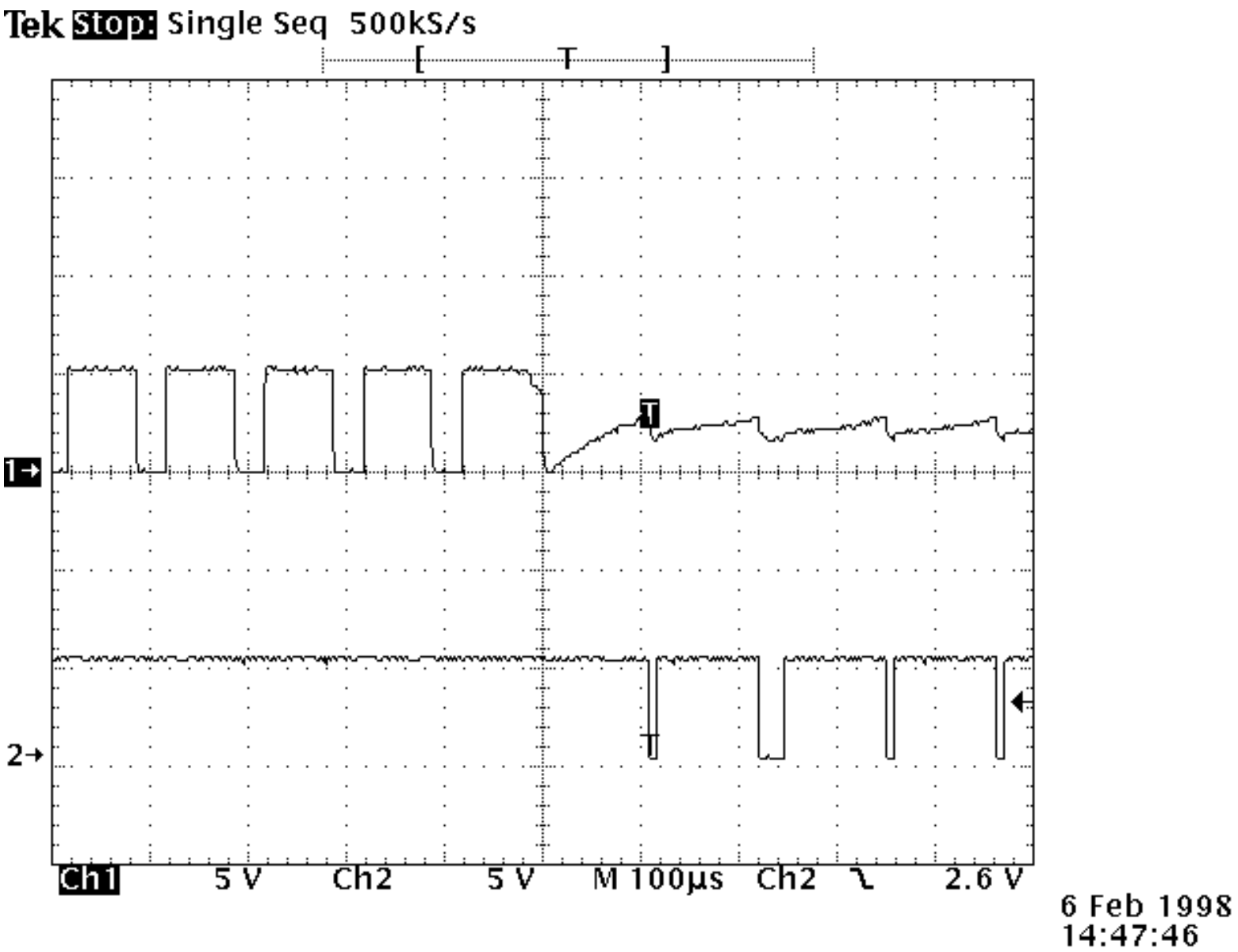
Filenames: summer (IsSpice) add3 (Micro-cap) add2 (Pspice)

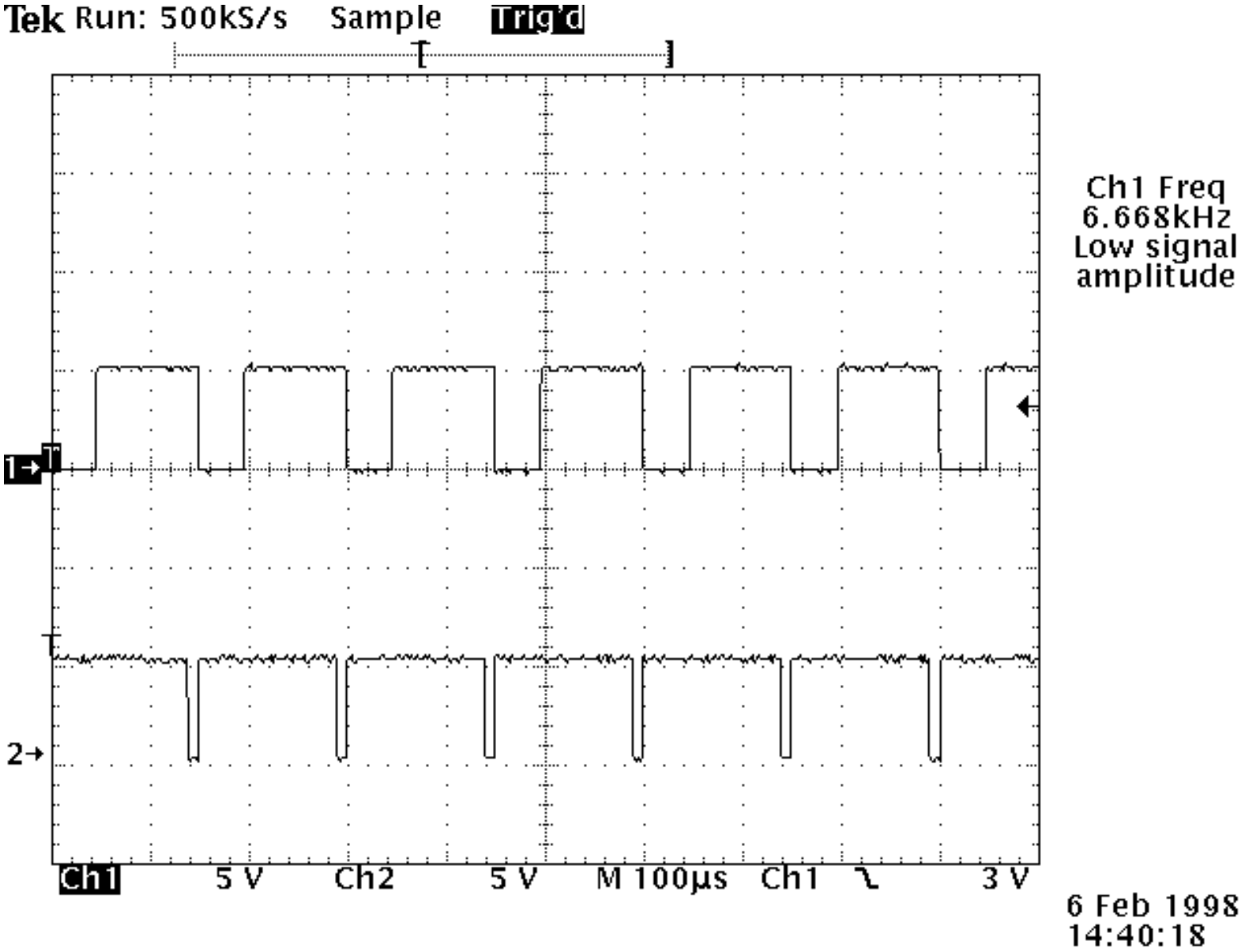
References

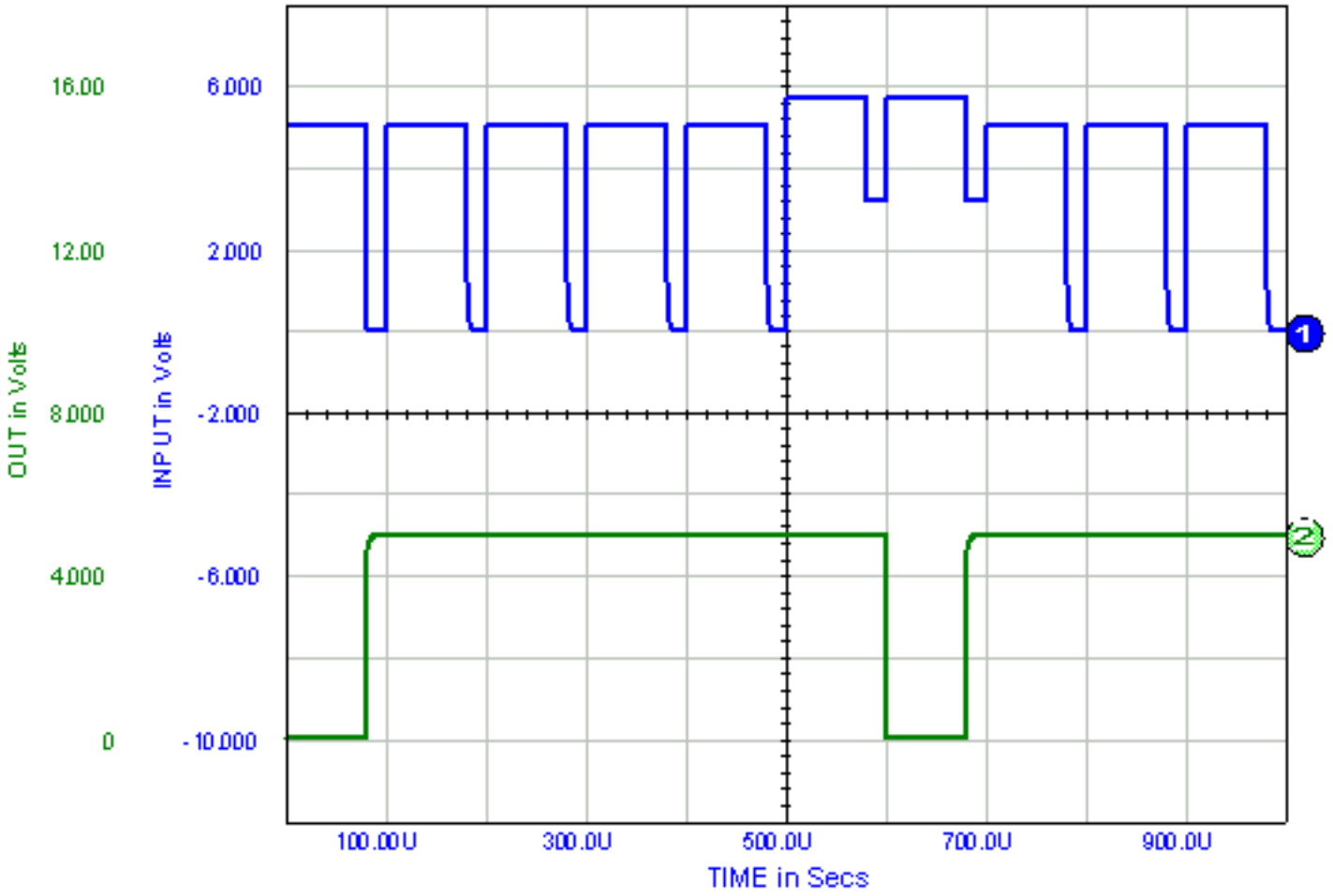
Linear Circuits Data Book Vol 3, Texas Instruments, 1992.

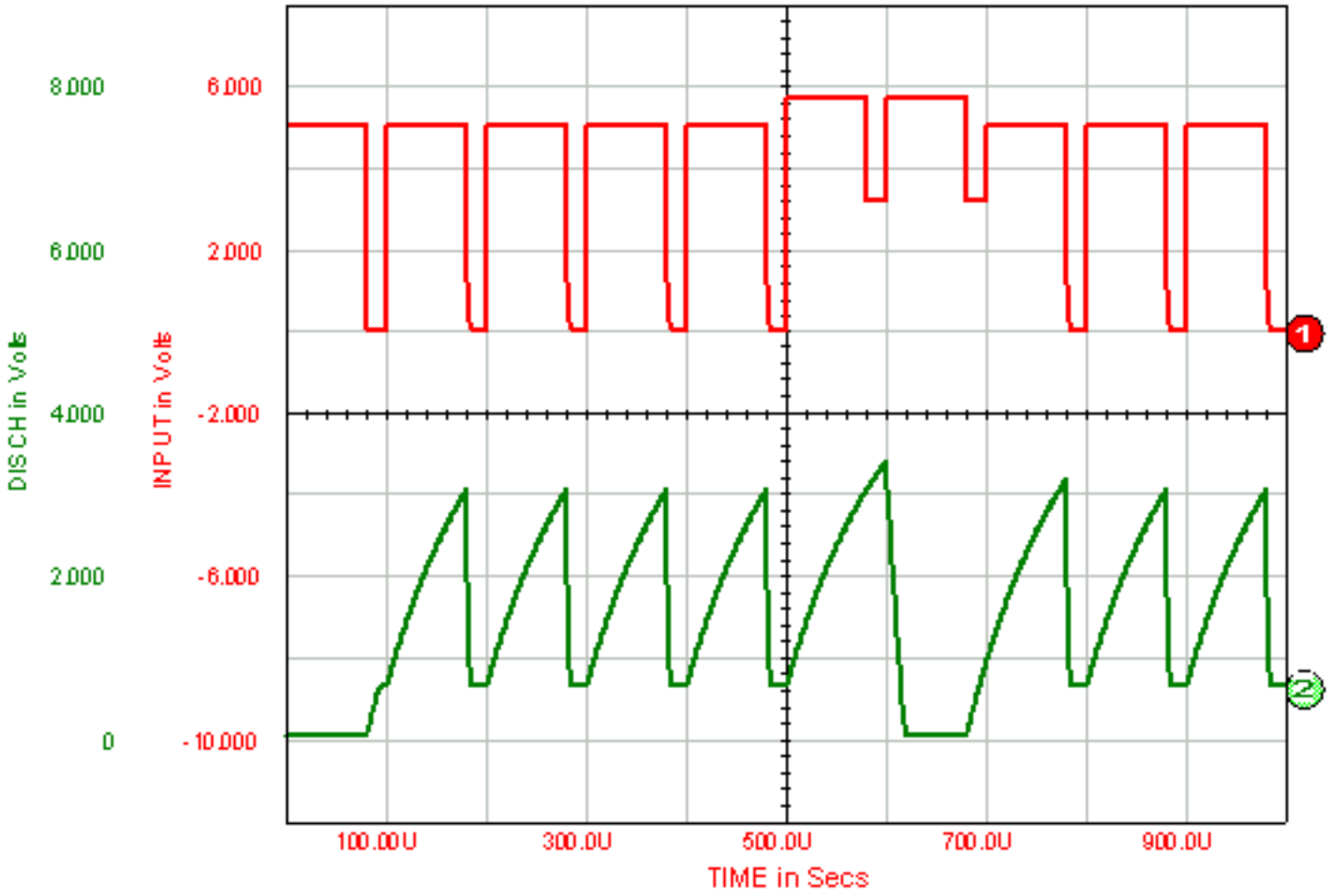

R3
100K
V(1)
TRIG
INPUT
VCC
5
R2
1K
V(5)
DISCH
V(1)
TRIG
VCC
DISCHG
TRIG
X2
UA555
THRES
OUT
CTRL
RESET
1
5
4
3
2
C1
.1U
Q1
QN2907A
V(2)
VC
C2
.01U
V(4)
OUT

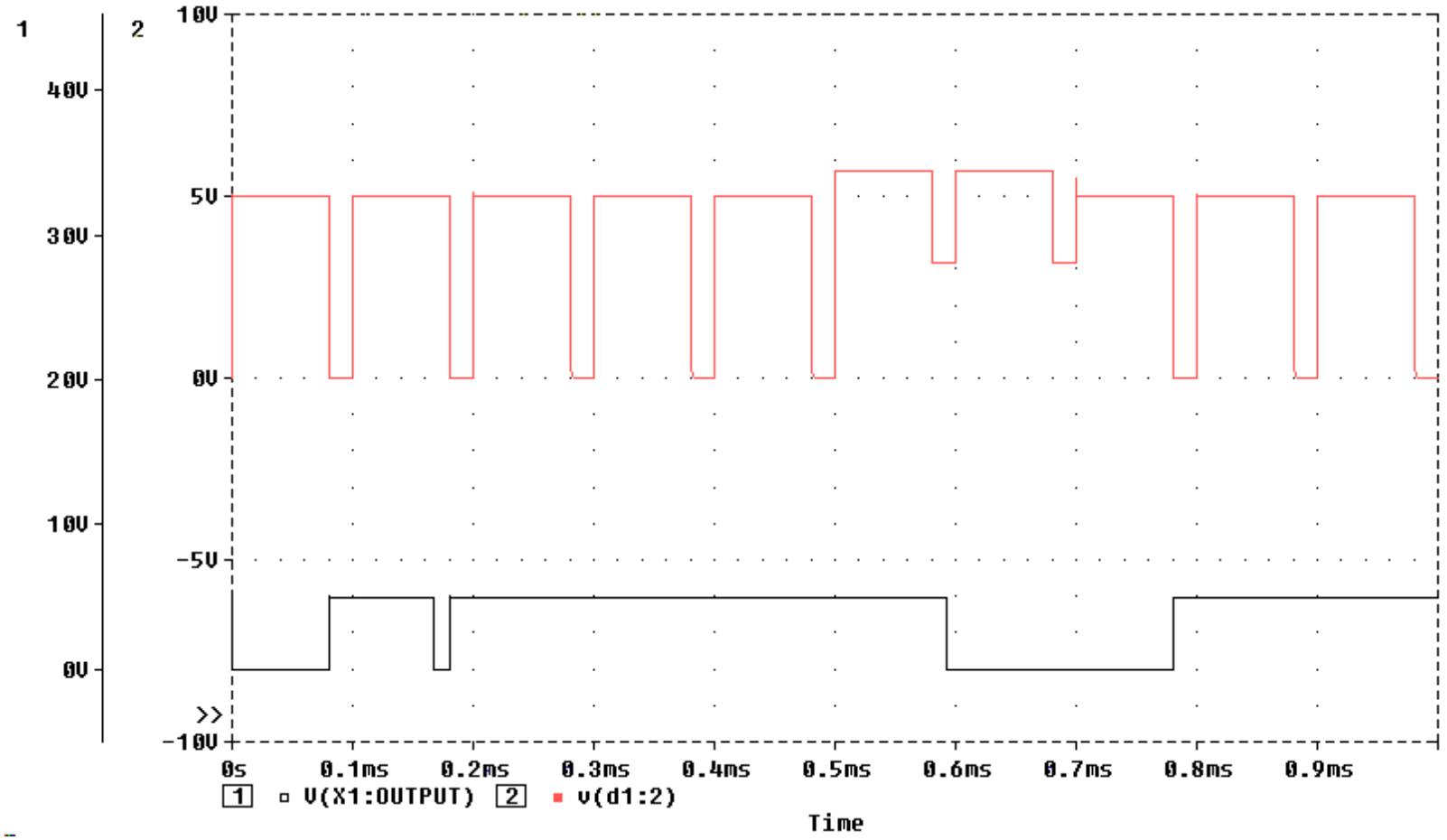

Tek Run: 500kS/s Sample Trig'd
Ch1 Freq
10kHz
Low signal
amplitude
Ch1 5 V Ch2 5 V M 100µs Ch1 3 V
6 Feb 1998
14:42:37

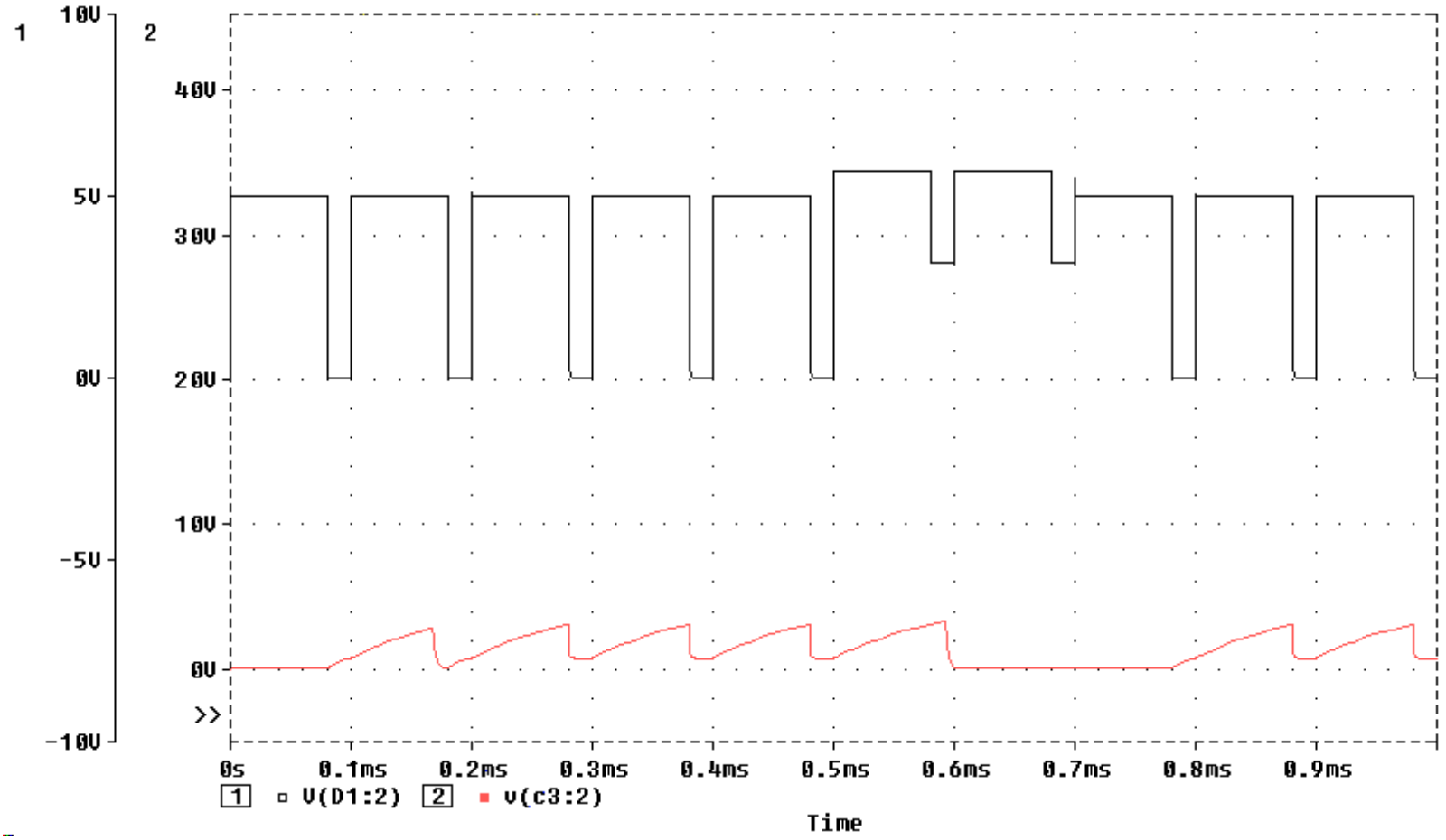

Tek Stop: Single Seq 500kS/s
1→
2→
Ch1 5 V Ch2 5 V M 100µs Ch2 ⌊ 2.6 V
6 Feb 1998
14:47:46

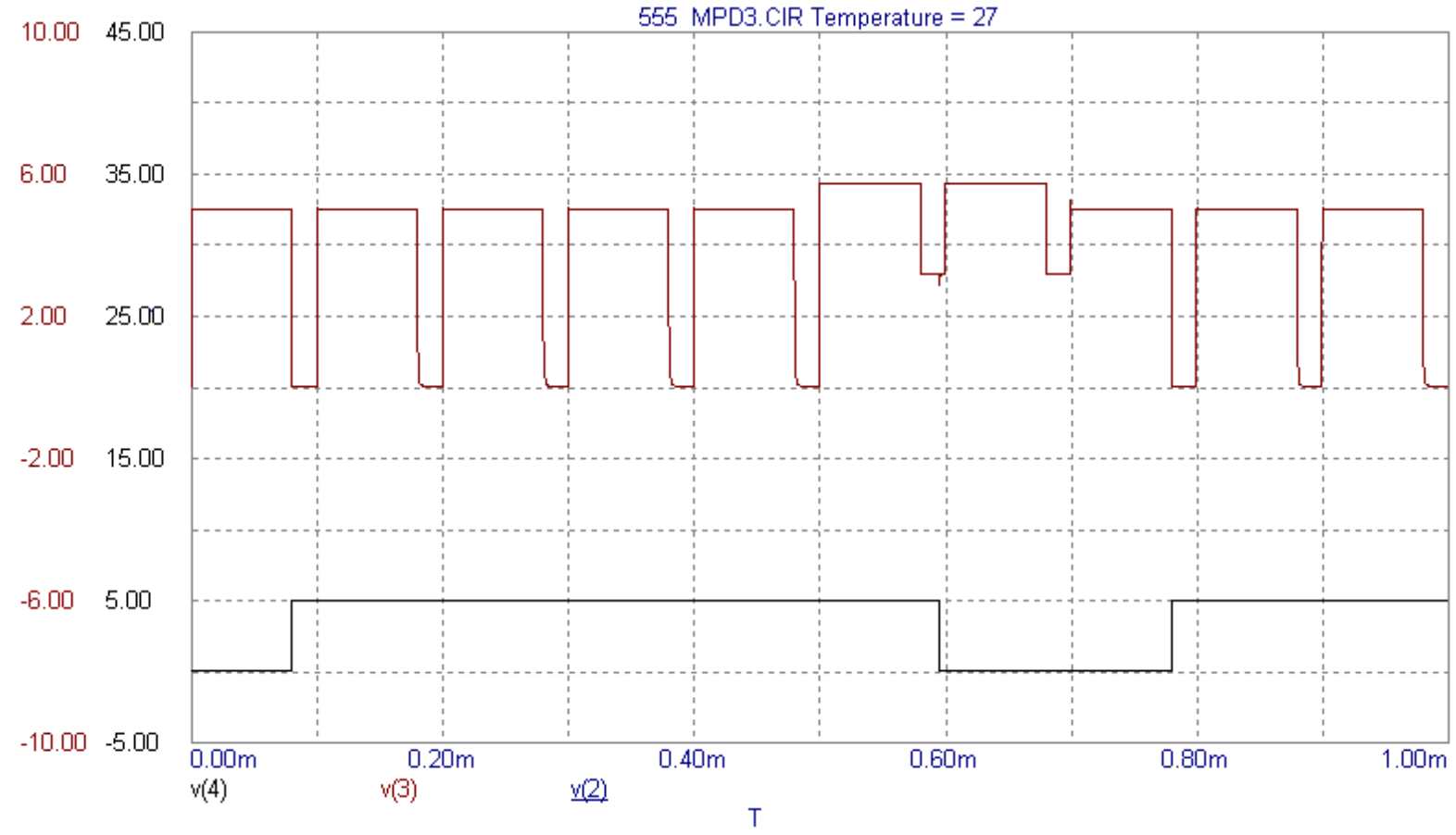

Tek Run: 500kS/s Sample Trig'd
Ch1 Freq
6.668kHz
Low signal
amplitude
1→
2→
Ch1 5 V Ch2 5 V M 100µs Ch1 ∿ 3 V
6 Feb 1998
14:40:18

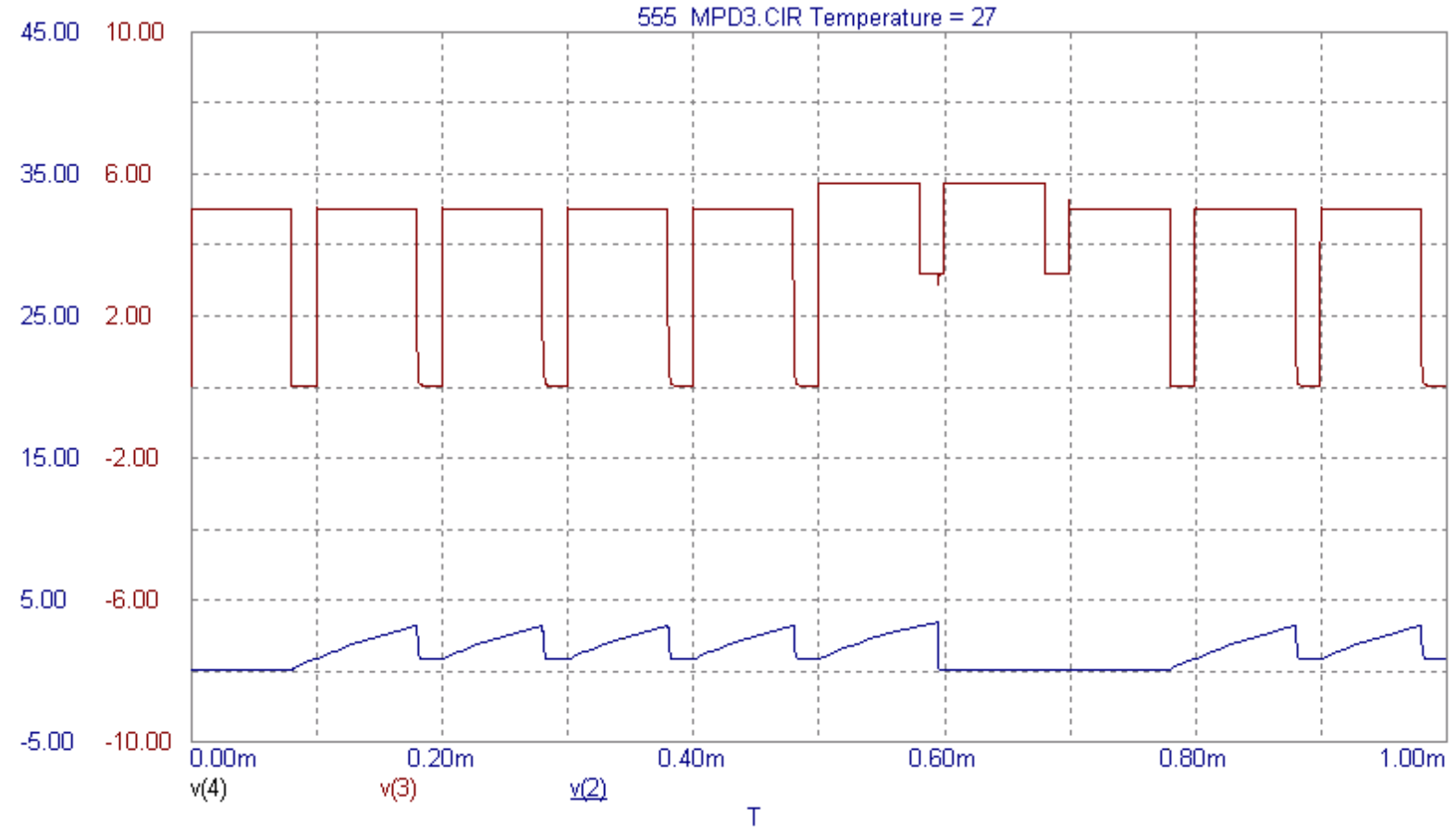

16.00
12.00
8.000
4.000
0
OUT in Volts
6.000
2.000
-2.000
-6.000
-10.000
INPUT in Volts
100.00U
300.0U
500.0U
700.0U
900.0U
TIME in Secs
1
2


8.000
6.000
4.000
2.000
0
DISCH in Volts
6.000
2.000
-2.000
-6.000
-10.000
INPUT in Volts
100.00U
300.0U
500.0U
700.0U
900.0U
TIME in Secs
1
2


1
2
40V
30V
20V
10V
0V
10V
5V
0V
-5V
-10V
>>
0s
0.1ms
0.2ms
0.3ms
0.4ms
0.5ms
0.6ms
0.7ms
0.8ms
0.9ms
1 V(X1:OUTPUT) 2 v(d1:2)
Time


1
2
10V
40V
5V
30V
0V
20V
10V
-5V
0V
>>
-10V
0s
0.1ms
0.2ms
0.3ms
0.4ms
0.5ms
0.6ms
0.7ms
0.8ms
0.9ms
1 V(D1:2) 2 v(c3:2)
Time


555 MPD3.CIR Temperature = 27
10.00
45.00
6.00
35.00
2.00
25.00
-2.00
15.00
-6.00
5.00
-10.00
-5.00
0.00m
0.20m
0.40m
0.60m
0.80m
1.00m
v(4)
v(3)
v(2)
T


555 MPD3.CIR Temperature = 27
45.00
10.00
35.00
6.00
25.00
2.00
15.00
-2.00
5.00
-6.00
-5.00
-10.00
0.00m
0.20m
0.40m
0.60m
0.80m
1.00m
v(4)
v(3)
v(2)
T

#24: Class AB Amplifier

A Class AB amplifier is defined as using a power stage that has output current flow for more then half, but less than all, of the input cycle [Gilbilisco: 1994]. .

One example of a Class AB amplifier circuit is shown in Figure 24-1. The voltage source VIN provides the input signal. Resistors R1 and R2 set the gain and bandwidth of the amplifier. Output transistors Q5 and Q6 provide sourcing and sinking current for the signal. Diodes D1 and D2 attempt to minimize the distortion created when the input signal passes through the region between where the NPN transistor (Q5) turns off and the PNP transistor (Q7) turns on (and vice versa). Resistors R9 and R10 limit the current draw from Q5 and Q7. R7 and R8 set the Quiescent current of Q5 and Q7. The load is modeled using a resistor (R_LOAD). The net result of this circuitry is a power boosted inverse output representation of the input signal, capable of driving low impedance loads.

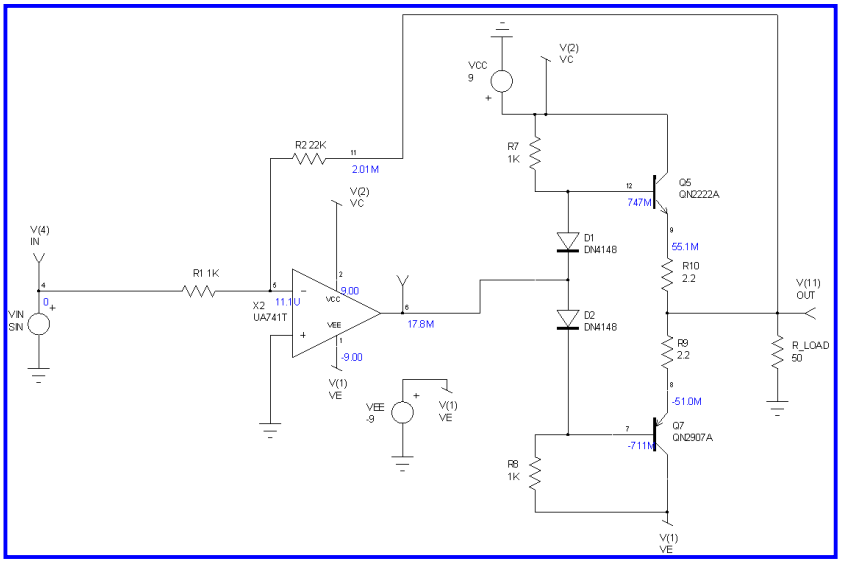


Figure 24-1: Schematic of the Class AB amplifier circuit

Three different measurements were made in order to characterize the performance of this amplifier circuit and show the correlation of the breadboard results to the SPICE models. The three inputs and their resulting measurements are described in detail in Table 24-1.

VIN SIN 0 10M 1K	Input is a 1 Khz sine wave with pk-pk amplitude of 200 mV.
VIN PULSE -100M 100M 0 100N 100N 50U 100U	Square wave of 10 Khz at a 50 % duty cycle used to measure transient loop response
VIN AC 1	AC simulation input to determine filter response

Table 24-1: Characteristic Measurements made on Class AB amplifier circuit

A 1 Khz sine wave was provided at the input and the output result was measured. The breadboard results are shown in Figure 24-2. The top trace is the output waveform. The bottom trace is the input waveform. The IsSpice, Pspice, and Microcap results are shown in Figures 24-3, 24-4, and 24-5 respectively.

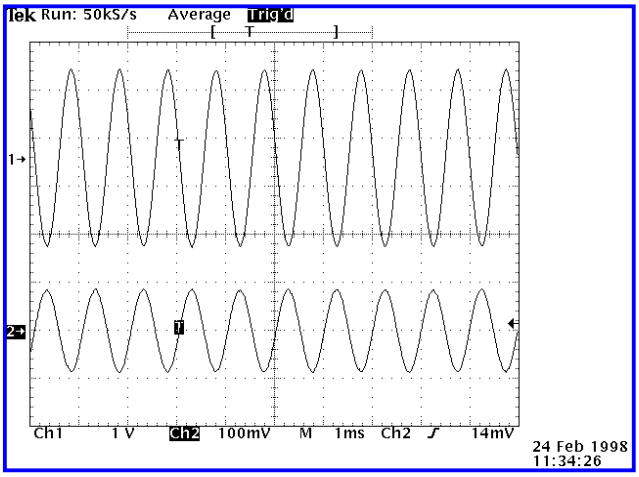


Figure 24-2: Breadboard results of Sine wave input

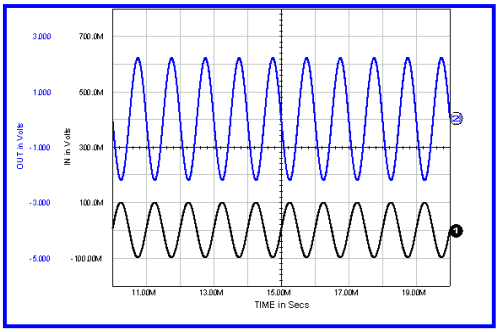


Figure 24-3: IsSpice results of Sine wave input

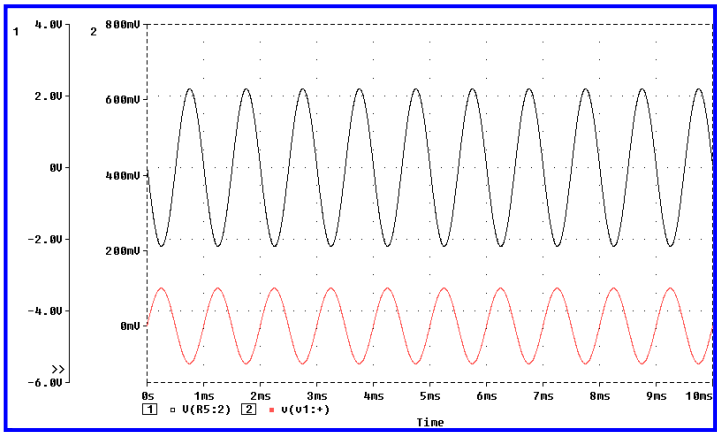


Figure 24-4: Pspice result of Sine wave input

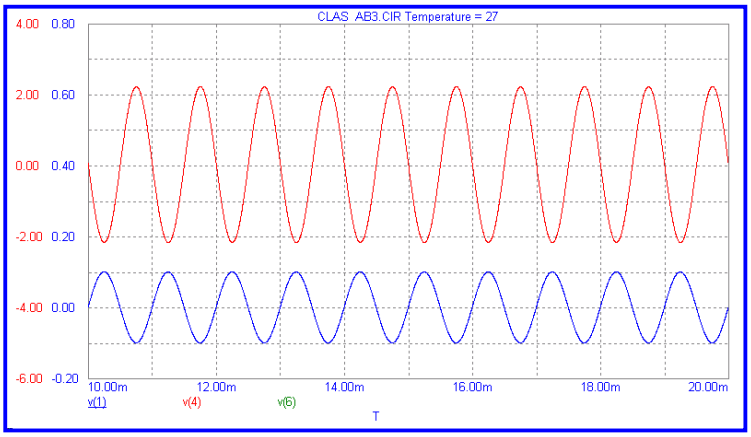


Figure 24-5: Microcap result of Sine wave input

The transient response of the amplifier was measured by using a 10 Khz square wave input with a 50 % duty cycle. The breadboard results are shown in Figure 24-6. The bottom trace is the input square wave, while the top trace is the output result. The Microcap, Pspice, and IsSpice results are shown in Figures 24-7 through 24-9.

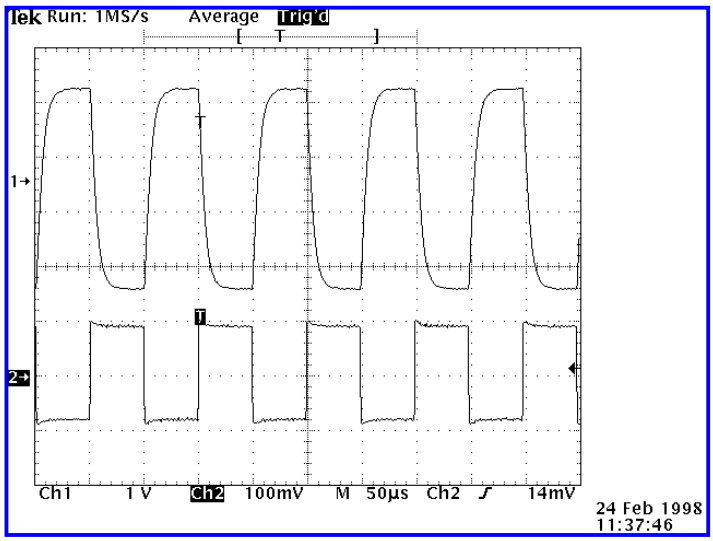


Figure 24-6: breadboard result of square wave input

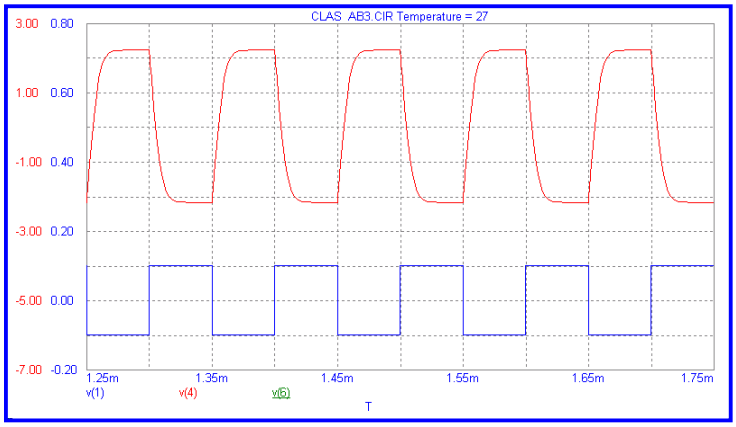


Figure 24-7: Microcap results of square wave input

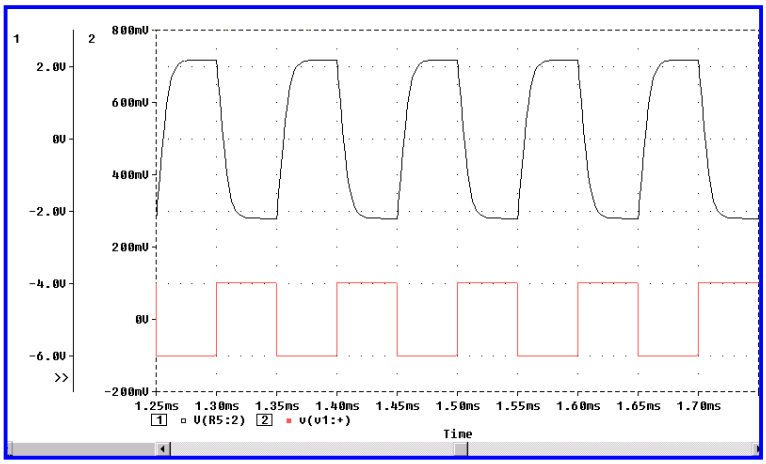


Figure 24-8: Pspice results of square wave input

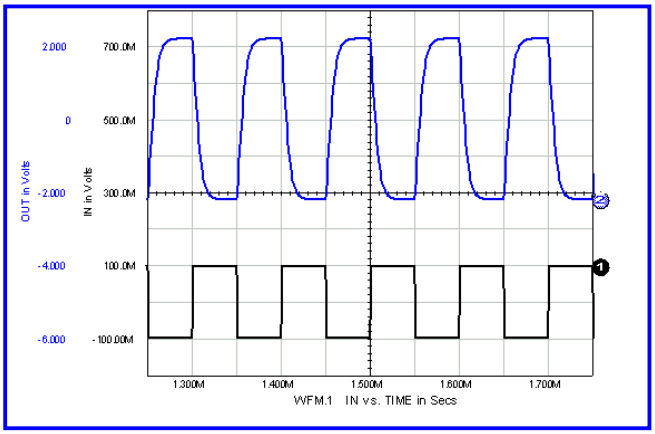


Figure 24-9: IsSpice results of square wave input

In order to measure the frequency response of the Class AB amplifier, the input voltage source was changed to a AC source. The breadboard results are shown in Figure 24-10. The IsSpice, Pspice, and Microcap results are shown in Figure 24-11 through 24-24.

Click Here to see the larger Image

Figure 24-10: Breadboard frequency response results

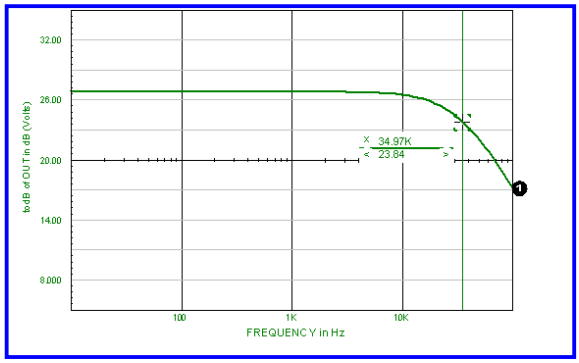


Figure 24-11: IsSpice frequency response results

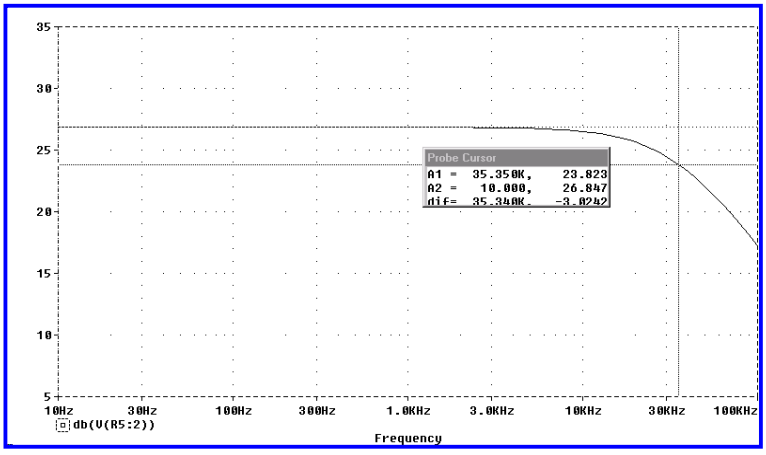


Figure 24-12: Pspice frequency response results

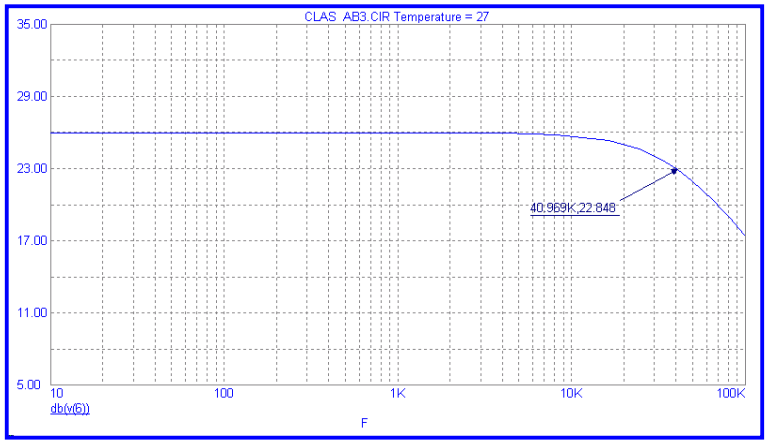


Figure 24-24: Microcap frequency response results

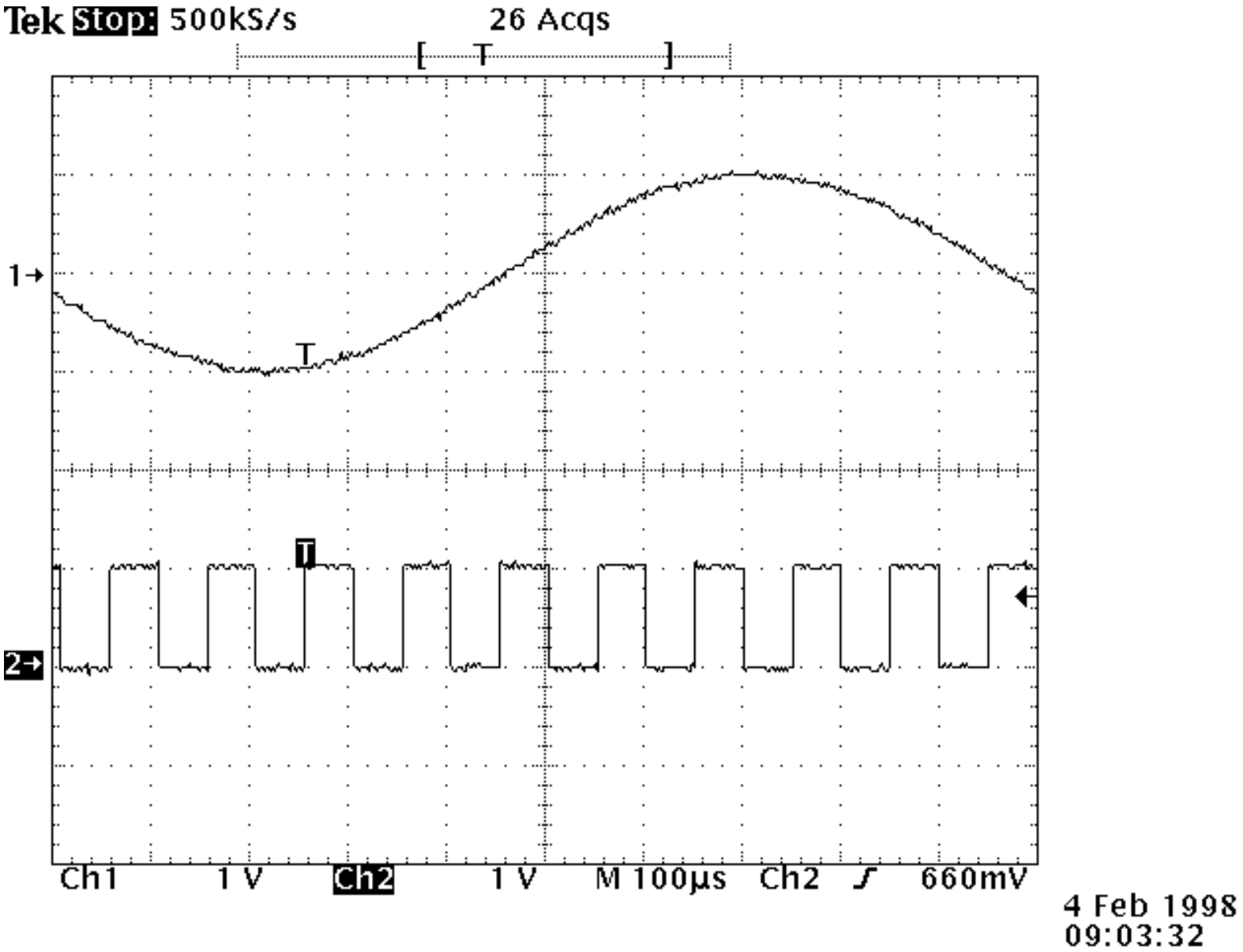
Run Time Summary		
IsSpice v 7.6	Pspice v 6.3	Micro-Cap V v2
26.33 Sec	32.59 Sec	48.576 Sec
Advantages: Improved efficiency over Class A type amplifiers, excellent drive capability		
Disadvantages: output not an exact linear reproduction of the input waveform, continuous current drain, efficiency not as good as other amplifier types.		

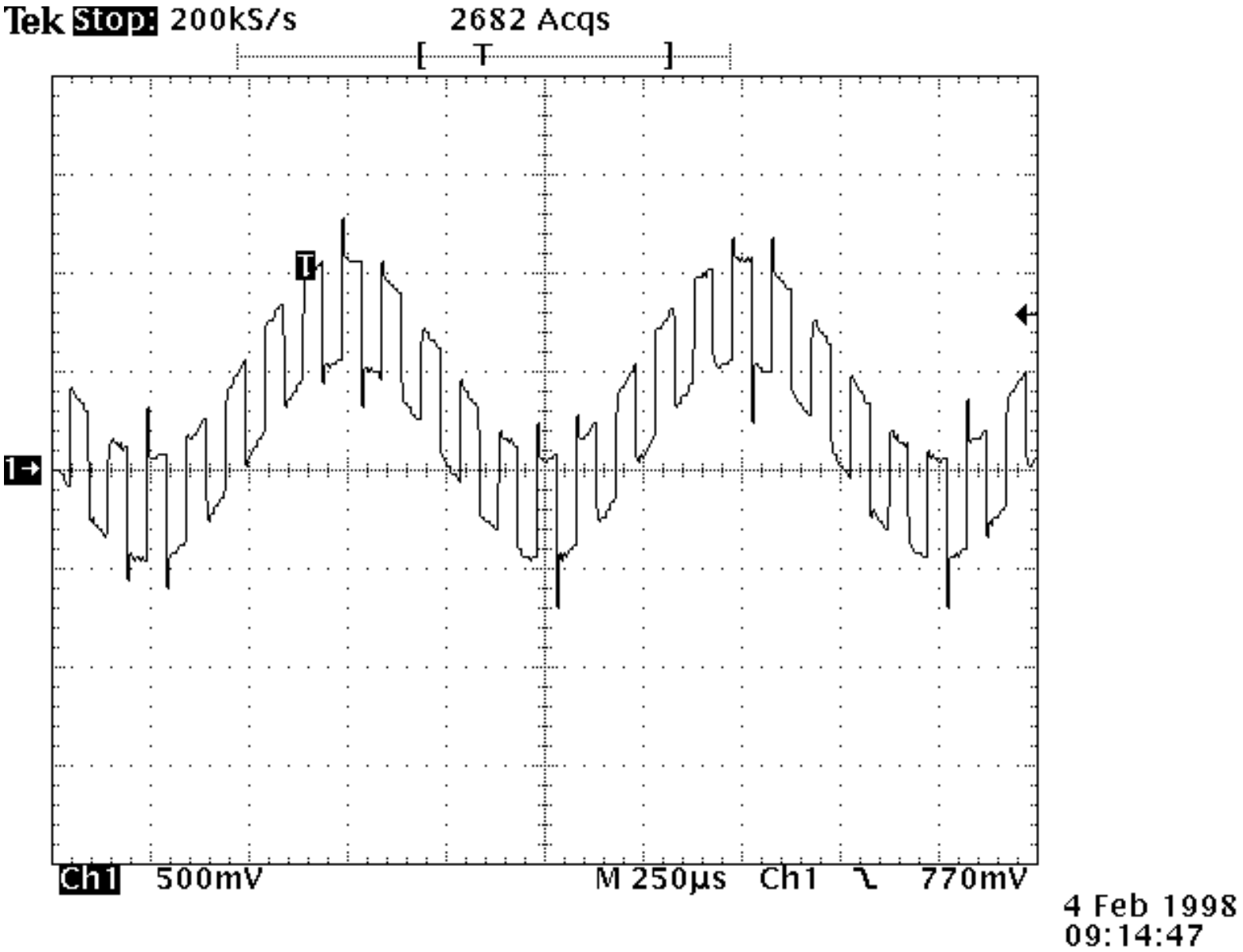
Filenames: Class_AB (IsSpice) Clas_AB3 (Microcap) Clas_AB2 (Pspice)

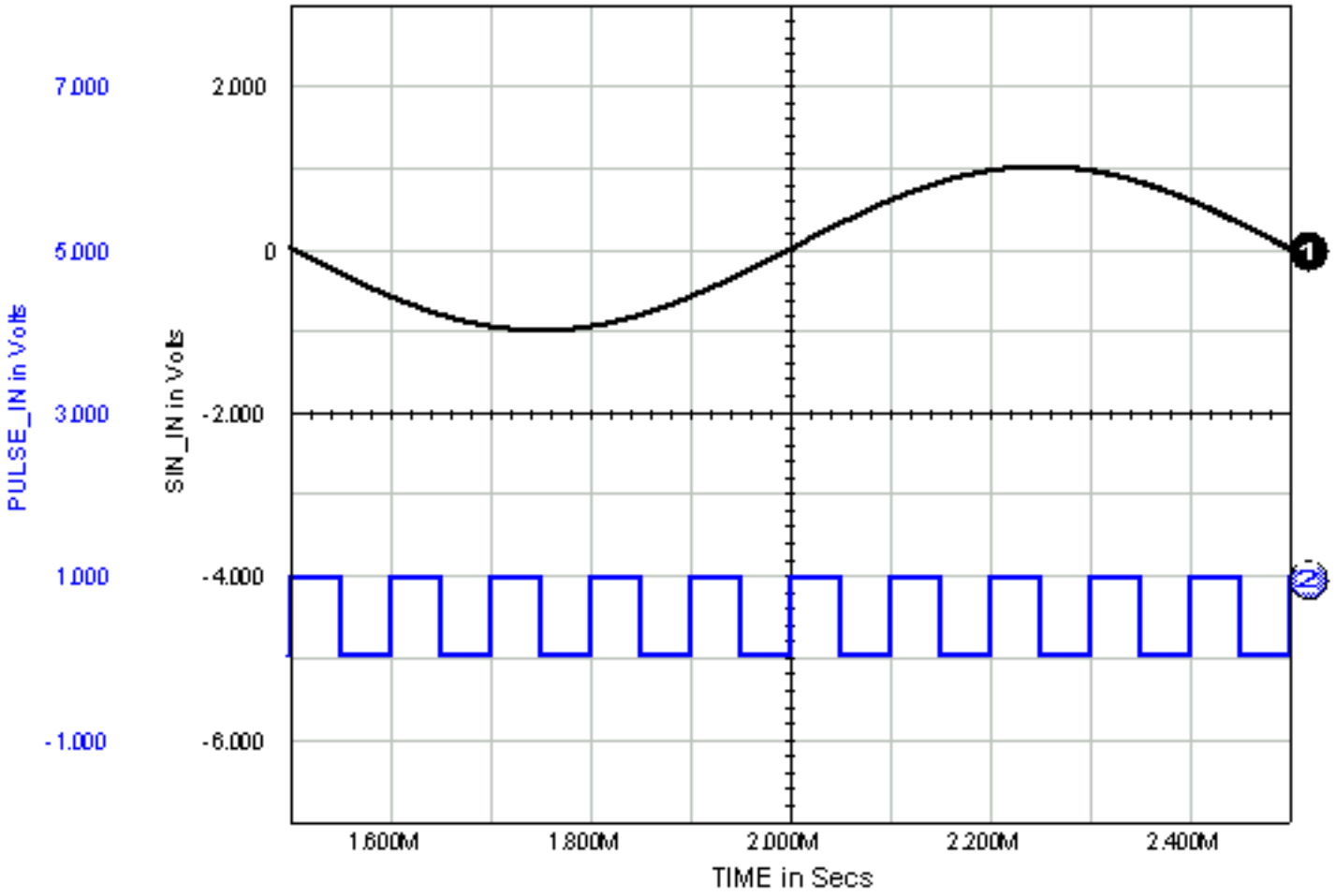
REFERENCES

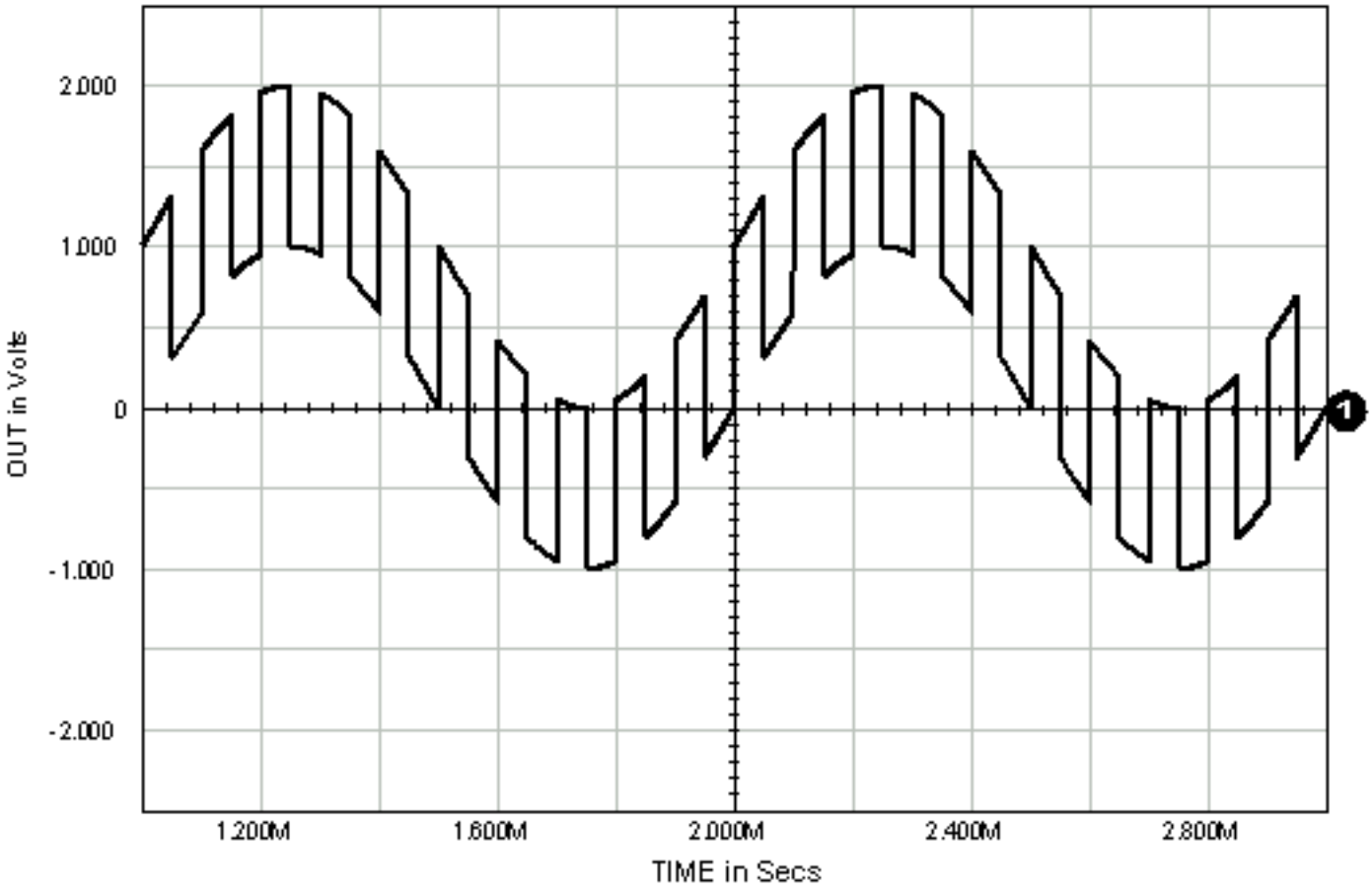
Gilbilisco, Stan, Ed. Encyclopedia of Electronics. TAB Books. PA: 1985

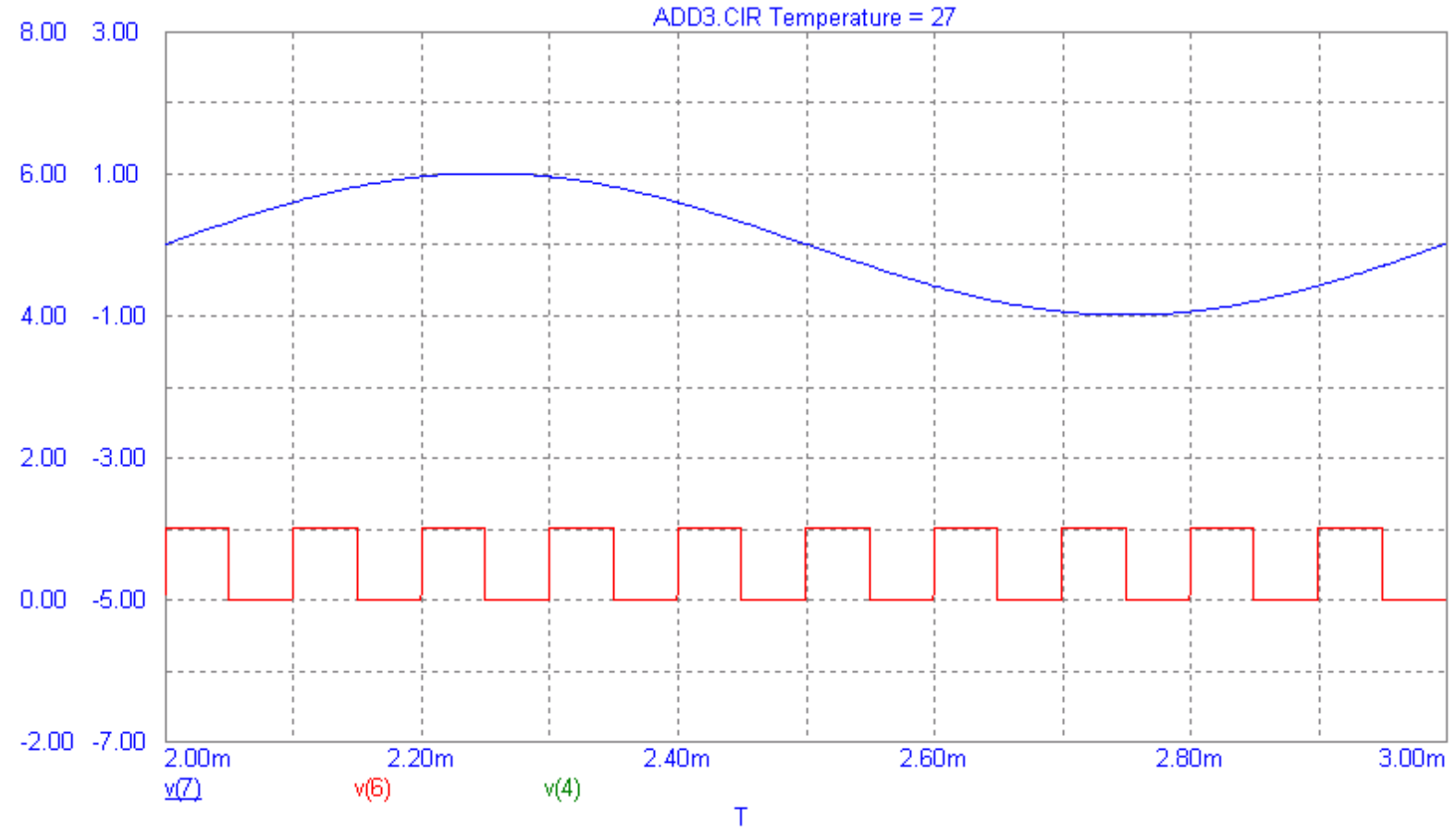
Gilbilisco, Stan, Ed. Amateur Radio Encyclopedia. TAB Books. PA: 1994

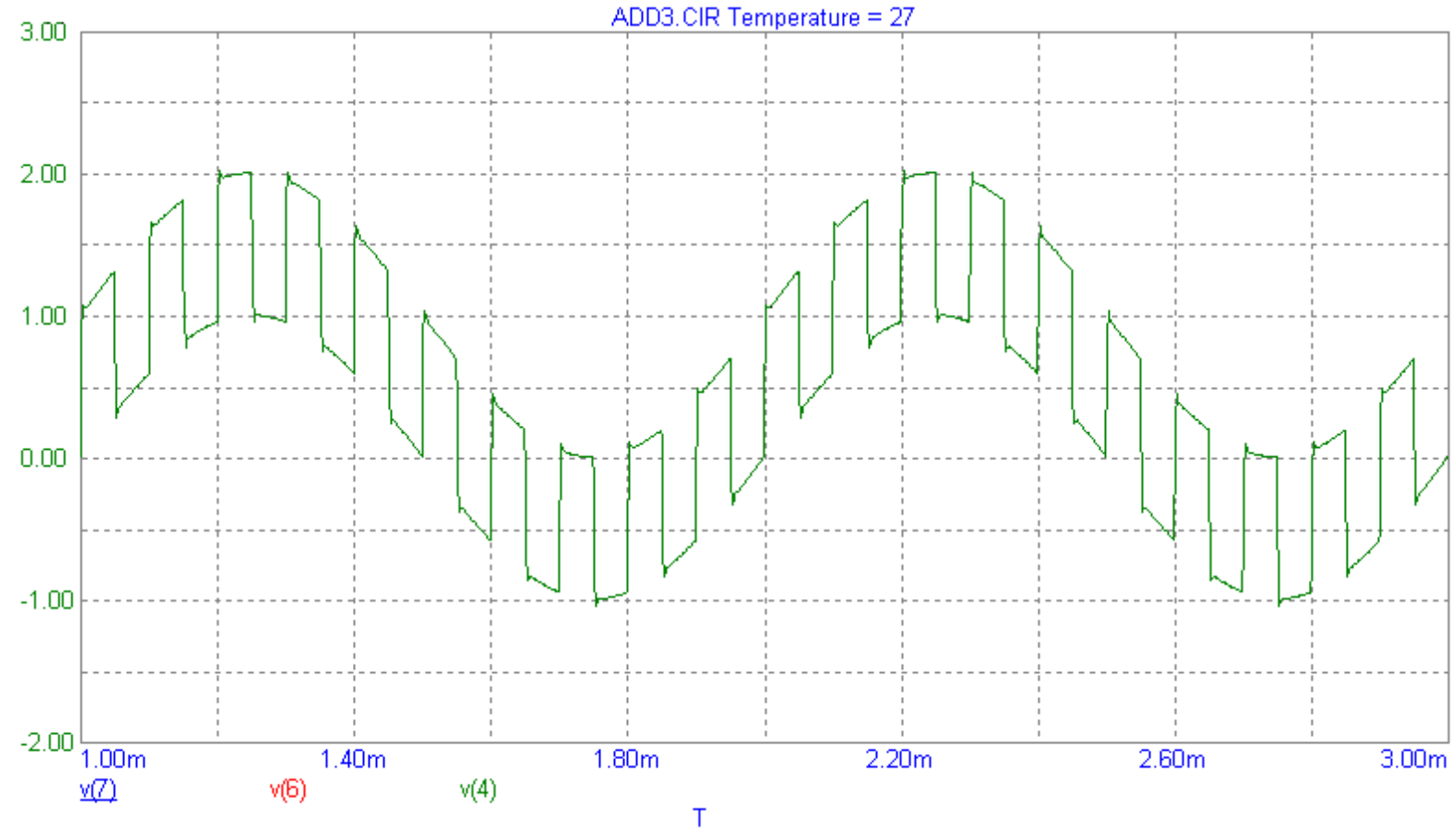

Tek Stop: 500kS/s
26 Acqs
1→
2→
Ch1 1 V
Ch2 1 V
M 100µs Ch2 ƒ 660mV
4 Feb 1998
09:03:32

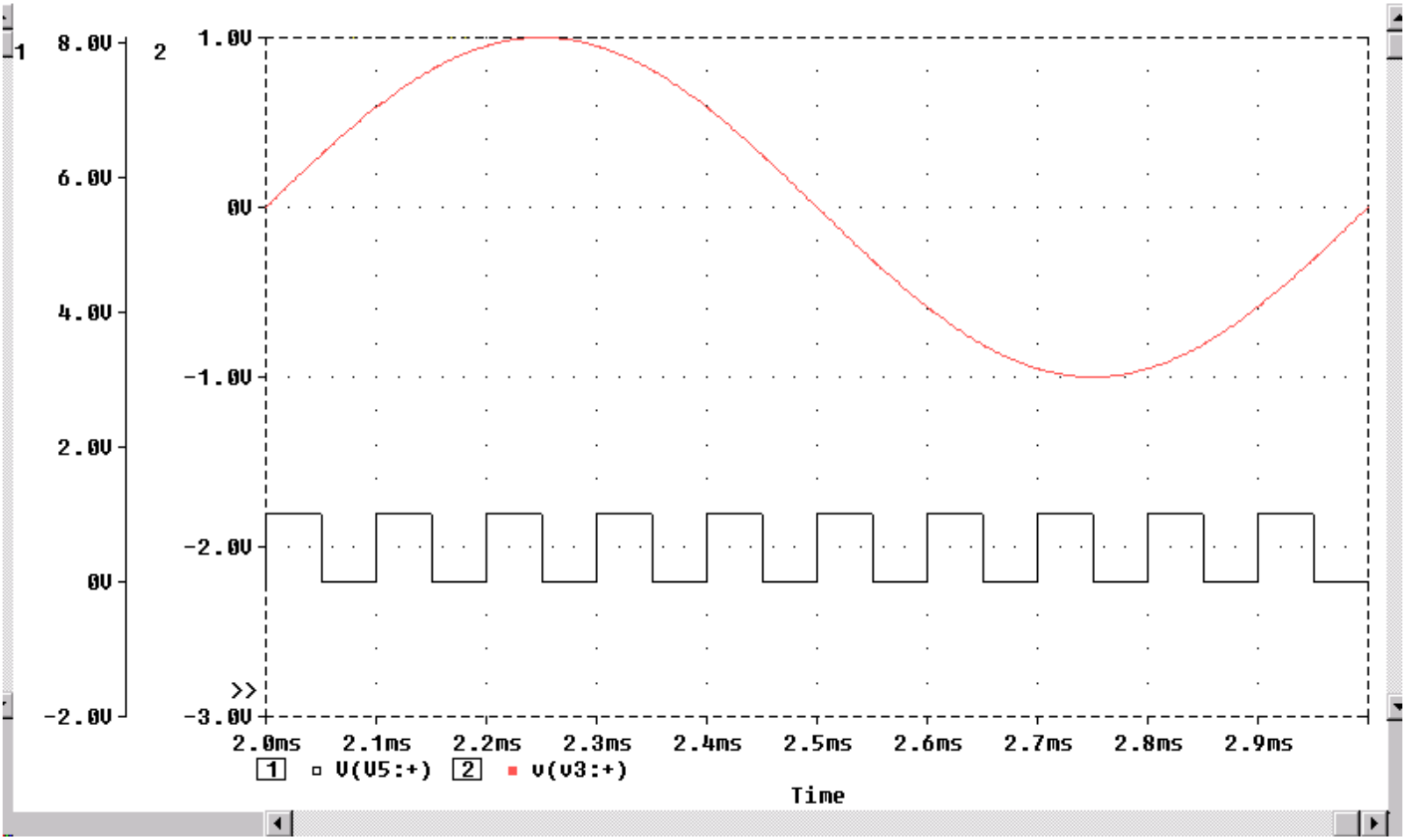

Tek Stop: 200kS/s
2682 Acqs
Ch1 500mV
M 250µs Ch1 ∖ 770mV
4 Feb 1998
09:14:47

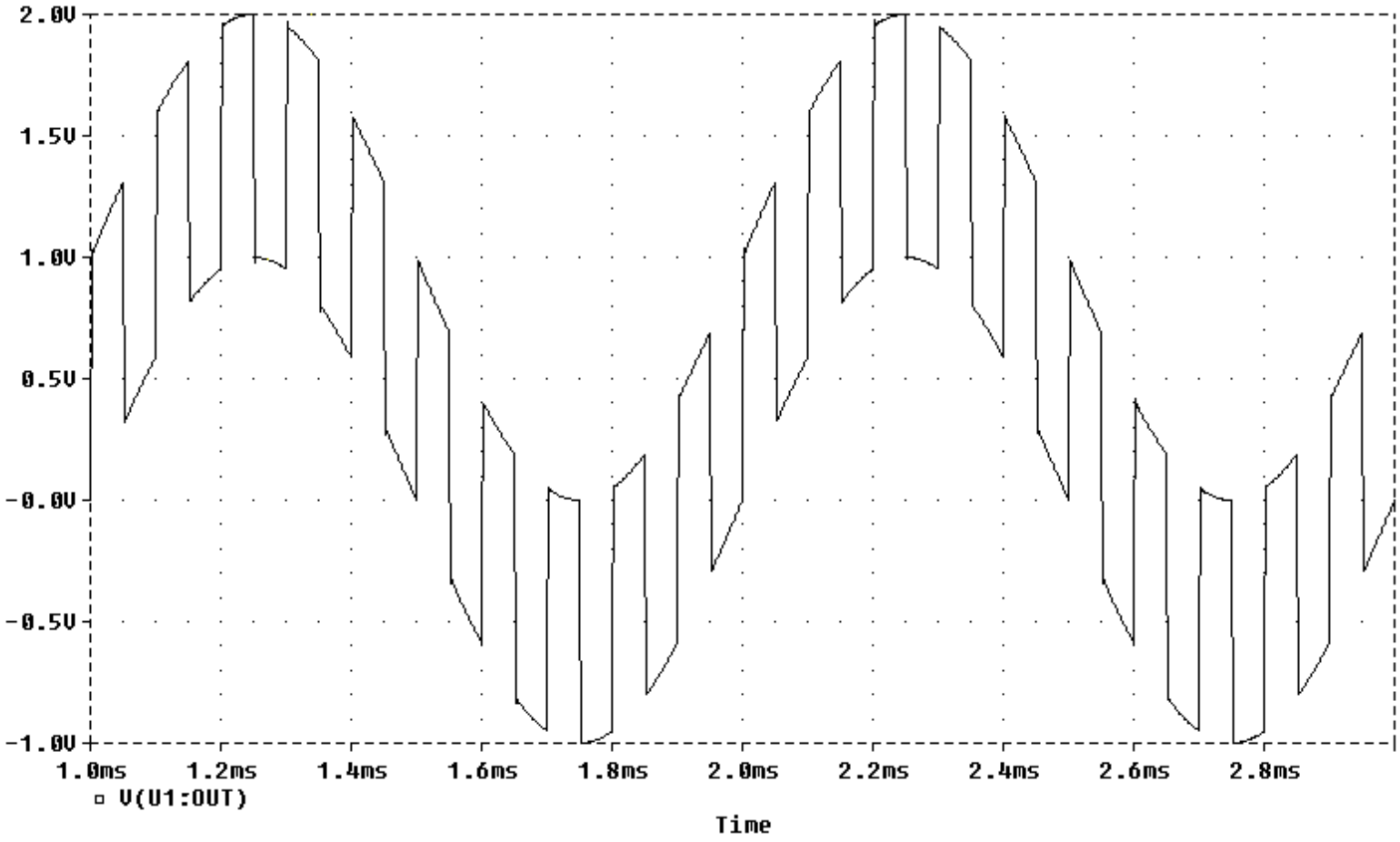

7.000
5.000
3.000
1.000
-1.000
PULSE_IN in Volts
2.000
0
-2.000
-4.000
-6.000
SIN_IN in Volts
1.600M
1.800M
2.000M
2.200M
2.400M
TIME in Secs
1
2


2.000
1.000
0
-1.000
-2.000
OUT in Volts
1.200M
1.600M
2.000M
2.400M
2.800M
TIME in Secs
1


ADD3.CIR Temperature = 27
8.00
3.00
6.00
1.00
4.00
-1.00
2.00
-3.00
0.00
-5.00
-2.00
-7.00
2.00m
2.20m
2.40m
2.60m
2.80m
3.00m
v(7)
v(6)
v(4)
T


ADD3.CIR Temperature = 27
3.00
2.00
1.00
0.00
-1.00
-2.00
1.00m
1.40m
1.80m
2.20m
2.60m
3.00m
v(7)
v(6)
v(4)
T


1
8.0V
6.0V
4.0V
2.0V
0V
-2.0V
2
1.0V
0V
-1.0V
-2.0V
>>
-3.0V
2.0ms
2.1ms
2.2ms
2.3ms
2.4ms
2.5ms
2.6ms
2.7ms
2.8ms
2.9ms
1 V(U5:+) 2 v(v3:+)
Time


2.0V
1.5V
1.0V
0.5V
-0.0V
-0.5V
-1.0V
1.0ms
1.2ms
1.4ms
1.6ms
1.8ms
2.0ms
2.2ms
2.4ms
2.6ms
2.8ms
V(U1:OUT)
Time

#25: Window Detector

Another application of the versatile comparator IC is the window detector. The window detector monitors an important signal (usually DC) and changes state if the level does not stay within the voltage range set by the window comparator.

The schematic for the window detector circuit is shown in Figure 25-1. The input signal is modeled by the independent voltage source V_IN. The power to the LM111 components in the circuit are powered by 10 volts DC. The emitter outputs of the comparators are tied to VEE, which are tied to ground. The 10 volt power is dropped to a 5.1 volt level through resistor R1 (which sets the current through the zener at the test current of the device) and zener diode D1 (1N4733). This 5.1 volt signal is fed into the non-inverting terminal of the upper comparator through a 10 K sense resistor (R8). This signal is also scaled down to 4.8 volts by a resistor divider consisting of R3 and R4. The 4.8 volt signal is fed into the inverting terminal of the lower comparator. Therefore, our upper and lower references are 5.1 volts and 4.8 volts. The open collector outputs of the comparators are connected to 5.1 volts through the pull up resistor R2. A table of the possible operating states of this circuit is presented in Table 25-1.

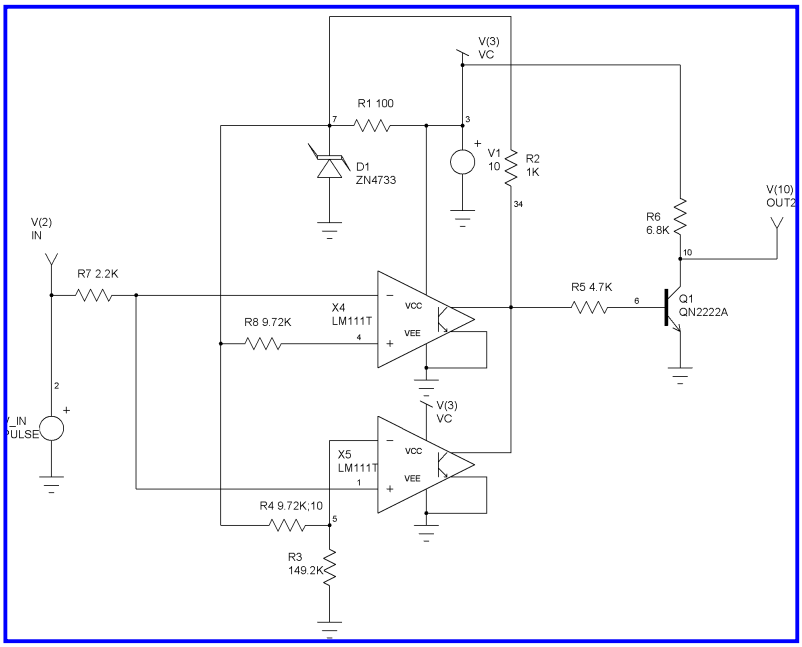


Figure 25-1: Schematic of the Window Comparator Circuit

Input Voltage Signal	Comparator Output	2N2222A Signal Output
Vin < 4.8 volts	Pulled low to ~ 100 mV	Pulled high to 10 volts
4.8 volts < Vin < 5.1 Volts	Pulled high to 5.1 volts	Low signal (~ 100 mV)
Vin > 5.1 volts	Pulled low to ~ 100 mV	Pulled high to 10 volts

Table 25-1: Circuit Behavior of window comparator

Transistor Q1 and resistors R5 and R6 simply realize an inverting function to provide the output of the circuit. In many cases, comparators in their normal operating steady state will have a high output in order to minimize power dissipation. This circuit follows that tradition, however also provides for a logic high output to drive control circuitry (such as a latch).

Three different measurements were made in order to characterize the performance of this window comparator circuit and show the correlation of the breadboard results to the SPICE models. The three inputs and their SPICE statements are described in detail in Table 25-2.

VIN PULSE 2 5 2.25M 1U 1U 2.75M 3M TRAN 1U 16M 6M 2U	Square wave from 2 to 5 volts at 333 Hz with a 90% duty cycle
VIN PULSE 5 8 2M 1U 1U 275U 3M TRAN 1U 10M 0 2U	Square wave from 5 to 8 volts at 333 Hz with a 10 % duty cycle
VIN PULSE 4 8 0 4M 4M 1U 8M TRAN 1U 13M 3M 2U	Triangular waveform from 4 to 8 volts at 125 Hz with a 50% duty cycle

Table 25-2: Characteristic Measurements made on window comparator circuit

The breadboard results of the comparator circuit when a 2 to 5 volt square wave is sensed is shown in Figure 25-2. The IsSpice results are shown in Figure 25-3 and the Microcap results are shown in Figure 25-4. It was not possible to simulate this circuit using the evaluation version of Pspice, because the number of transistors allowed was exceeded.

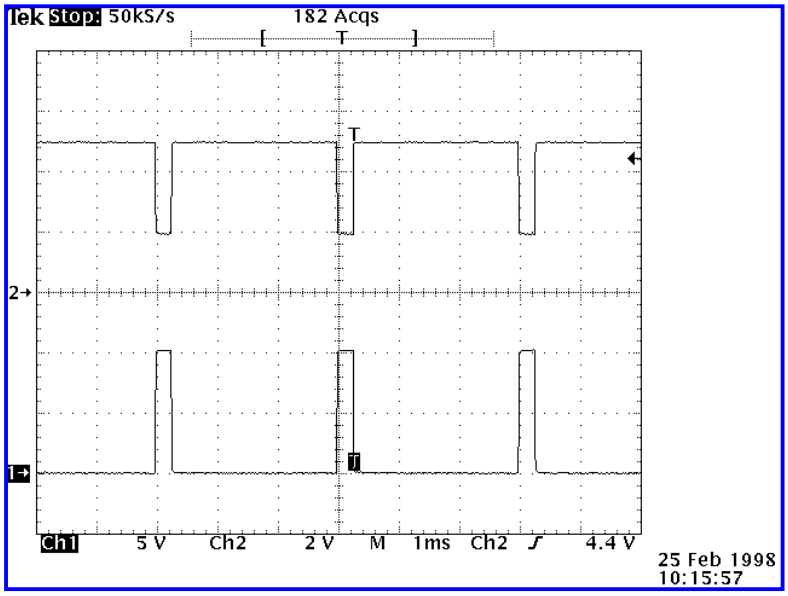


Figure 25-2: Breadboard results of 2 to 5 volt square wave input

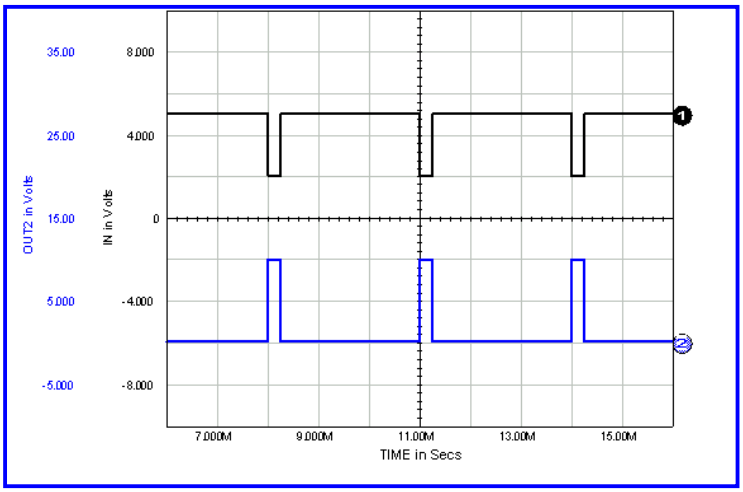


Figure 25-3: IsSpice results of 2 to 5 volt square wave input

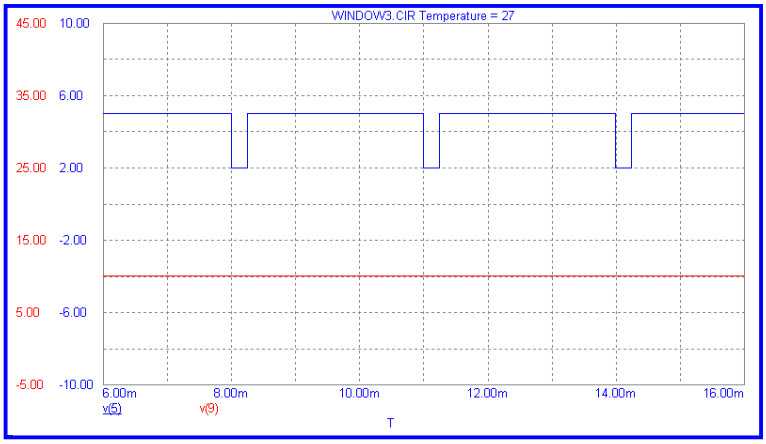


Figure 25-4: Microcap result of 2 to 5 volt square wave input

Examining the results of Figure 25-4, it is noted there was no state change

when the input signal transitioned between 2 and 5. Upon further examination, the culprit was determined to be the Microcap zener diode model of the 1N4733.

Using the Microsemi ® data sheet of the 1N4733A, the data sheet shows a nominal zener voltage of 5.1 volts at a test current of 49 mA. The IsSpice model shows 5.101 volts at 49 mA, while the Microcap model shows 5.819 volts at a current of 42 mA. With results such as these, the logical question is are the models correct?

In order to answer this question, the zener voltages vs. zener currents were plotted for the Microcap diode, IsSpice diode, and a lab diode. The test circuit is shown below in Figure 25-5.

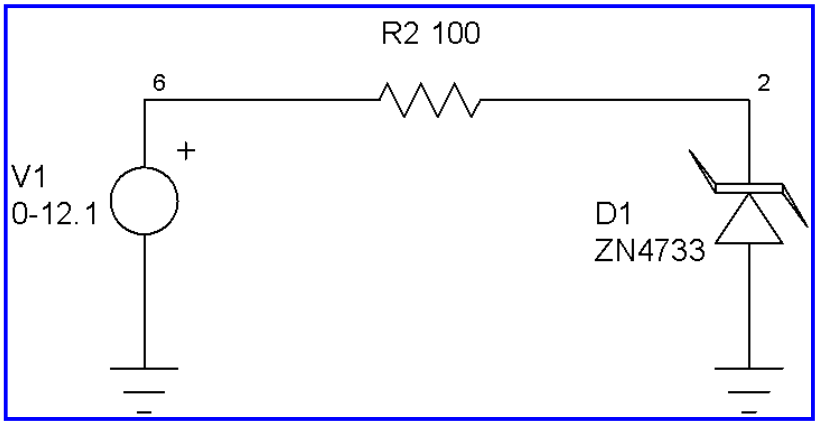


Figure 25-5: Breadboard frequency response results

The lab diode used the figure 25-5 configuration and zener current vs. zener voltage was plotted. The graph in Figure 25-6 shows the curves for the Microcap 1N4733, IsSpice 1N4733, and a 1N4733A model designed by Analytical Engineering.

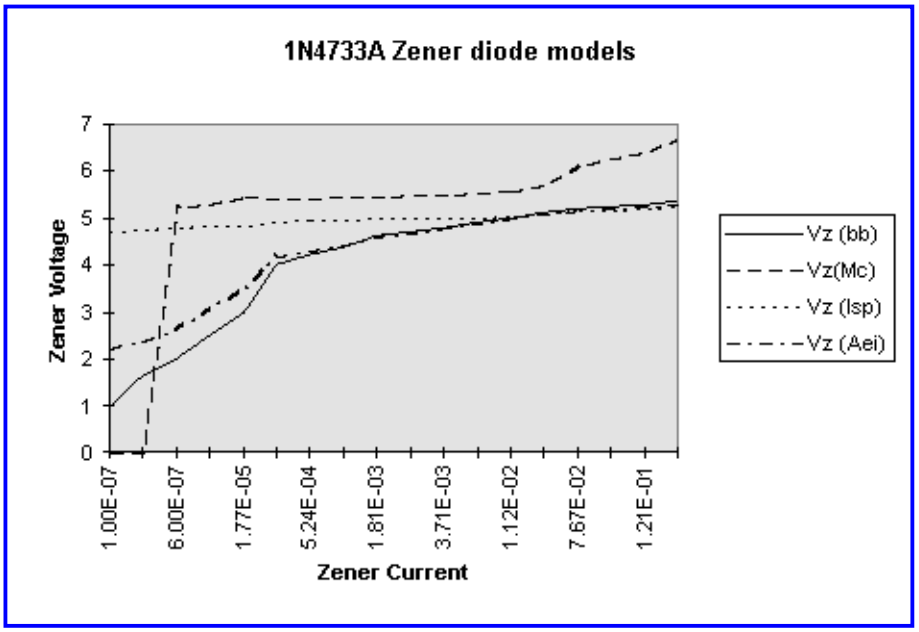


Figure 25-6: 1N4733 diode plots - Zener current vs. Zener voltage

Examining the results of Figure 25-6, it is noted the measured data of the lab diode shows a knee at approximately 3.9 volts. Above this point, the zener voltage changes at a different rate than below this point. In order to properly model the zener voltage at both of these regions, a subcircuit is required. The results of Figure 25-6 clearly illustrate the advantages of using a subcircuit to model a zener diode.

In order to allow the Microcap SPICE model of the window comparator to run properly, the AEI zener diode model was used instead of the 1N4733 model that ships with Microcap. The 2 to 5 volt square wave was fed into the modified Microcap model. The results are shown in Figure 25-7.

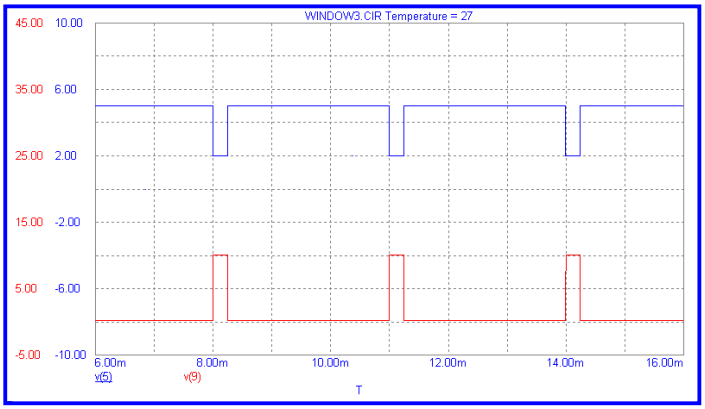


Figure 25-7: Microcap results of 2 to 5 volt square wave input

The breadboard, IsSpice, and Microcap (with AEI diode model) results of a 5 to 8 volt square wave input are shown in Figures 25-8 through 25-10. The breadboard, IsSpice, and Microcap results of a triangular waveform from 4 to 8 volts are shown in Figures 25-11 through 25-13.

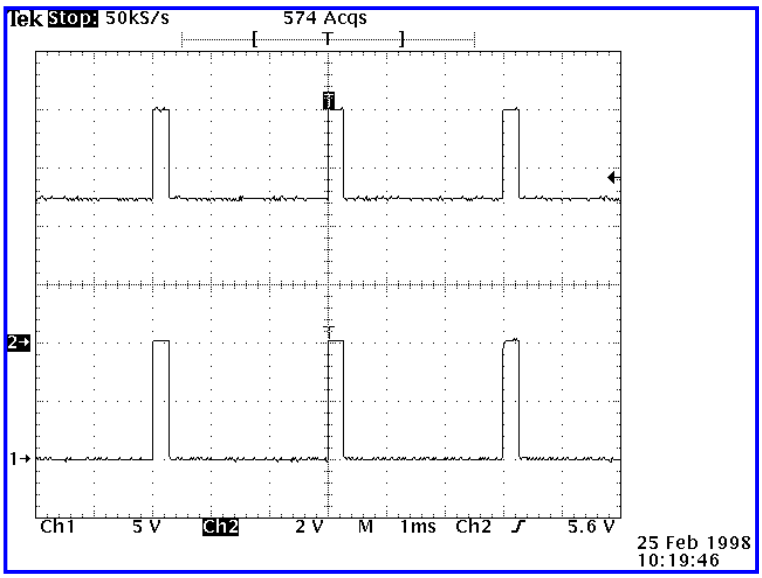


Figure 25-8: Breadboard results of 5 to 8 volt square wave input

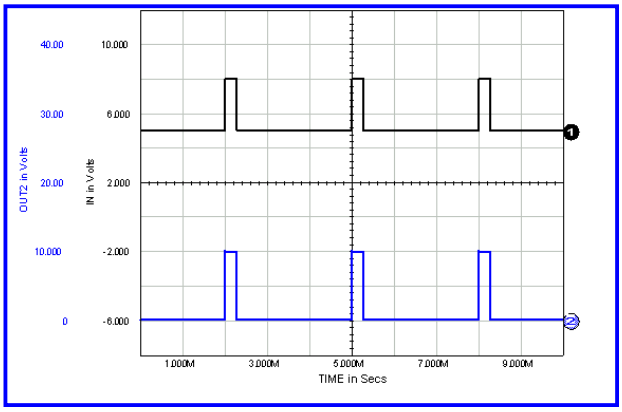


Figure 25-9: IsSpice results of 5 to 8 volt square wave input

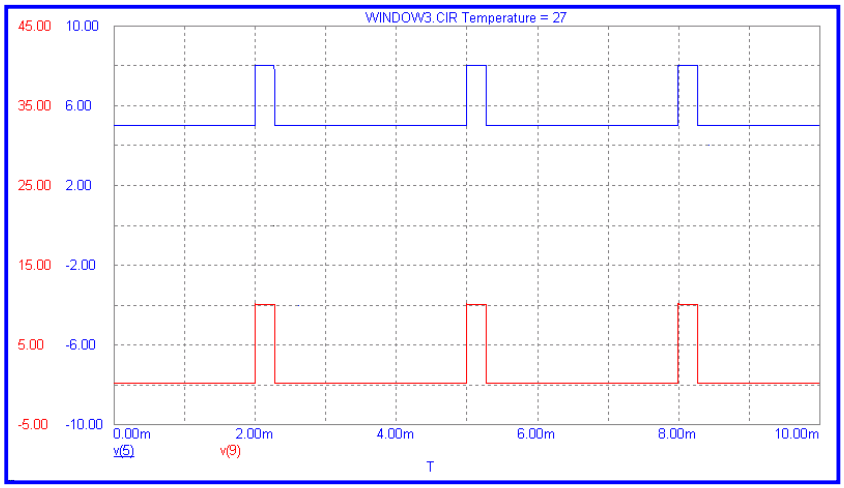


Figure 25-10: IsSpice results of 5 to 8 volt square wave input

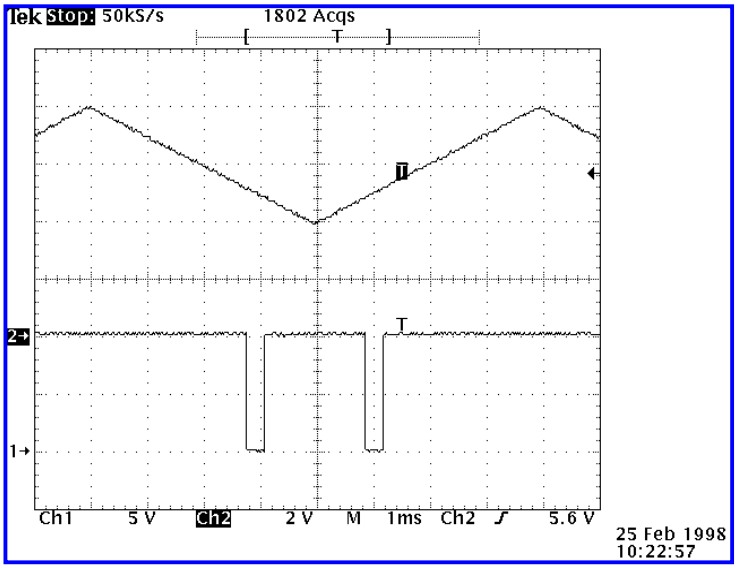


Figure 25-11: Breadboard results of 4 to 8 volt triangle wave input

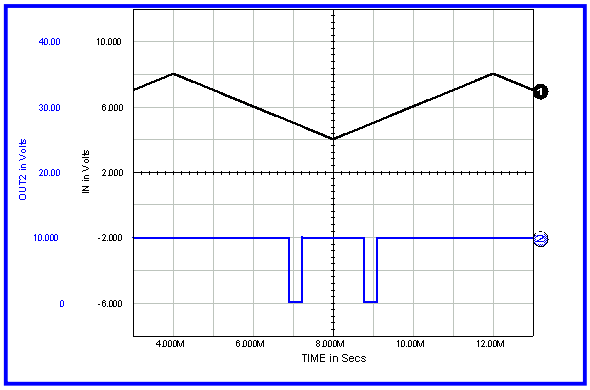


Figure 25-12: IsSpice results of 4 to 8 volt triangle wave input

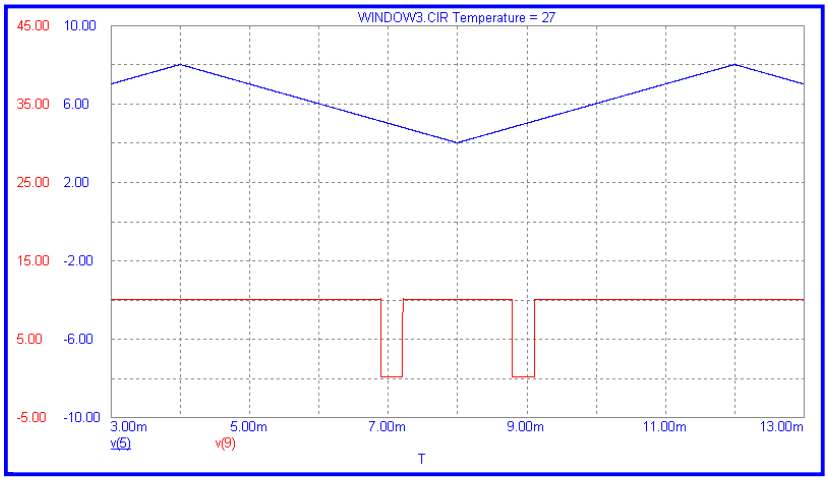


Figure 25-13: Microcap results of 4 to 8 volt triangle wave input

Run Time Summary		
IsSpice v 7.6	Pspice v 6.3	Micro-Cap V v2
20.6 Sec	N/A*	31.68 Sec
Advantages: versatile and easily adjustable		
Disadvantages: poor Zener diode accuracy (5% initial tolerance) creates errors in trip points. Other circuit variants more precise		

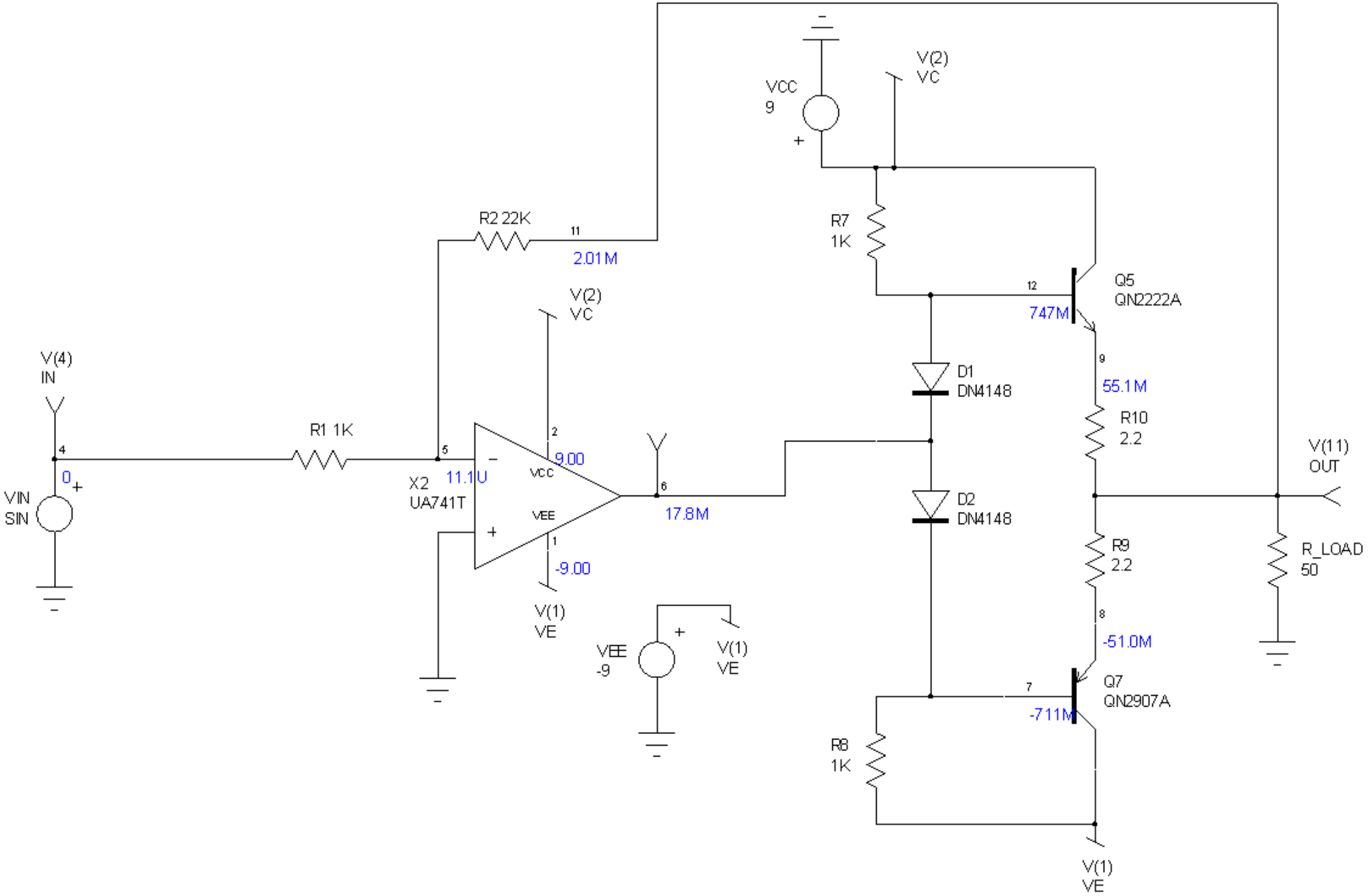
*The evaluation version of Pspice was not capable of simulating this circuit

Filenames: Window (IsSpice) Window3 (Microcap) 1N4733A.XLS (Excel)

REFERENCES

Gilbilisco, Stan, Ed. Encyclopedia of Electronics. TAB Books. PA: 1985

Gilbilisco, Stan, Ed. Amateur Radio Encyclopedia. TAB Books. PA: 1994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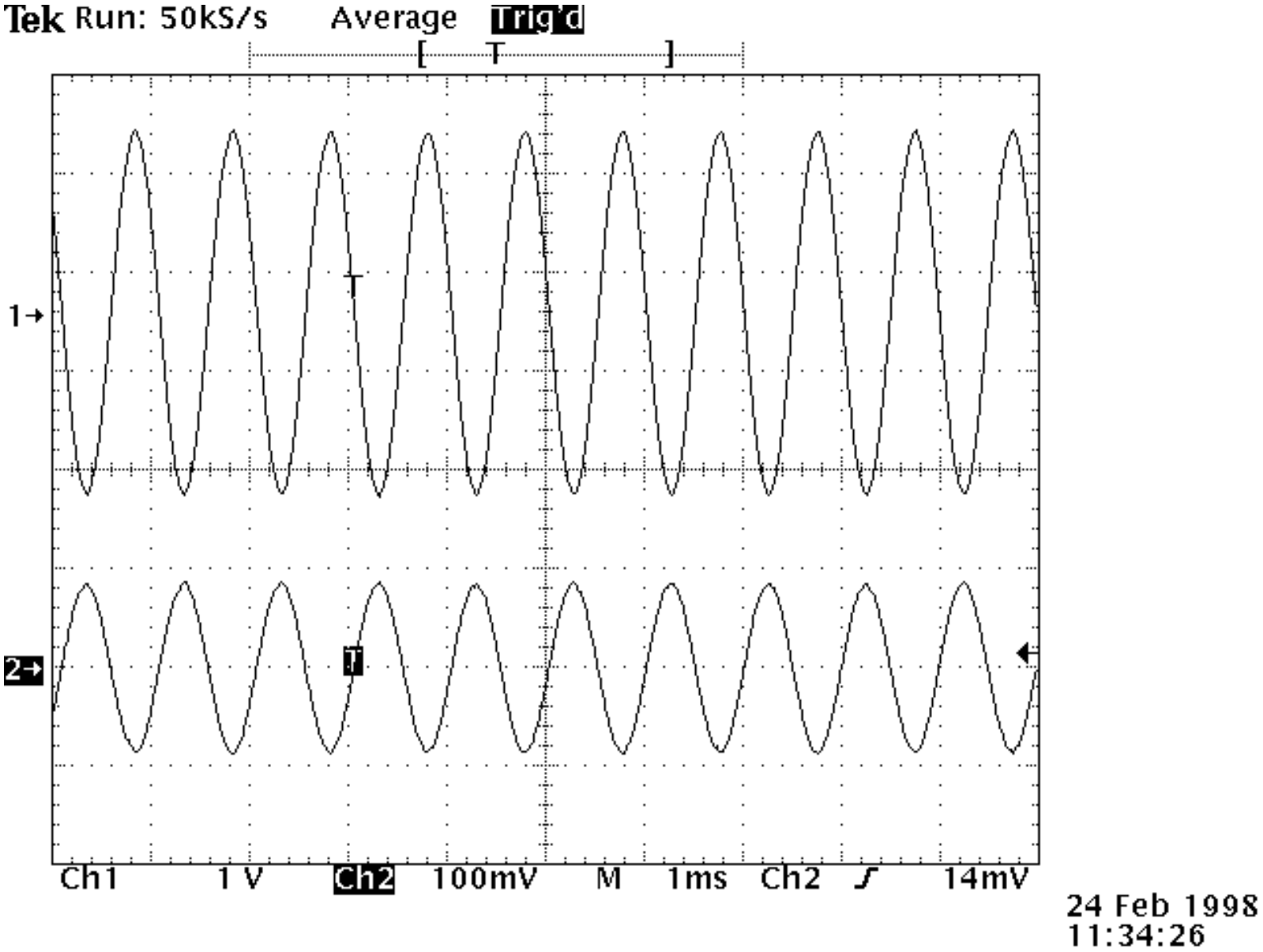
V(2)
VC
R2 22K
11
2.01M
R7
1K
12
Q5
QN2222A
747M
V(2)
VC
V(4)
IN
D1
DN4148
9
55.1M
R10
2.2
V(11)
OUT
R1 1K
4
5
2
9.00
0
VIN
SIN
X2
UA741T
11.1U
VCC
VEE
6
17.8M
D2
DN4148
R9
2.2
R_LOAD
50
1
-9.00
V(1)
VE
VEE
-9
V(1)
VE
8
-51.0M
7
Q7
QN2907A
-711M
R8
1K
V(1)
VE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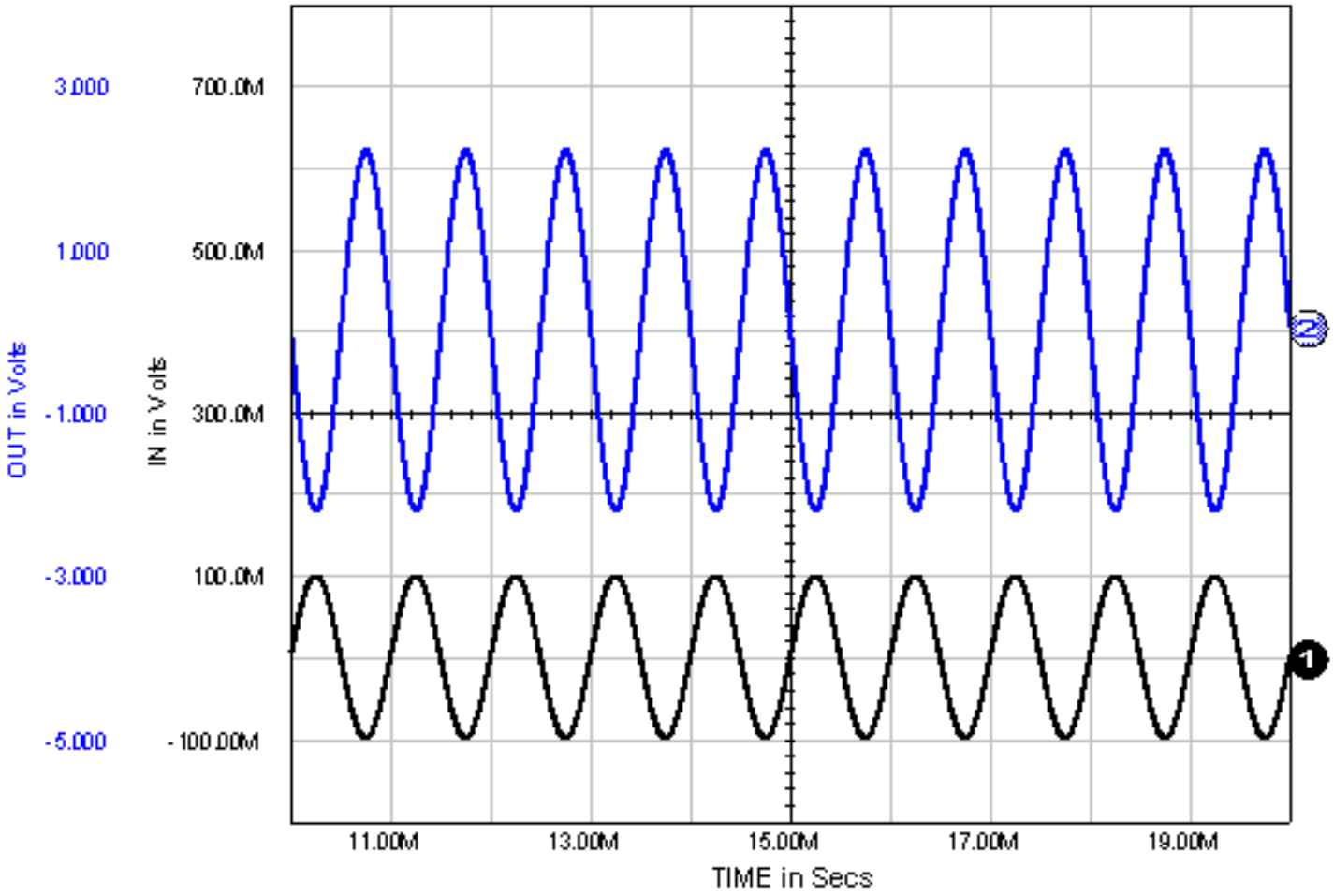
1→
2→
Ch1 1 V Ch2 100mV M 1ms Ch2 ∫ 14mV
24 Feb 1998
11:34:26


3.000
1.000
-1.000
-3.000
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OUT in Volts
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500.0M
300.0M
100.0M
-100.00M
IN in Volts
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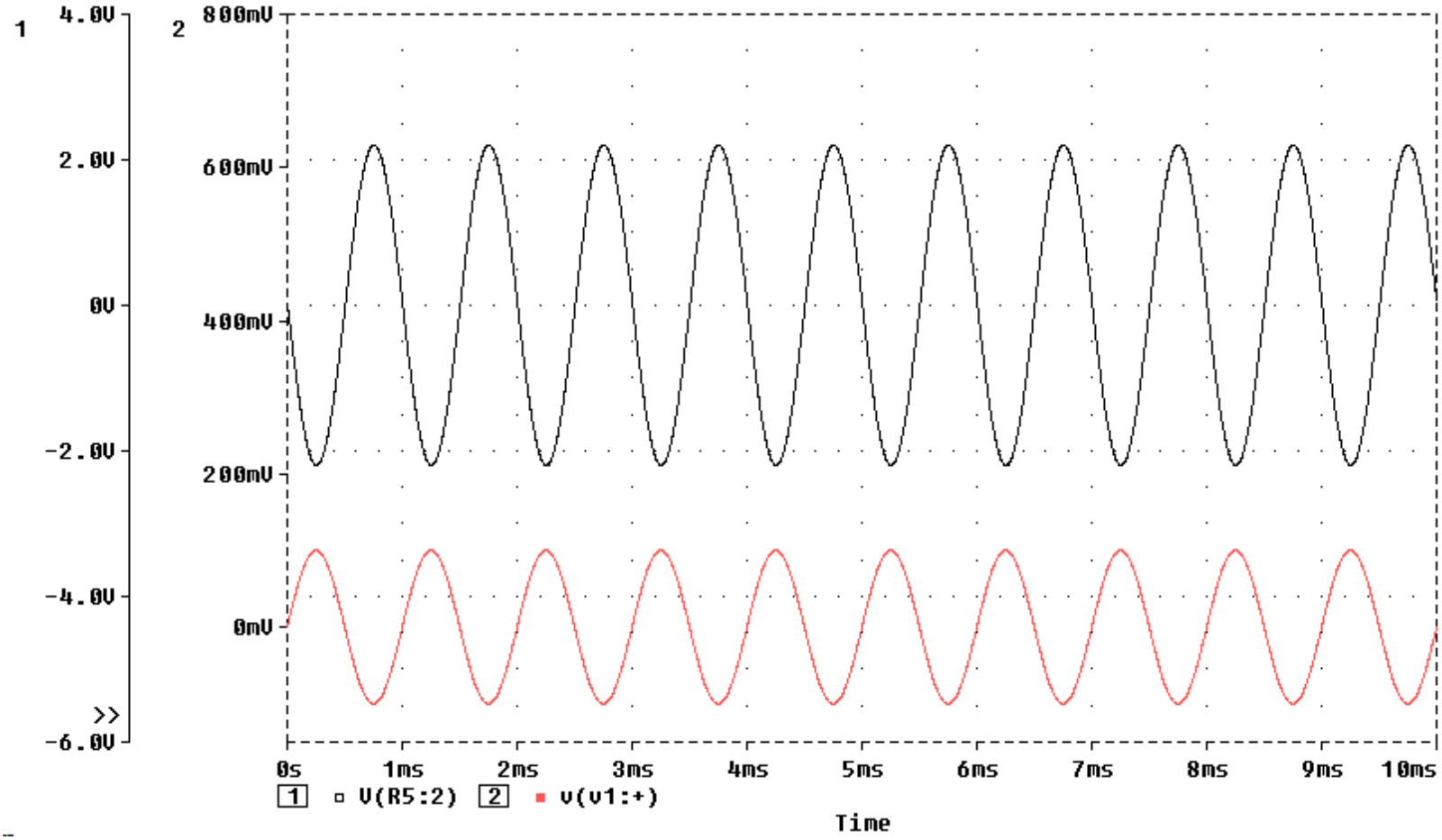
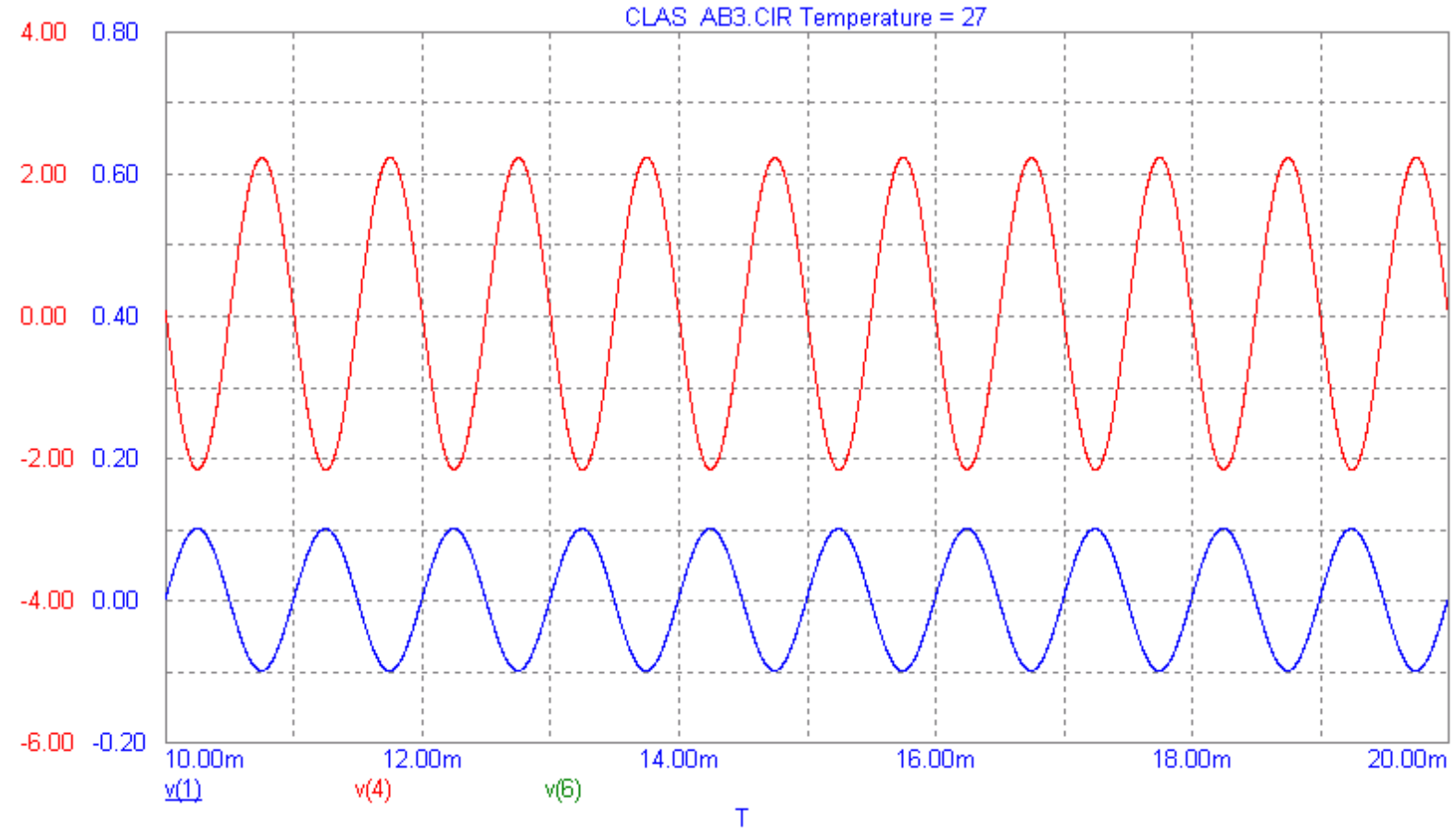
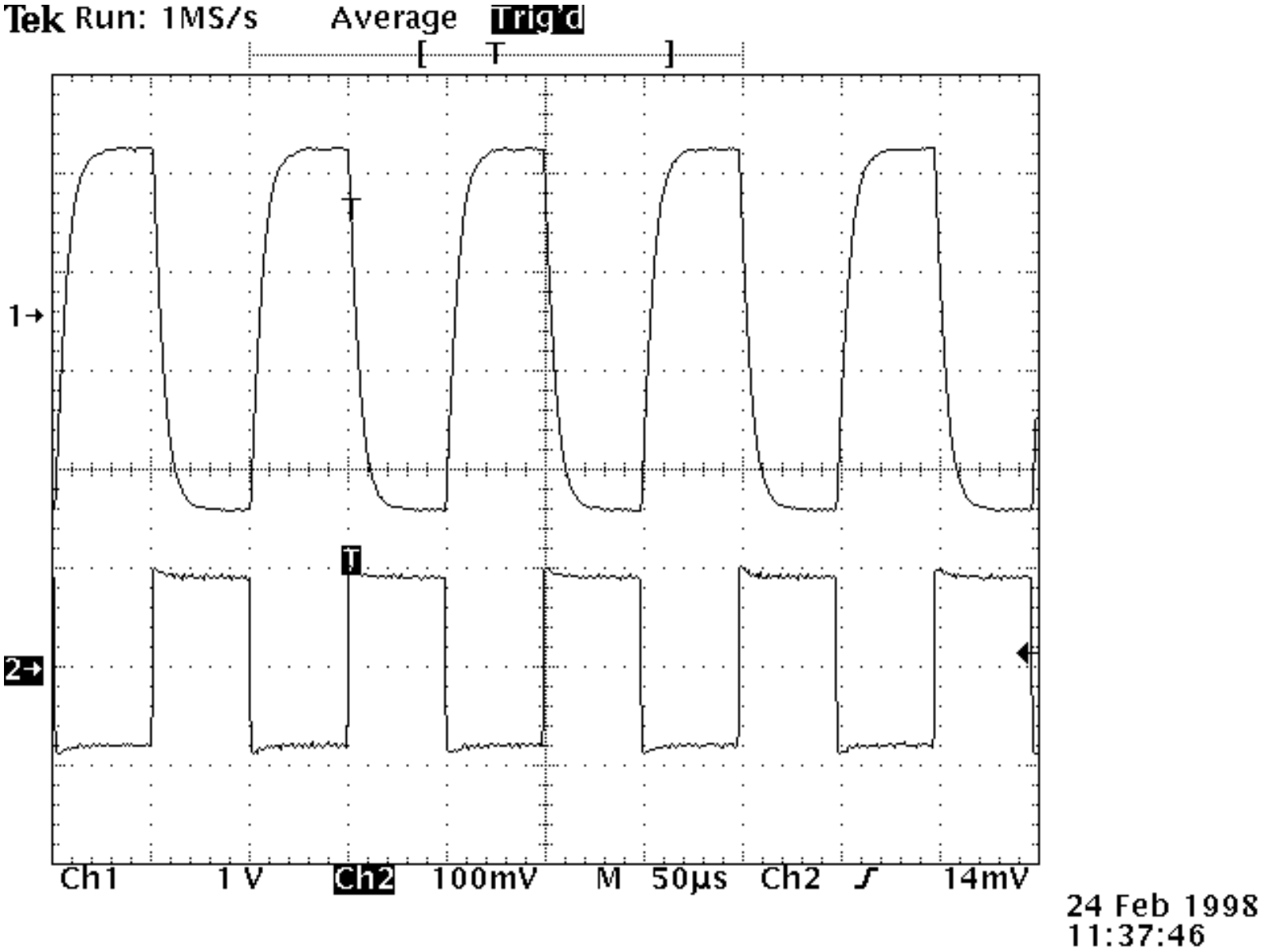
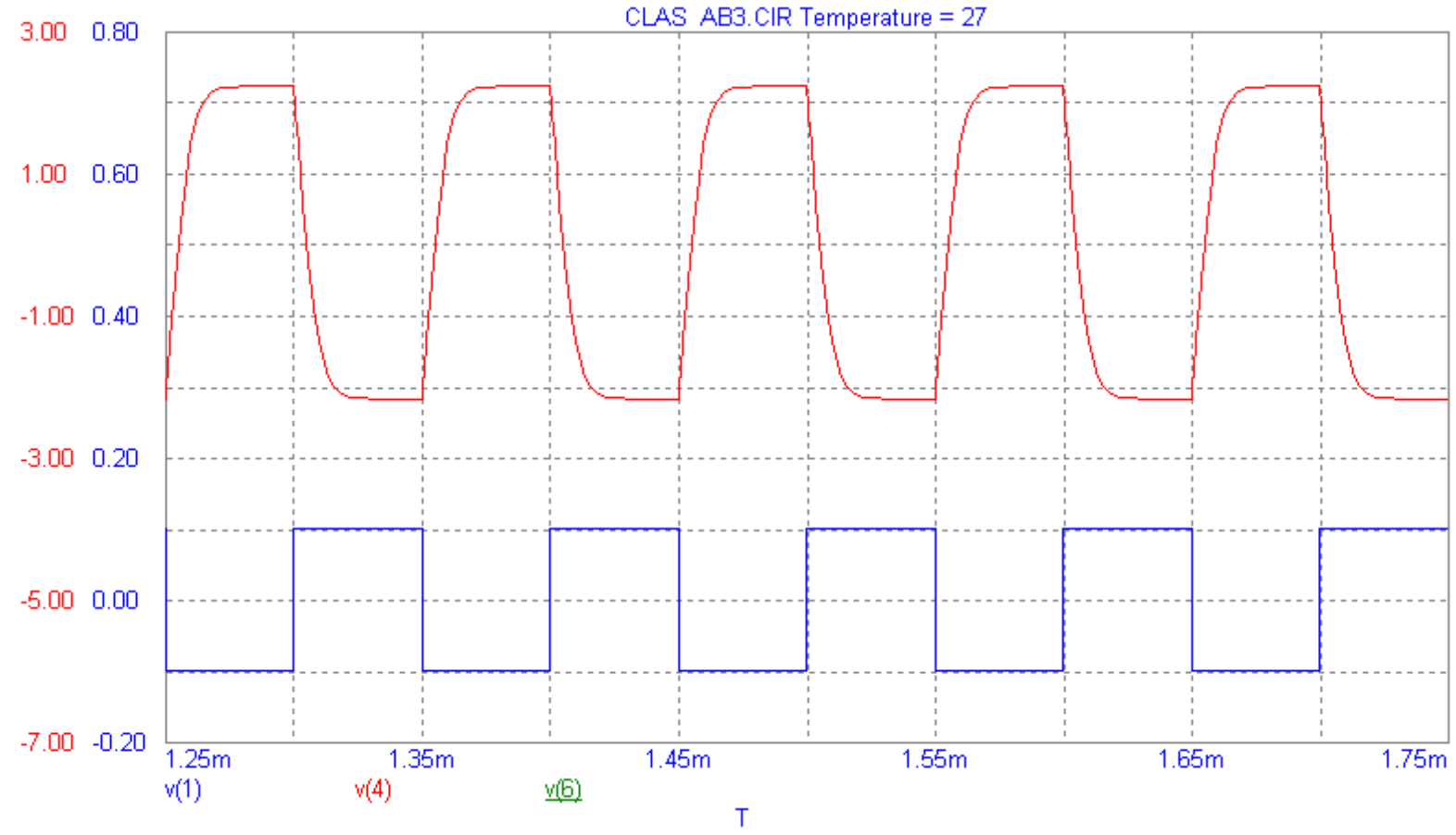
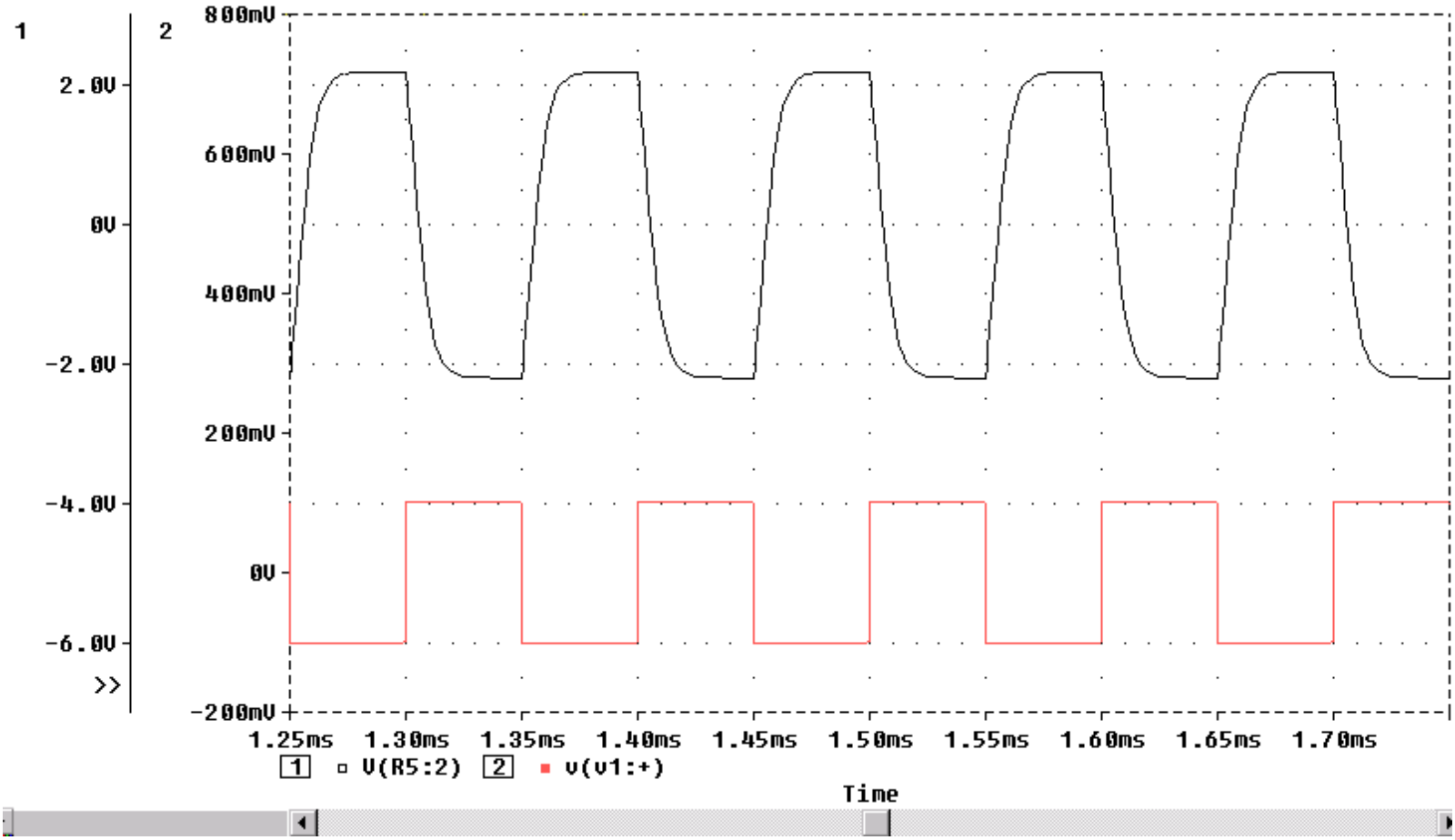
13.00M
15.00M
17.00M
19.00M
TIME in Secs
2
1

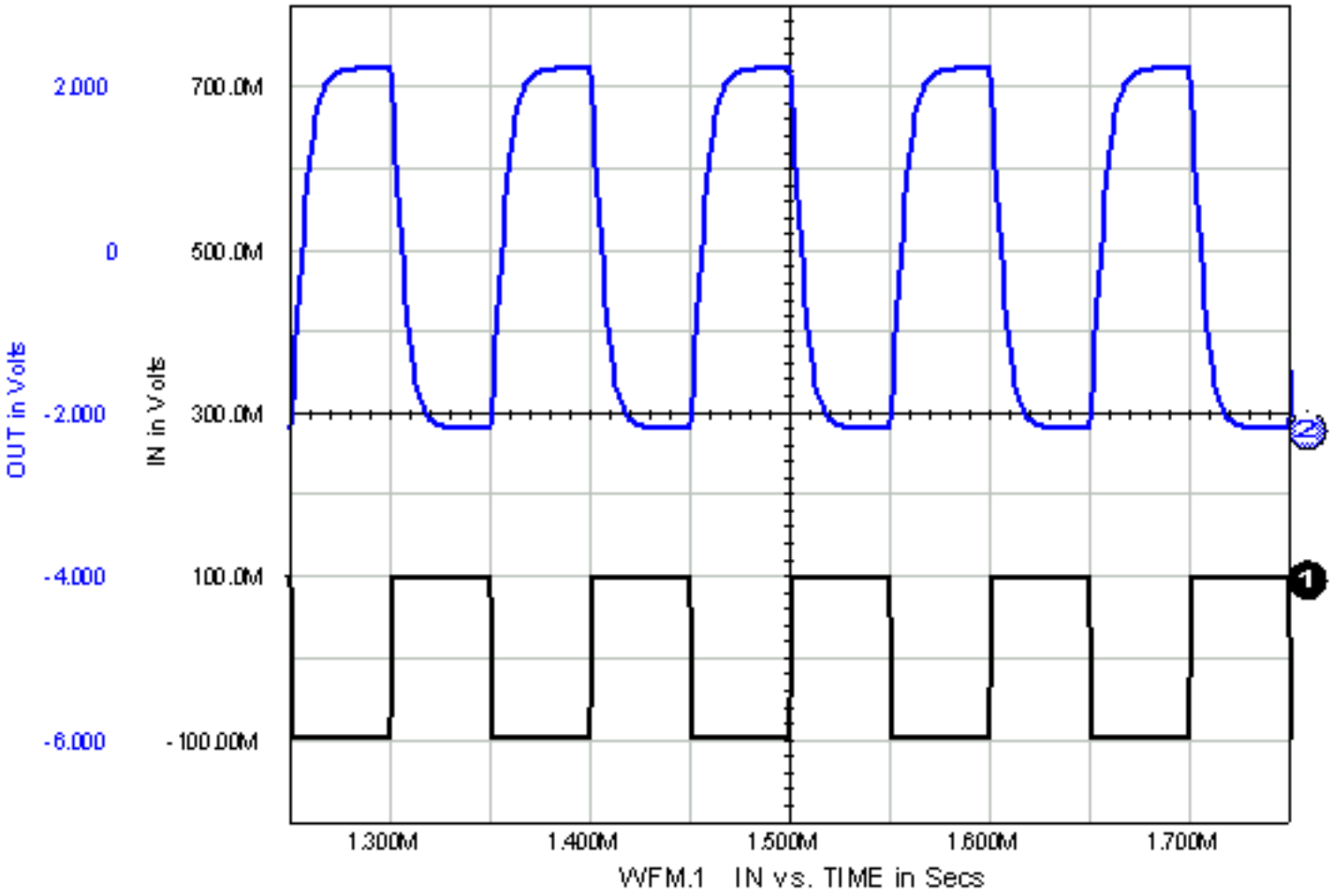

1
4.0V
2.0V
0V
-2.0V
-4.0V
>>
-6.0V
2
800mV
600mV
400mV
200mV
0mV
0s
1ms
2ms
3ms
4ms
5ms
6ms
7ms
8ms
9ms
10ms
1 V(R5:2) 2 V(V1:+)
Time

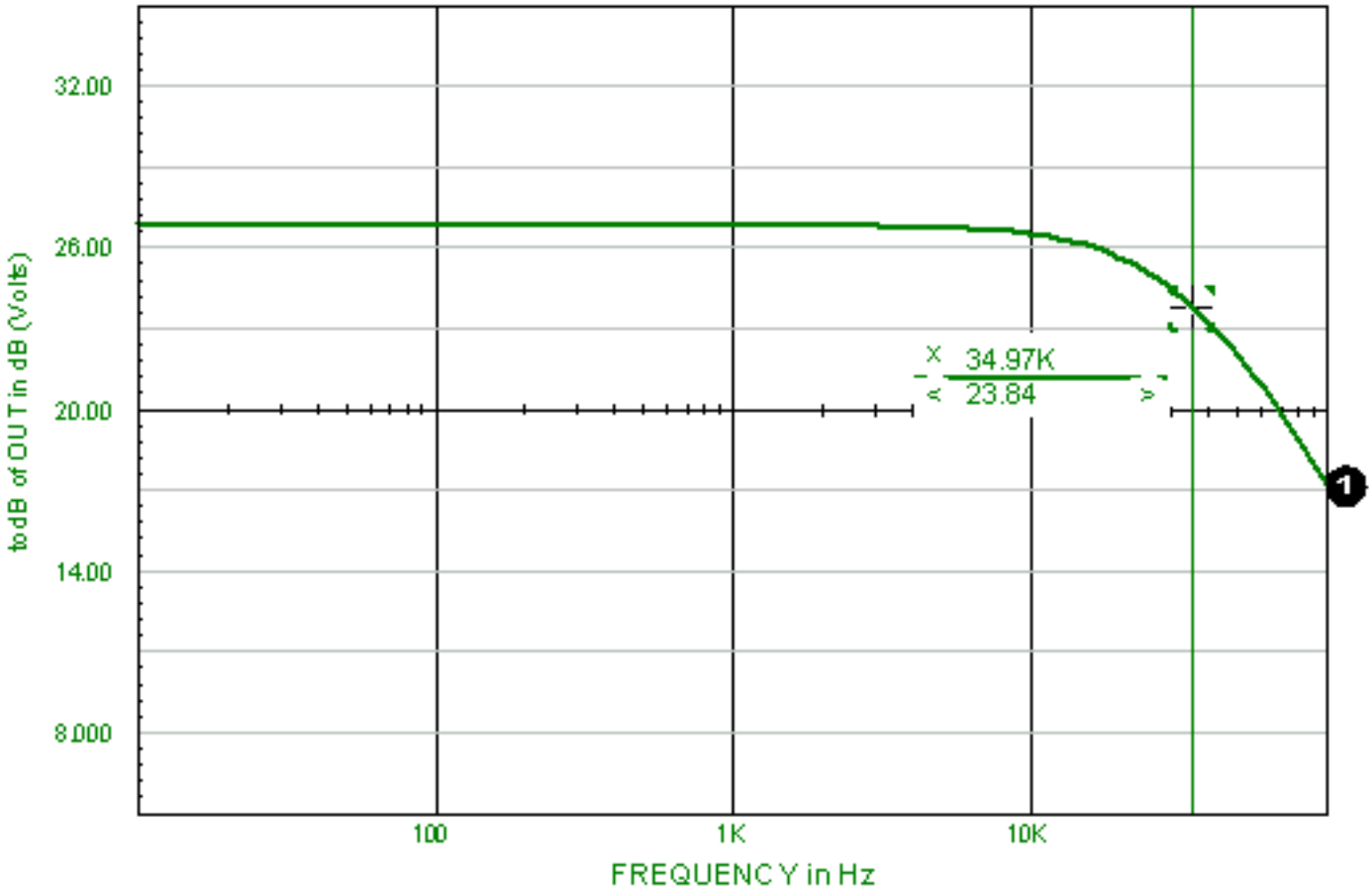

CLAS AB3.CIR Temperature = 27
4.00
0.80
2.00
0.60
0.00
0.40
-2.00
0.20
-4.00
0.00
-6.00
-0.20
10.00m
12.00m
14.00m
16.00m
18.00m
20.00m
v(1)
v(4)
v(6)
T

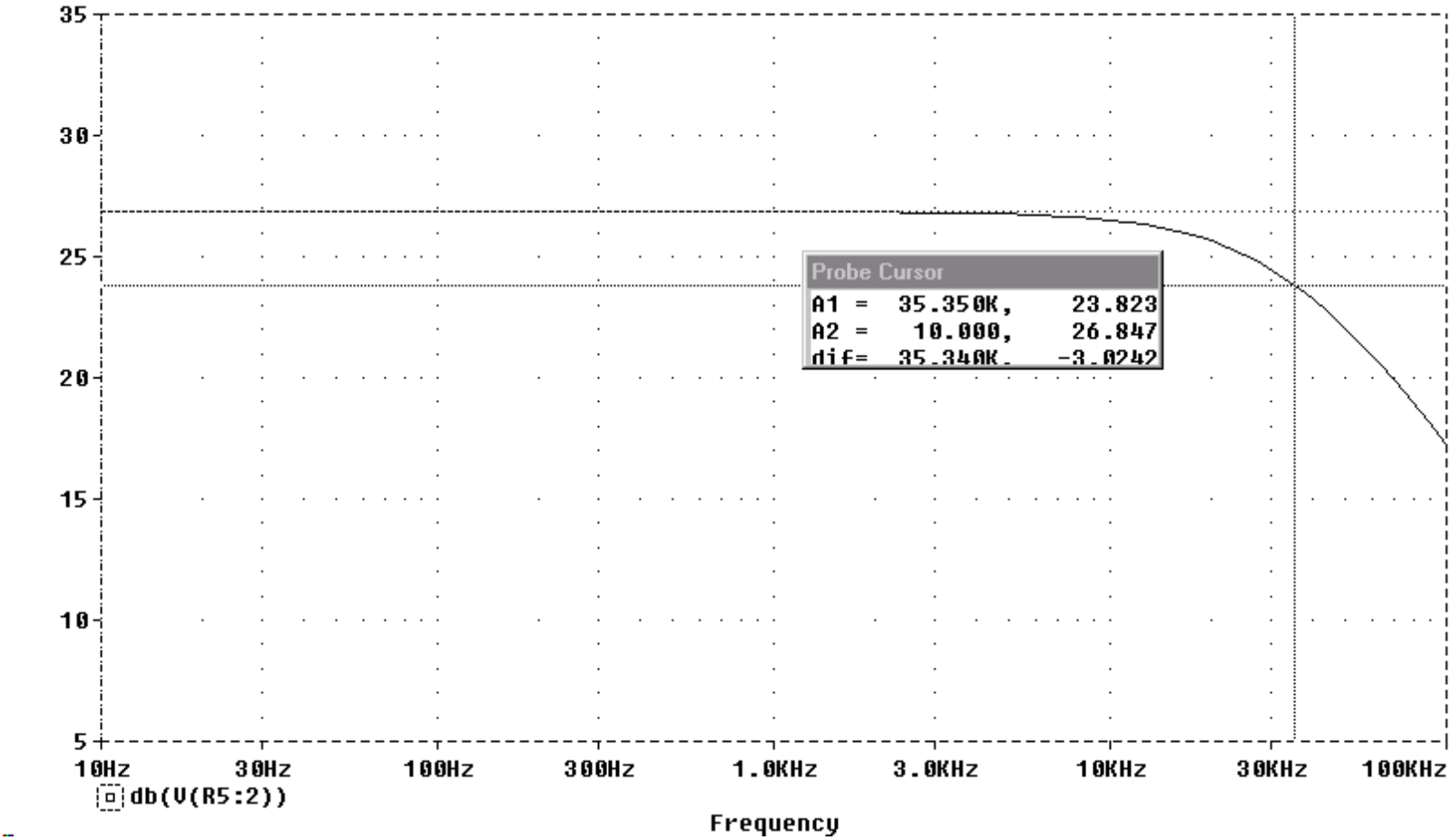

Tek Run: 1MS/s Average Trig'd
1→
2→
Ch1 1 V Ch2 100mV M 50µs Ch2 14mV
24 Feb 1998
11:37:46

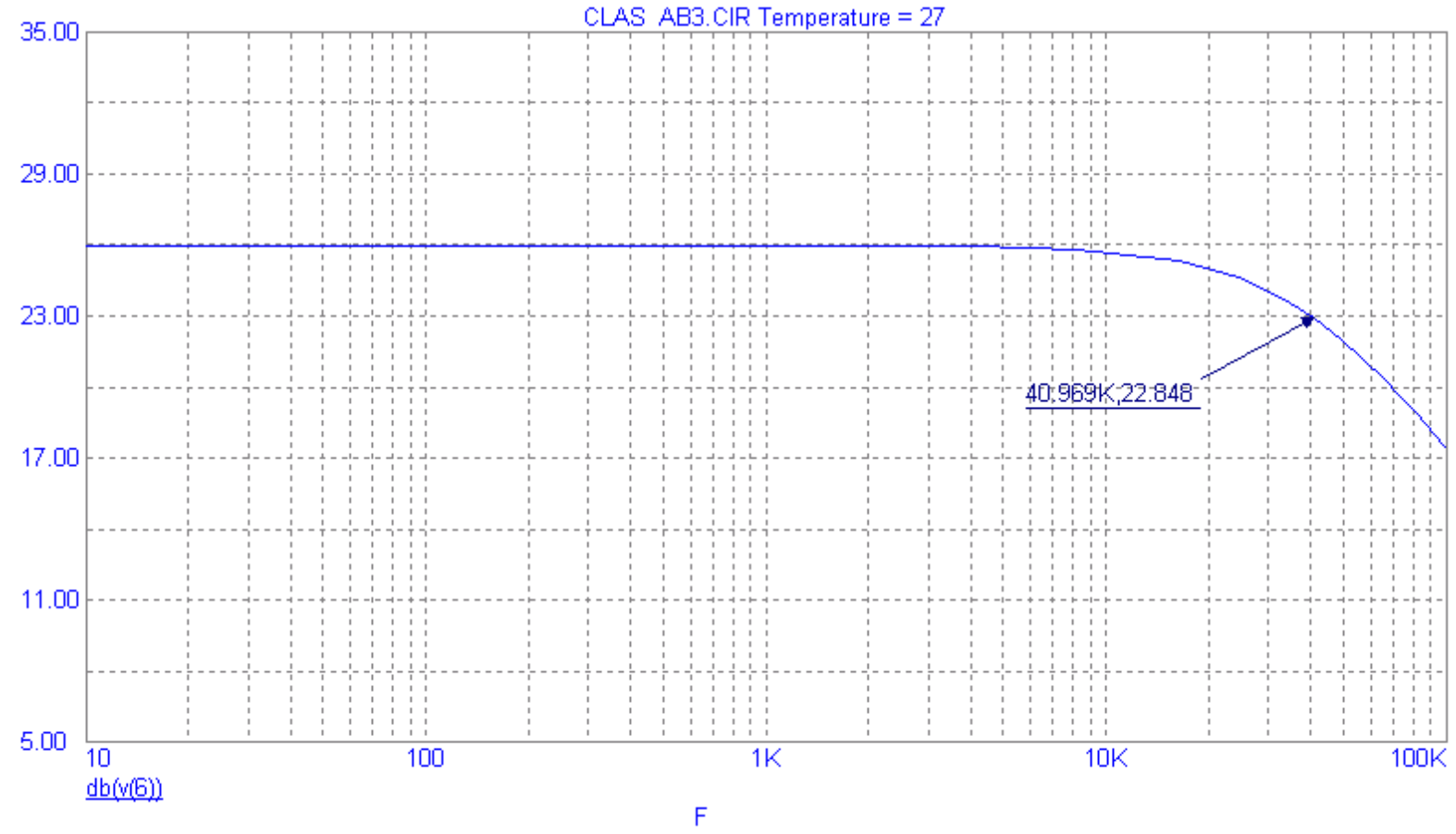

CLAS AB3.CIR Temperature = 27
3.00
0.80
1.00
0.60
-1.00
0.40
-3.00
0.20
-5.00
0.00
-7.00
-0.20
1.25m
1.35m
1.45m
1.55m
1.65m
1.75m
v(1)
v(4)
v(6)
T


1
2
800mV
2.0V
600mV
0V
400mV
-2.0V
200mV
-4.0V
0V
-6.0V
>>
-200mV
1.25ms
1.30ms
1.35ms
1.40ms
1.45ms
1.50ms
1.55ms
1.60ms
1.65ms
1.70ms
1 V(R5:2) 2 V(V1:+)
Time


2.000
0
-2.000
-4.000
-6.000
OUT in Volts
700.0M
500.0M
300.0M
100.0M
-100.00M
IN in Volts
1.300M
1.400M
1.500M
1.600M
1.700M
WFM.1 IN vs. TIME in Secs
2
1


32.00
26.00
20.00
14.00
8.000
to dB of OUT in dB (Volts)
X 34.97K
< 23.84 >
1
100
1K
10K
FREQUENCY in Hz


35
30
25
20
15
10
5
Probe Cursor
A1 = 35.350K, 23.823
A2 = 10.000, 26.847
dif= 35.340K, -3.0242
10Hz
30Hz
100Hz
300Hz
1.0KHz
3.0KHz
10KHz
30KHz
100KHz
db(V(R5:2))
Frequency


CLAS AB3.CIR Temperature = 27
35.00
29.00
23.00
17.00
11.00
5.00
40.969K,22.848
10
100
1K
10K
100K
db(v(6))
F

#26: Voltage Clamp

A voltage clamping circuit is a process setting the positive or negative peaks of an AC wave form to a specific DC level. A common method of creating a clamping circuit is the use of a capacitor diode network, or a zener diode. However, the accuracy of a zener diode is dependent of the operating current and temperature. Operating a zener diode at lower than tested currents, in the "soft" region, creates unpredictability in the temperature coefficient and the zener voltage.

The circuit shown in Figure 26-1 is a precision clamp, which can be constructed with an operational amplifier, resistor, and a reference voltage. A 500Hz sine wave and triangular waveform was used as an input signal in Figure 26-2 through Figure 26-9.

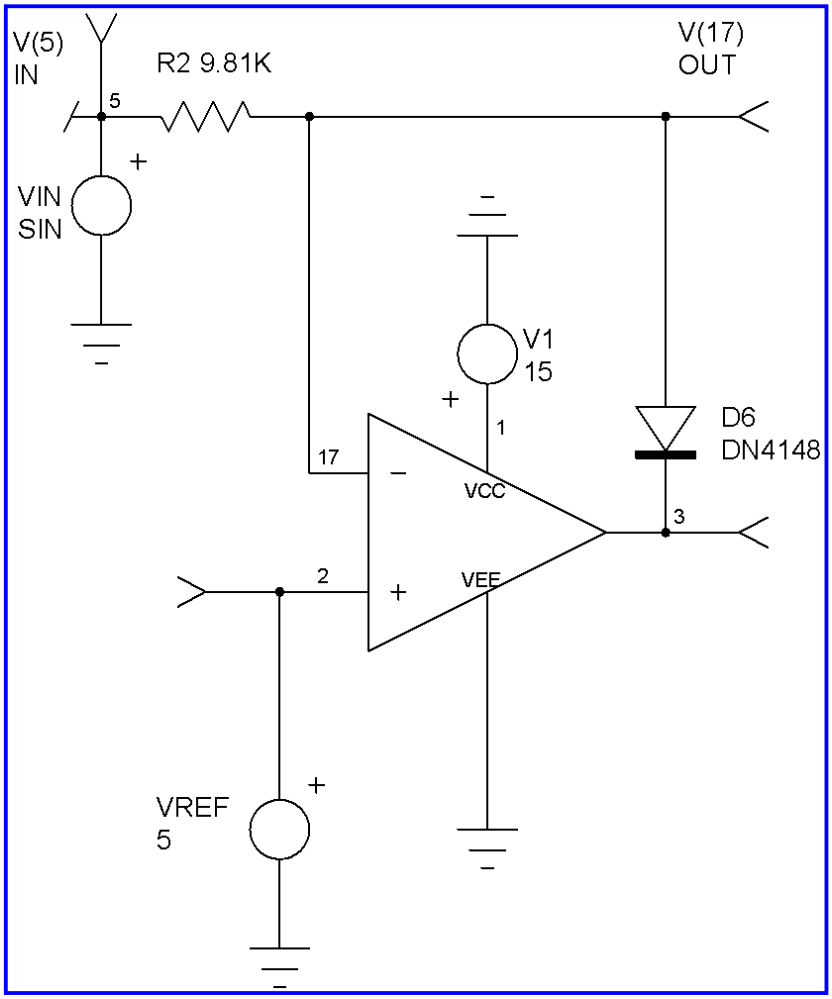


Figure 26-1: Voltage Clamping Circuit

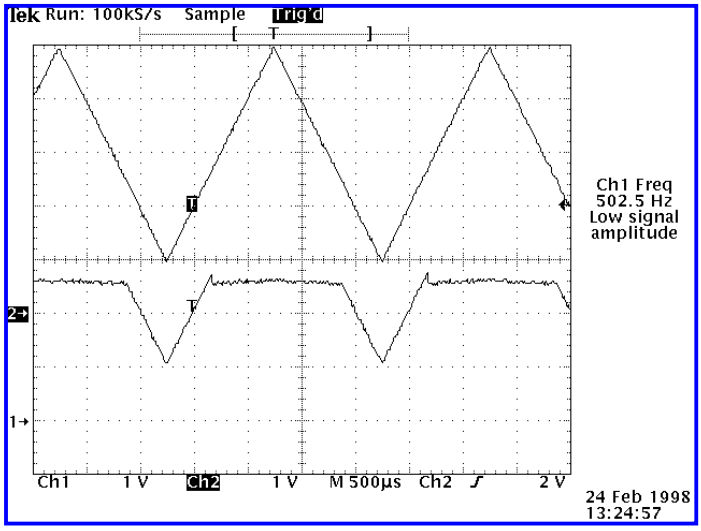


Figure 26-2: Measured Clamping of 500Hz Triangular Waveform

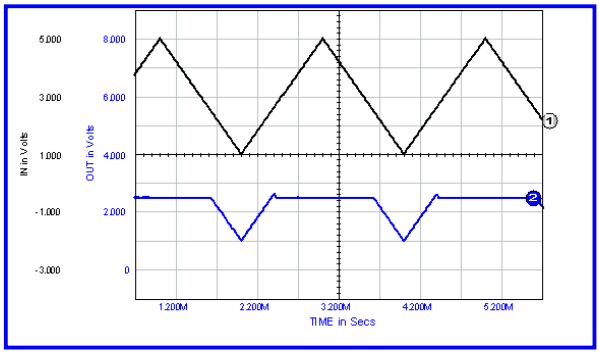


Figure 26-3: Ispice Simulated Clamping of 500Hz Triangular Waveform

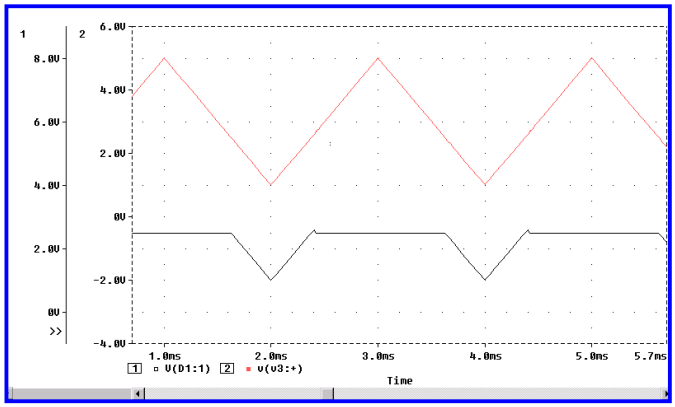


Figure 26-4: Pspice Simulated Clamping of 500Hz Triangular Waveform

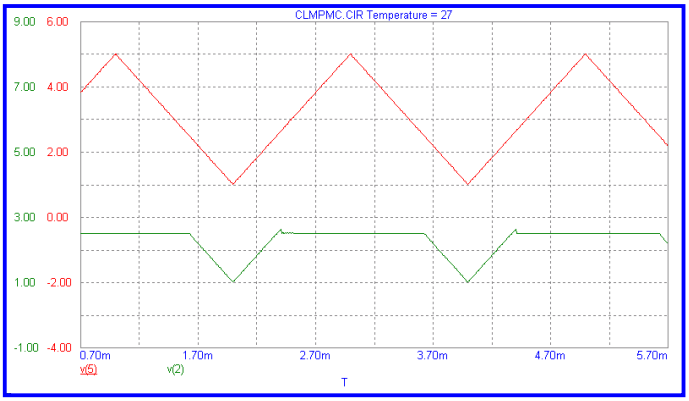


Figure 26-5: Micro-Cap V Simulated Clamping of 500Hz Triangular Waveform

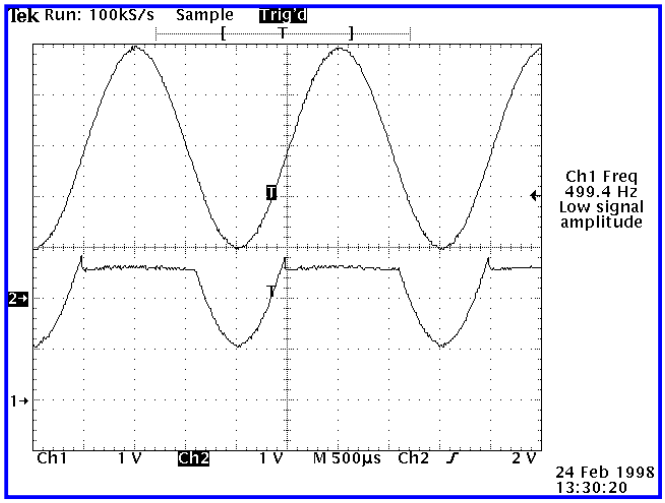


Figure 26-6: Measured Clamping of 500Hz Sine Waveform

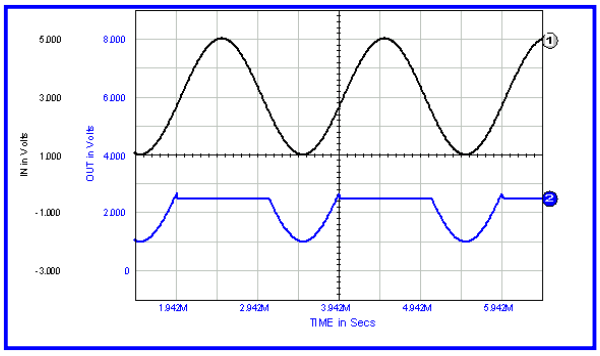


Figure 26-7: Ispice Simulated Clamping of 500Hz Sine Waveform

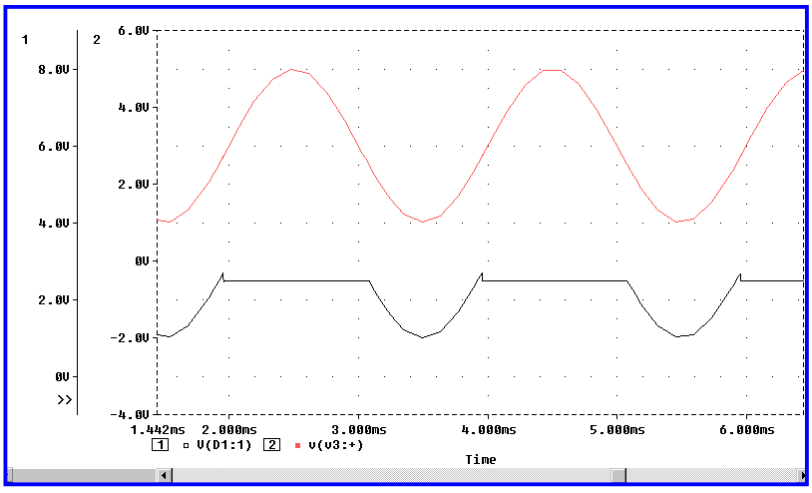


Figure 26-8: Pspice Simulated Clamping of 500Hz Sine Waveform

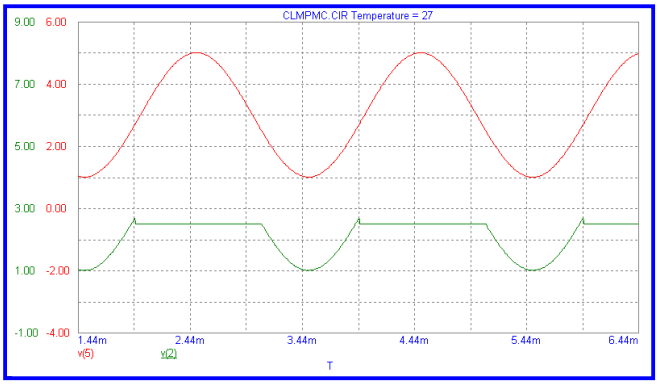


Figure 26-9: Micro-Cap V Simulated Clamping of 500Hz Sine Waveform

A 5KHz sine waveform was used as an input signal in Figure 26-9 through Figure 26-12.

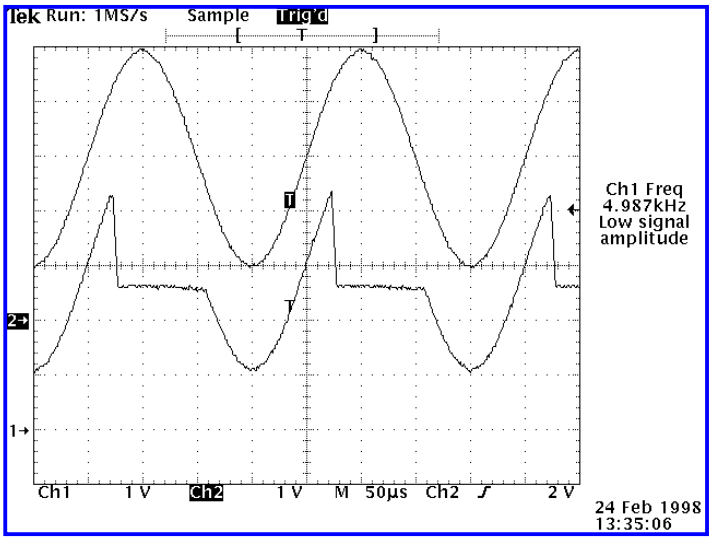


Figure 26-10: Measured Clamping of 5KHz Sine Waveform

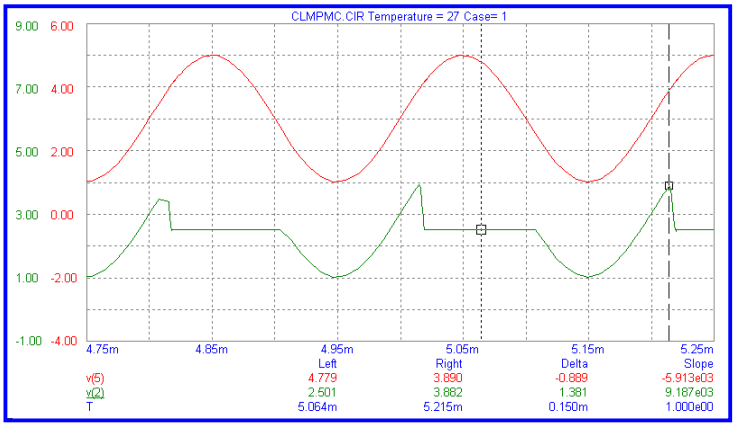


Figure 26-11: Micro-Cap V Simulated Clamping of 5KHz Sine Waveform

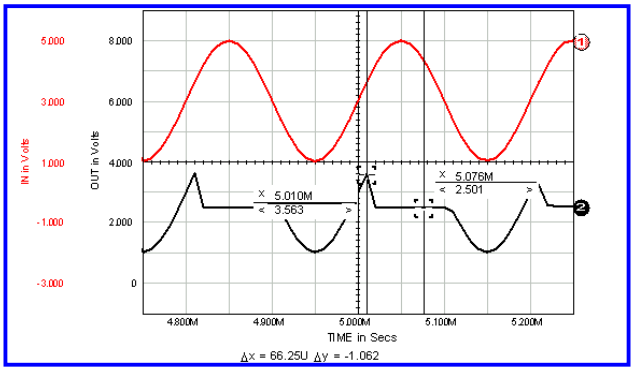


Figure 26-12: Ispice Simulated Clamping of 5KHz Sine Waveform

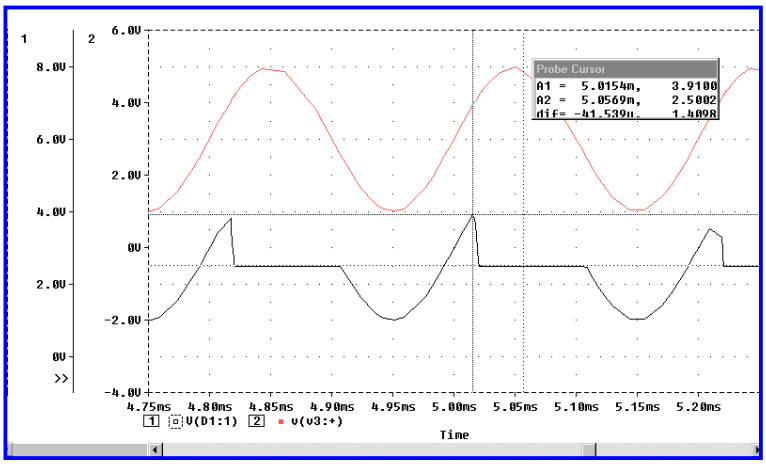


Figure 26-13: Pspice Simulated Clamping of 500Hz Sine Waveform

To reduce the switching spike select a operational amplifier larger slew rate. The simulation below compares the output of a UA741 to that of an LM318.

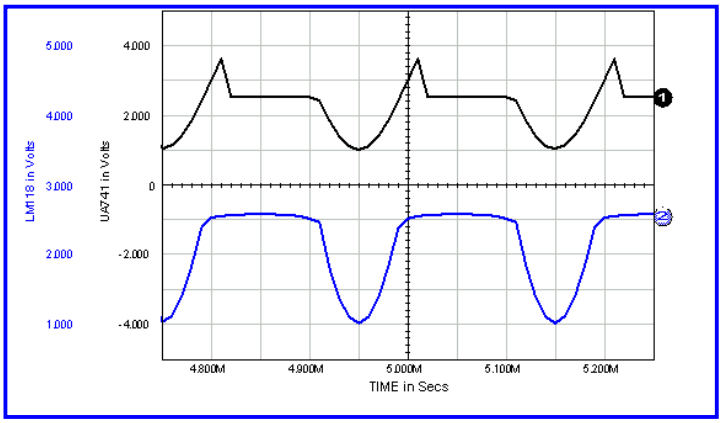
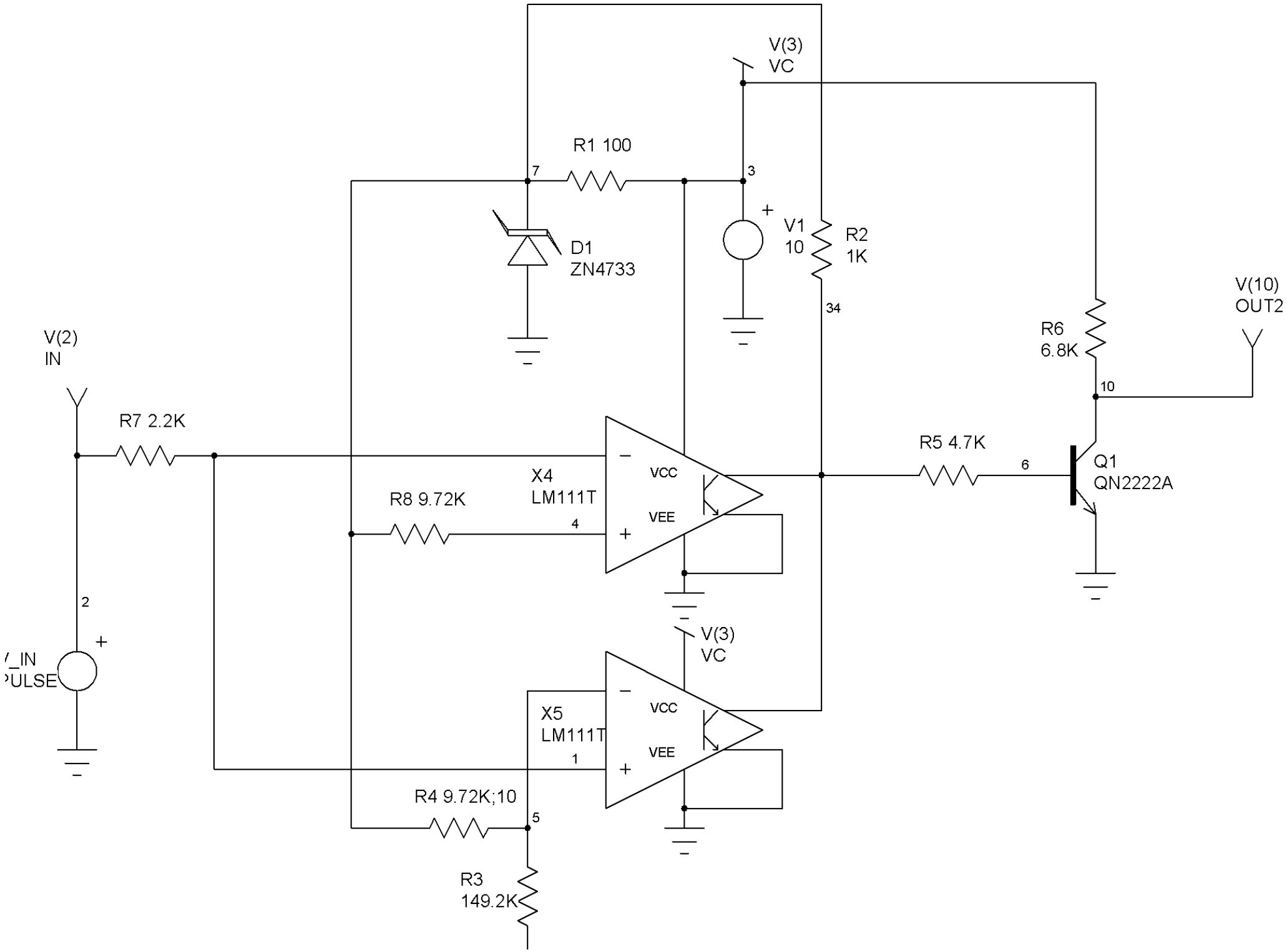
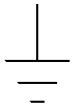


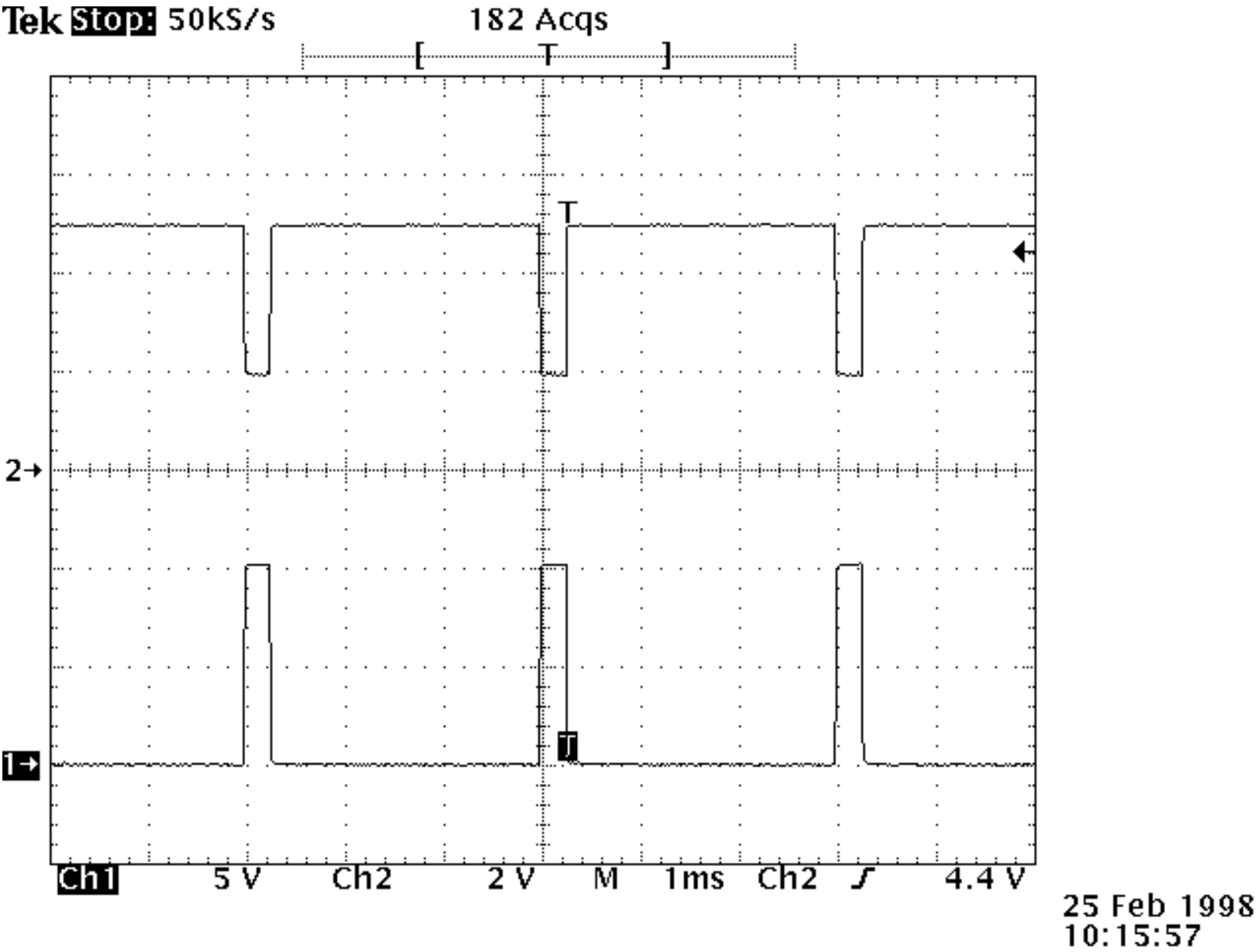
Figure 26-14: Clamping of UA741 (TOP) -VS- Clamping of LM318

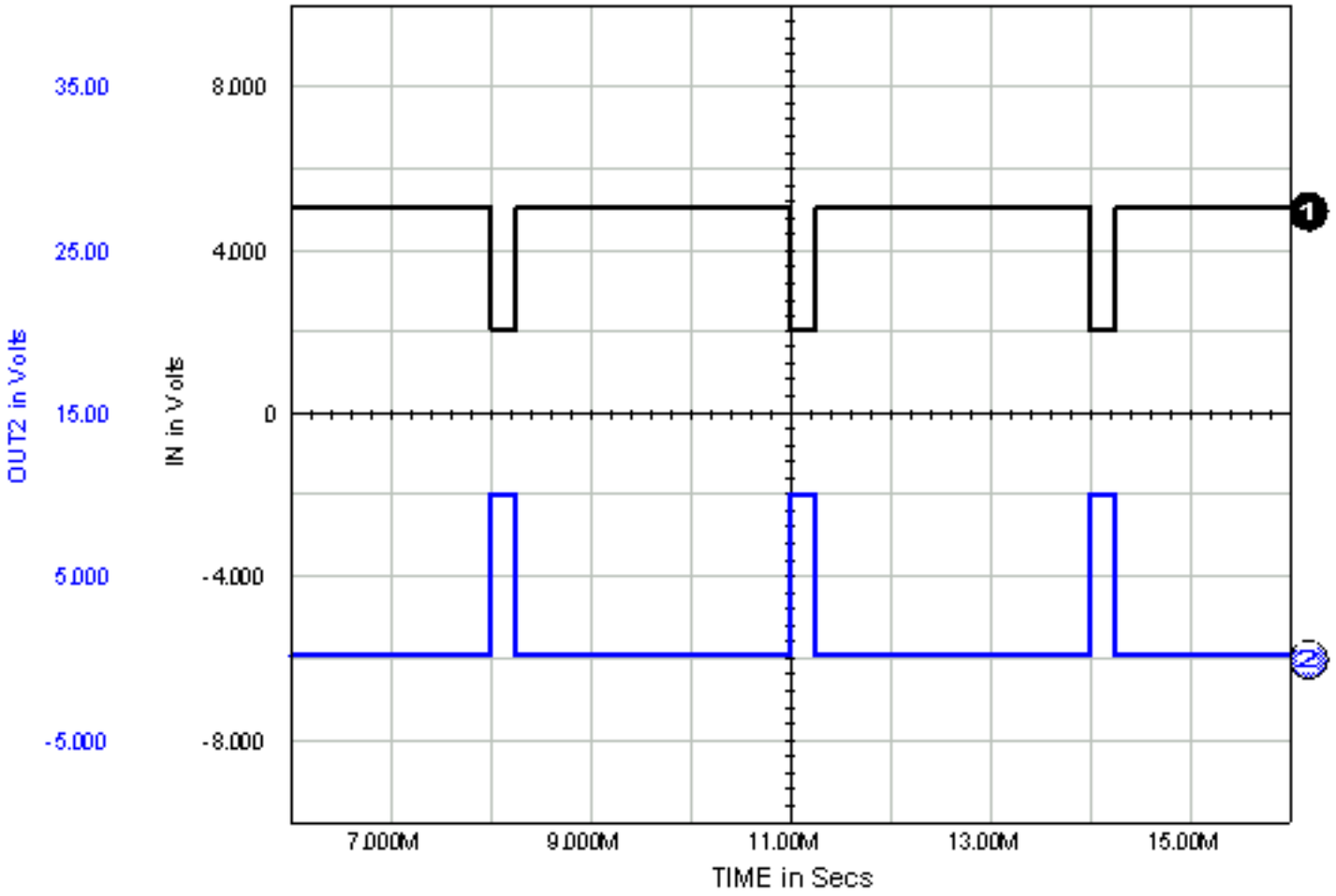
Table 26-1: Simulation Results

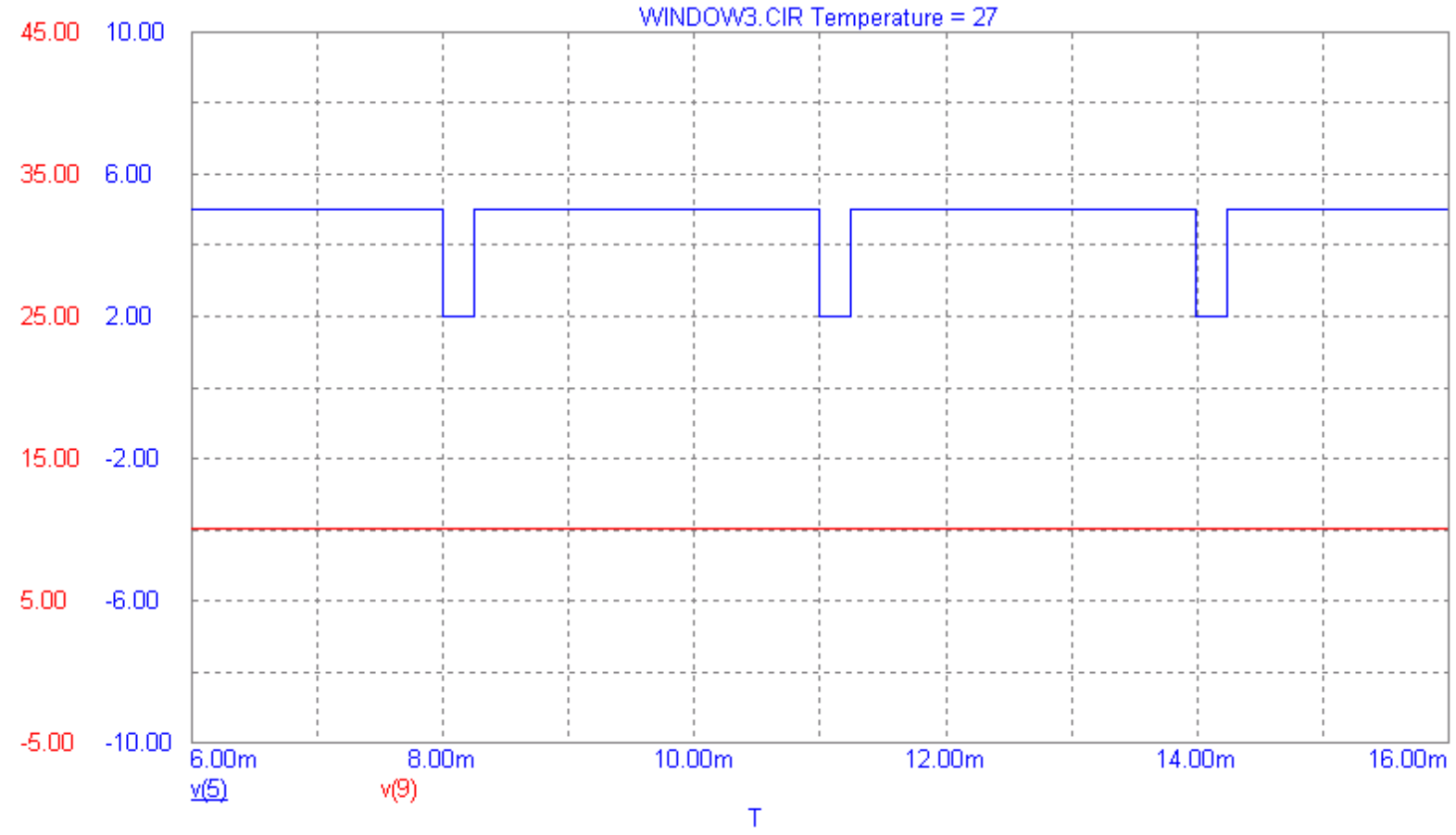
Simulator	File Name (5KHz sine wave)	Overshoot	Run Time
Measured Data	NA	1.8 Volt	NA
Micro-Cap V	Clmpmc	1.38 Volt	19.52 Sec
Pspice	Clmps	1.4 Volt	10.8 Sec
Ispice	clmpis	1.06 Volt	11.17 Sec

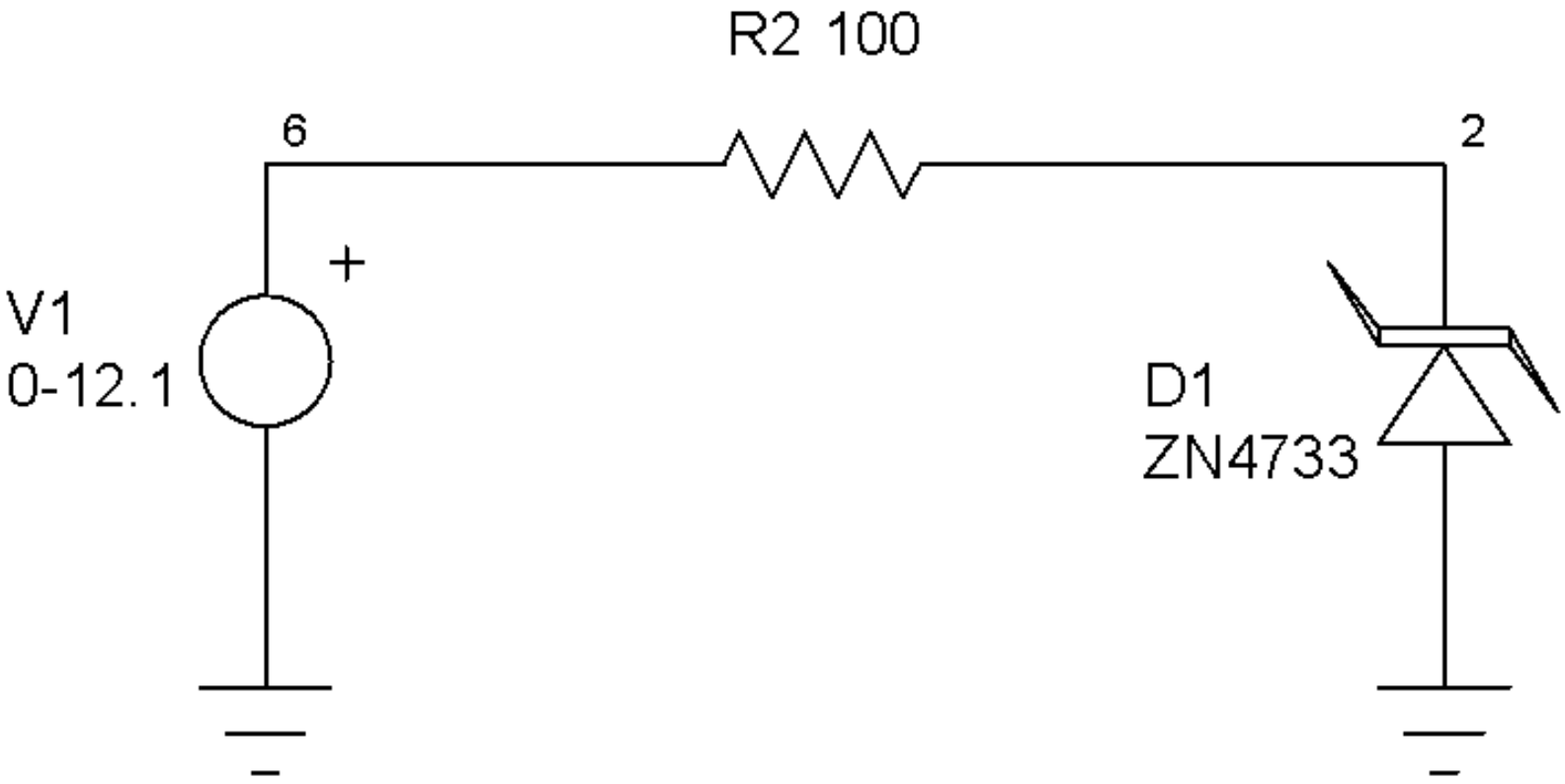

V(3)
VC
R1 100
7
3
D1
ZN4733
V1
10
R2
1K
34
V(10)
OUT2
R6
6.8K
10
V(2)
IN
R7 2.2K
X4
LM111T
VCC
VEE
4
R8 9.72K
R5 4.7K
6
Q1
QN2222A
2
V(3)
VC
X5
LM111T
VCC
VEE
1
R4 9.72K;10
5
R3
149.2K

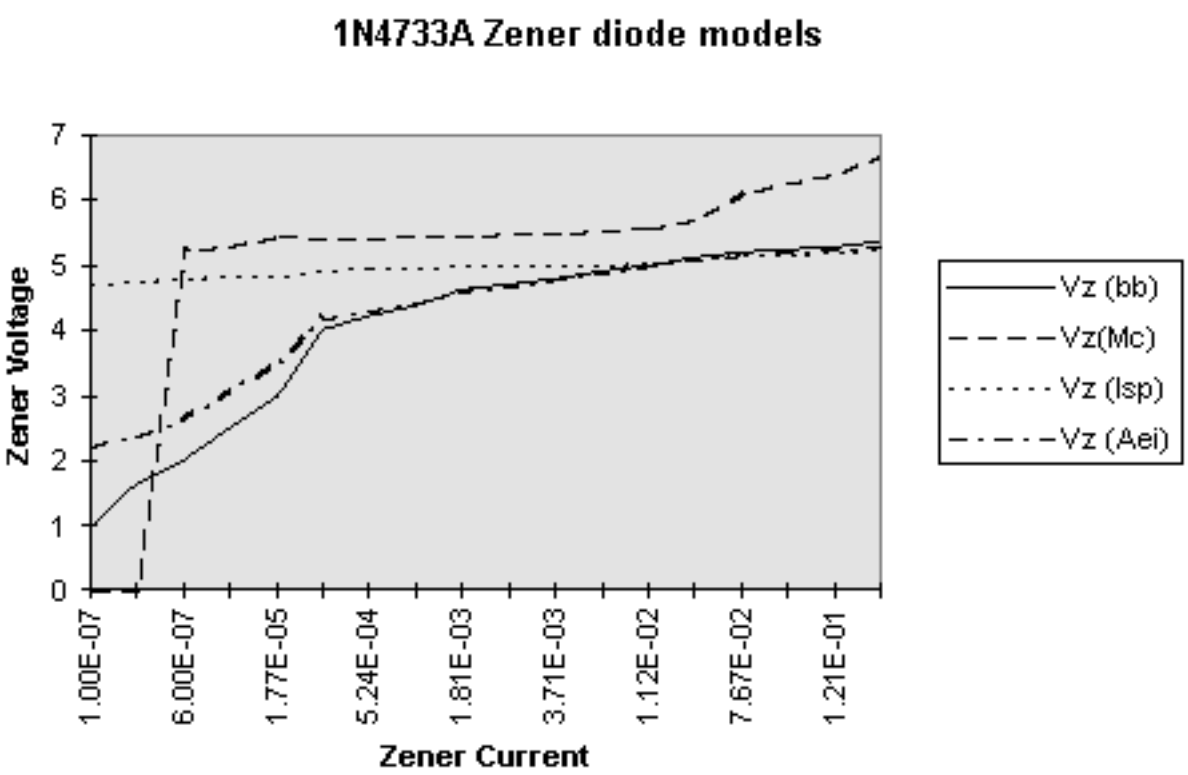


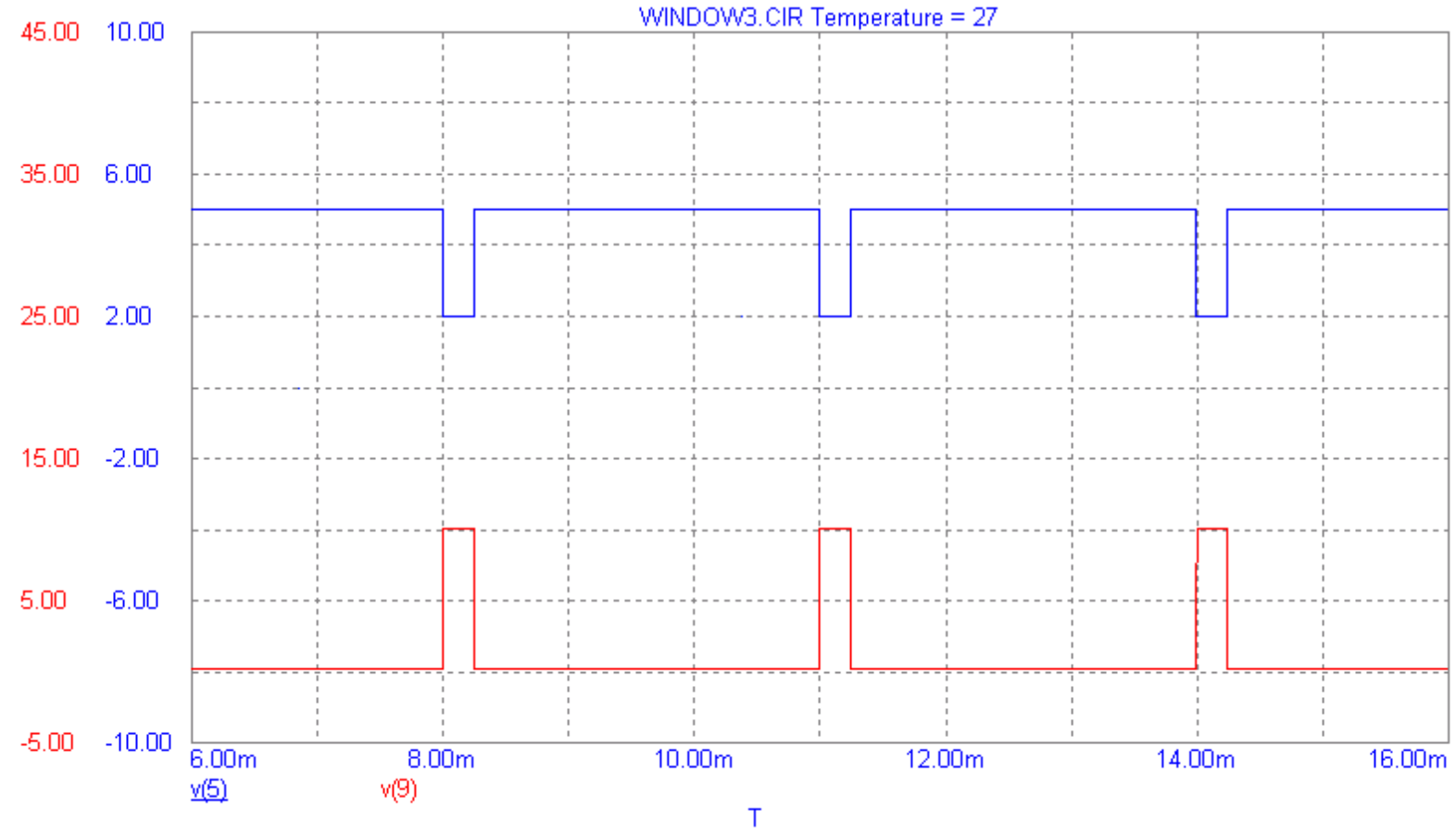

Tek Stop: 50kS/s
182 Acqs
T
2→
1→
Ch1 5 V Ch2 2 V M 1ms Ch2 ∫ 4.4 V
25 Feb 1998
10:15:57

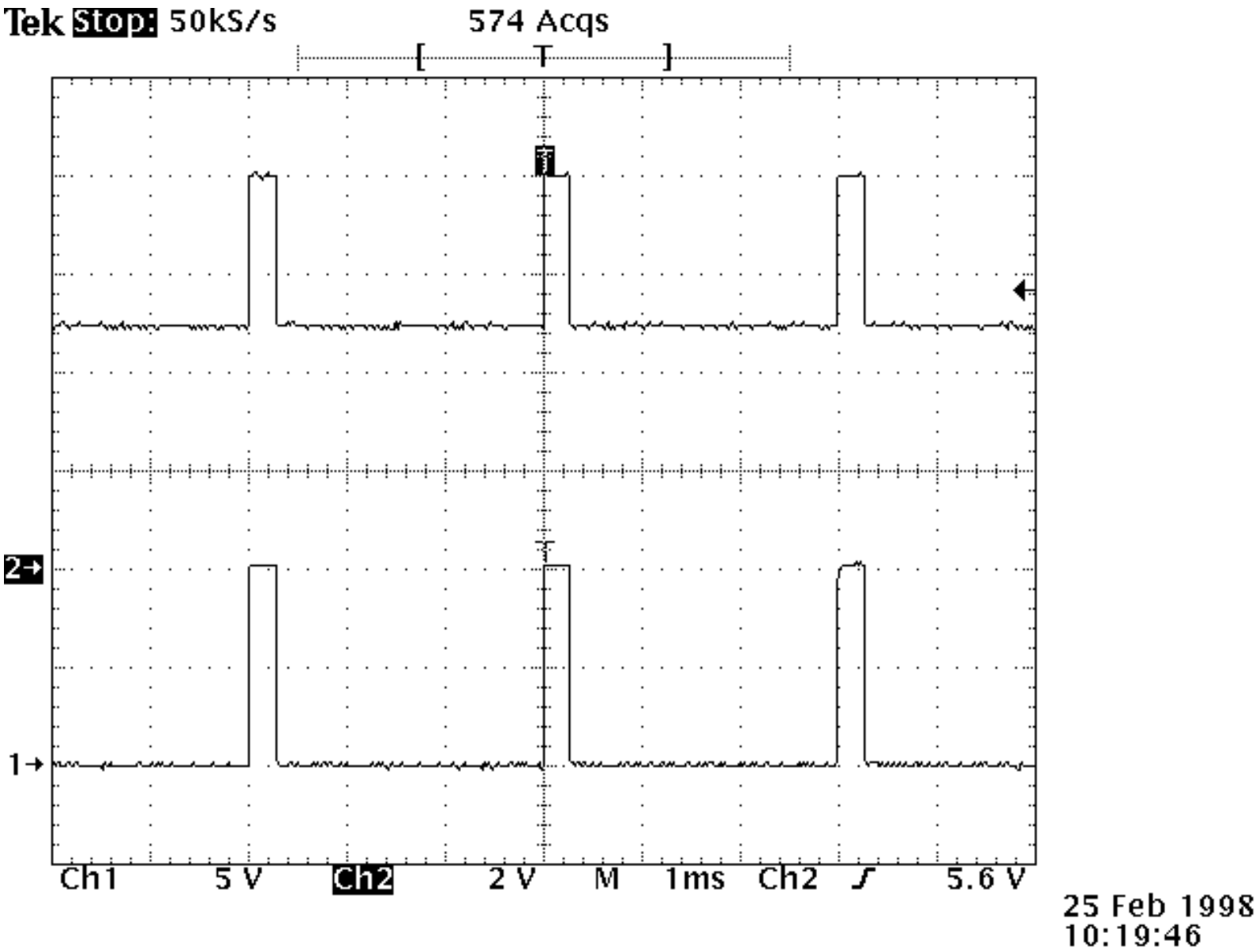

35.00
25.00
15.00
5.000
-5.000
OUT2 in Volts
8.000
4.000
0
-4.000
-8.000
IN in Volts
7.000M
9.000M
11.00M
13.00M
15.00M
TIME in Secs
1
2

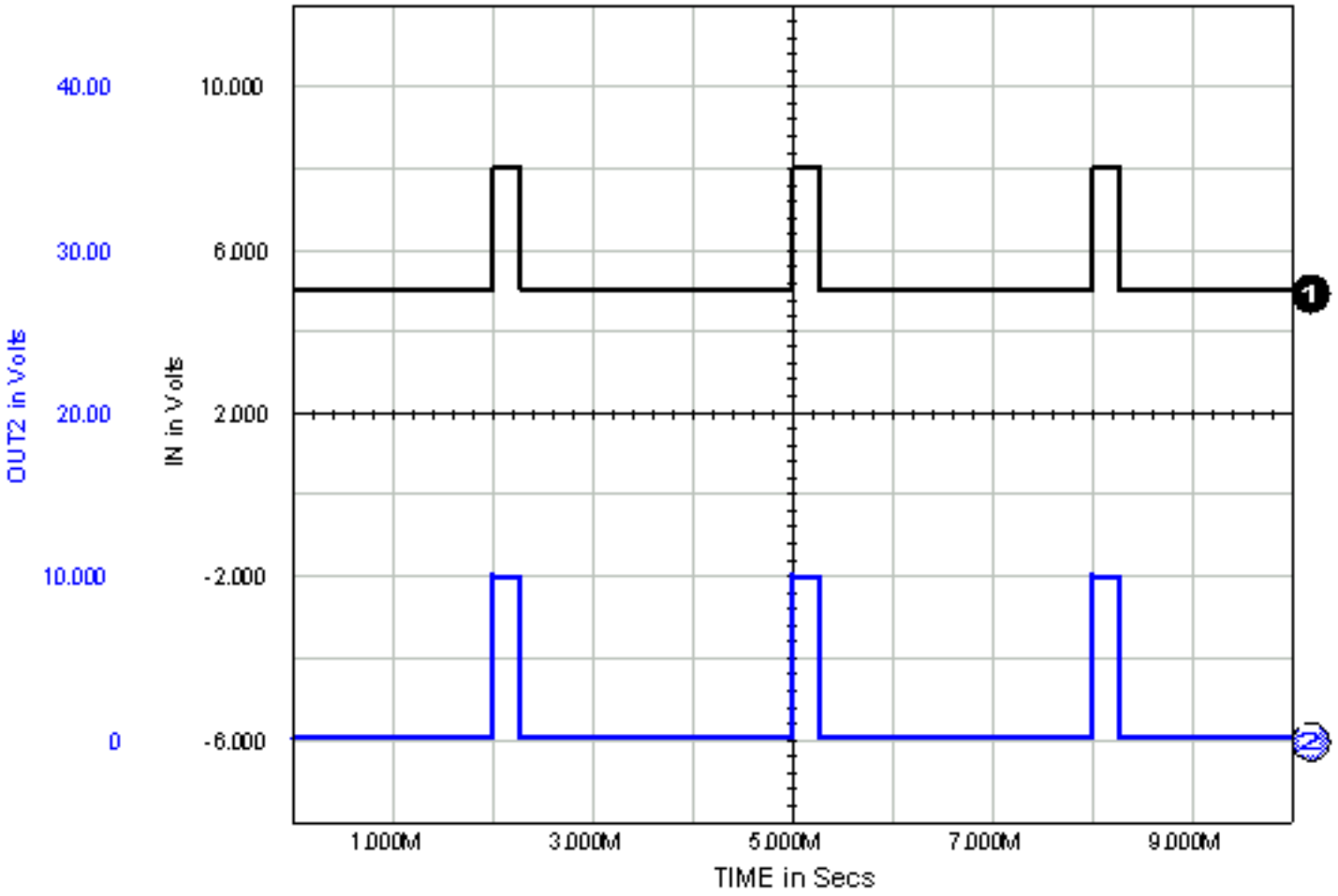

WINDOW3.CIR Temperature = 27
45.00
10.00
35.00
6.00
25.00
2.00
15.00
-2.00
5.00
-6.00
-5.00
-10.00
6.00m
8.00m
10.00m
12.00m
14.00m
16.00m
v(5)
v(9)
T

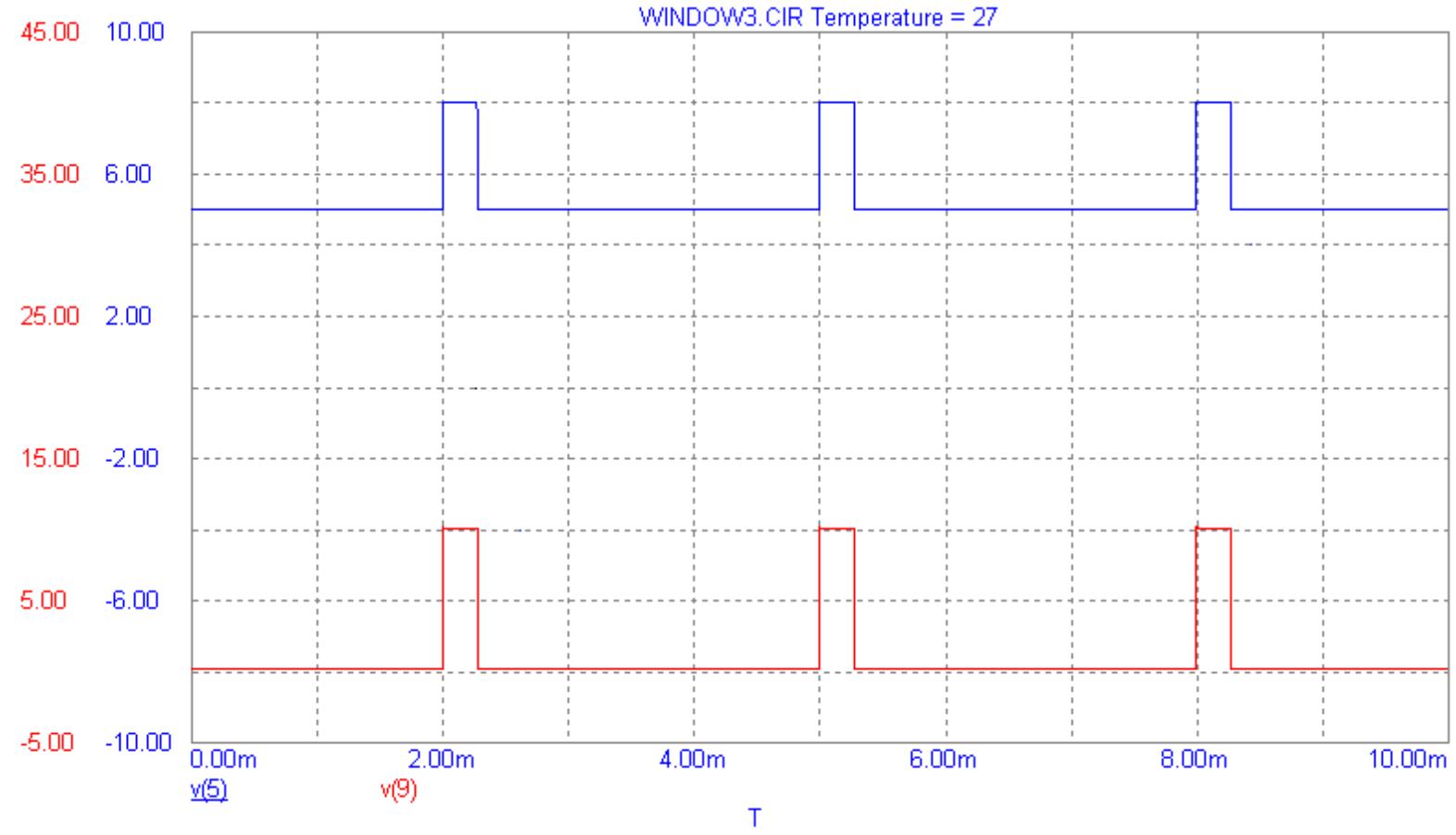

R2 100
6
2
+
V1
0-12.1
D1
ZN4733

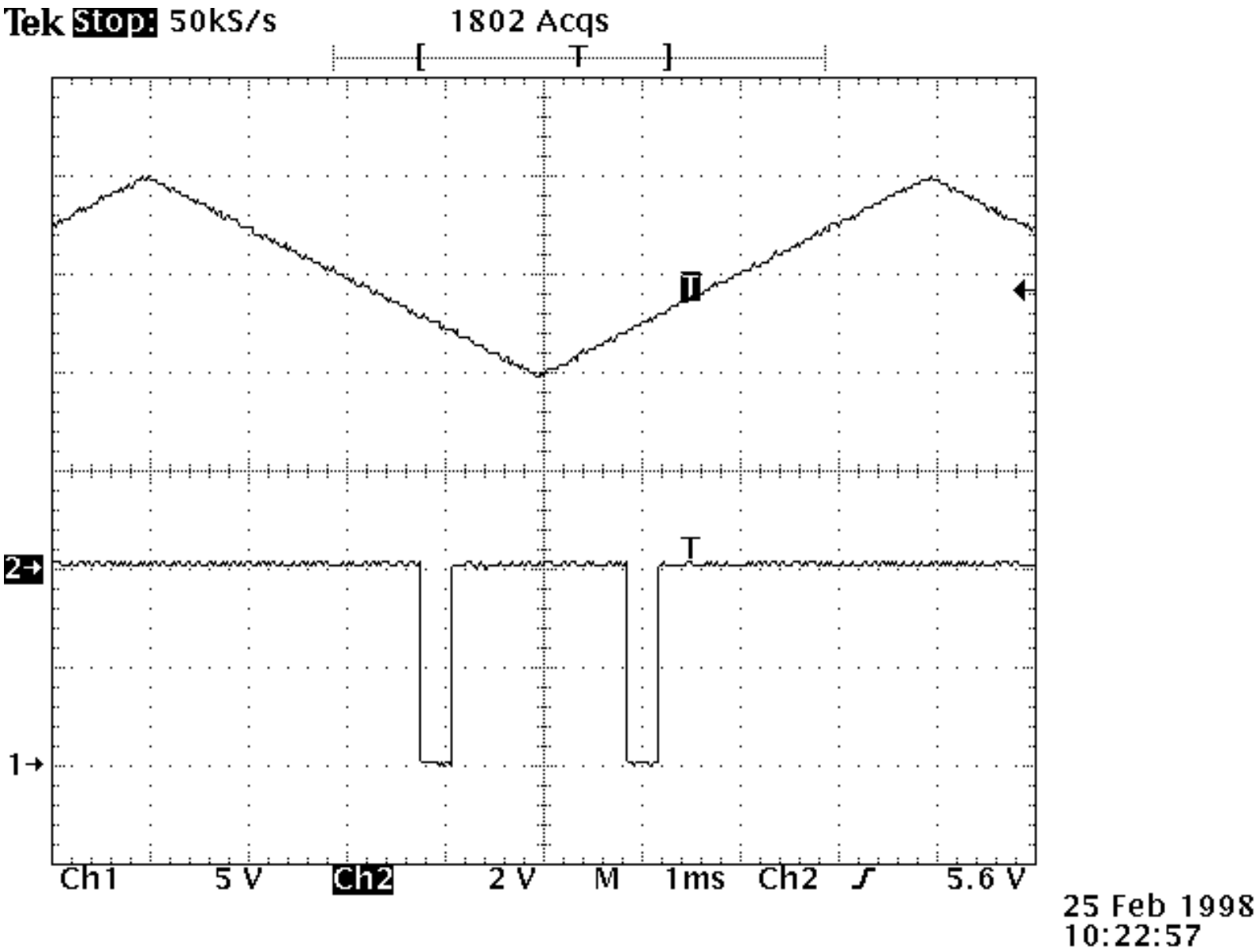

1N4733A Zener diode models
Zener Voltage
0
1
2
3
4
5
6
7
1.00E-07
6.00E-07
1.77E-05
5.24E-04
1.81E-03
3.71E-03
1.12E-02
7.67E-02
1.21E-01
Zener Current
Vz (bb)
Vz(Mc)
Vz (Isp)
Vz (Aei)

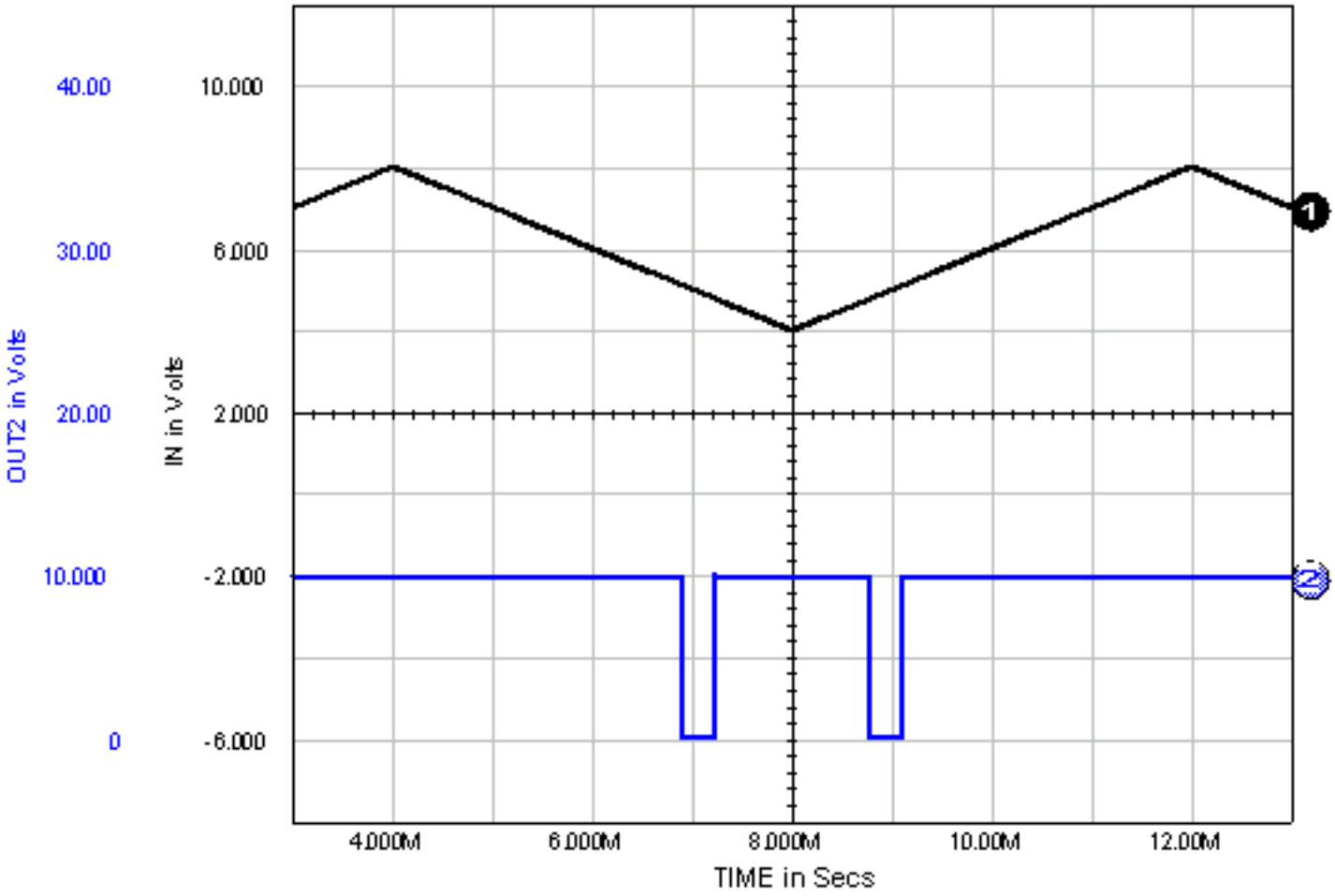

WINDOW3.CIR Temperature = 27
45.00
10.00
35.00
6.00
25.00
2.00
15.00
-2.00
5.00
-6.00
-5.00
-10.00
6.00m
8.00m
10.00m
12.00m
14.00m
16.00m
v(5)
v(9)
T

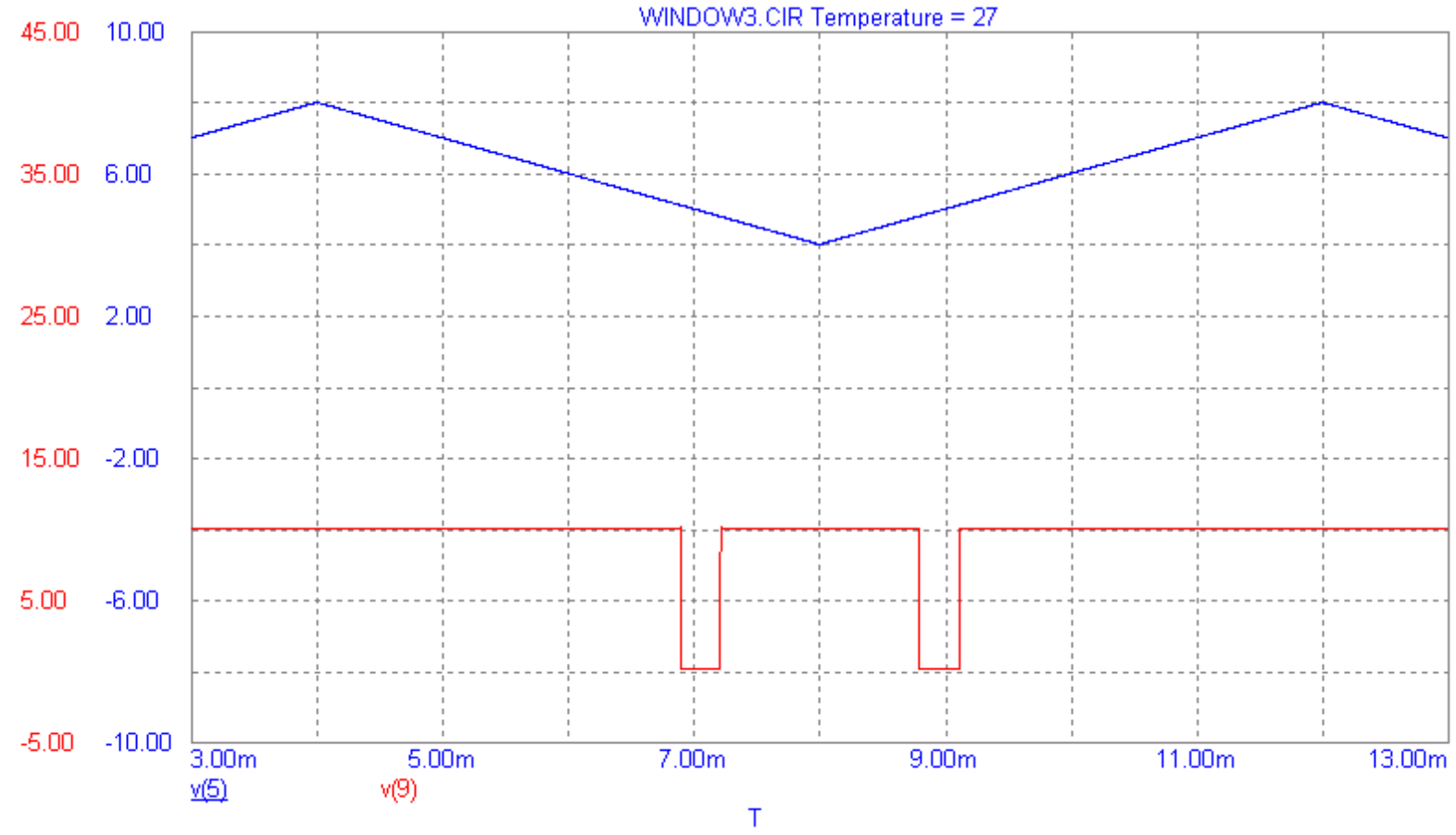

Tek Stop: 50kS/s
574 Acqs
2→
1→
Ch1 5 V Ch2 2 V M 1ms Ch2 ʃ 5.6 V
25 Feb 1998
10:19:46


40.00
30.00
20.00
10.000
0
OUT2 in Volts
10.000
6.000
2.000
-2.000
-6.000
IN in Volts
1
2
1.000M
3.000M
5.000M
7.000M
9.000M
TIME in Secs


WINDOW3.CIR Temperature = 27
45.00
10.00
35.00
6.00
25.00
2.00
15.00
-2.00
5.00
-6.00
-5.00
-10.00
0.00m
2.00m
4.00m
6.00m
8.00m
10.00m
v(5)
v(9)
T


Tek Stop: 50kS/s
1802 Acqs
2→
1→
Ch1 5 V Ch2 2 V M 1ms Ch2 ∫ 5.6 V
25 Feb 1998
10:22:57


40.00
30.00
20.00
10.000
0
OUT2 in Volts
10.000
6.000
2.000
-2.000
-6.000
IN in Volts
4.000M
6.000M
8.000M
10.00M
12.00M
TIME in Secs
1
2


WINDOW3.CIR Temperature = 27
45.00
10.00
35.00
6.00
25.00
2.00
15.00
-2.00
5.00
-6.00
-5.00
-10.00
3.00m
5.00m
7.00m
9.00m
11.00m
13.00m
v(5)
v(9)
T

#27 Resistance to Voltage

The basic element of an ohm meter is a circuit that can take a resistance and convert it into a voltage. This is most simply realized by using a circuit like the one shown in Figure 27-1. This circuit provide a linear increase in voltage for increasing resistance from 1 to 1K ohms. Using two or three know resistors, a conversion table between output voltage and resistance can be developed.

A simple modification to this circuit alters the range of resistance to be detected. Changing R3 alters the range of the resistance that can be detected by decreasing the rate of rise of the output voltage. This increases the range, but also decreases the accuracy of the ohm meter.

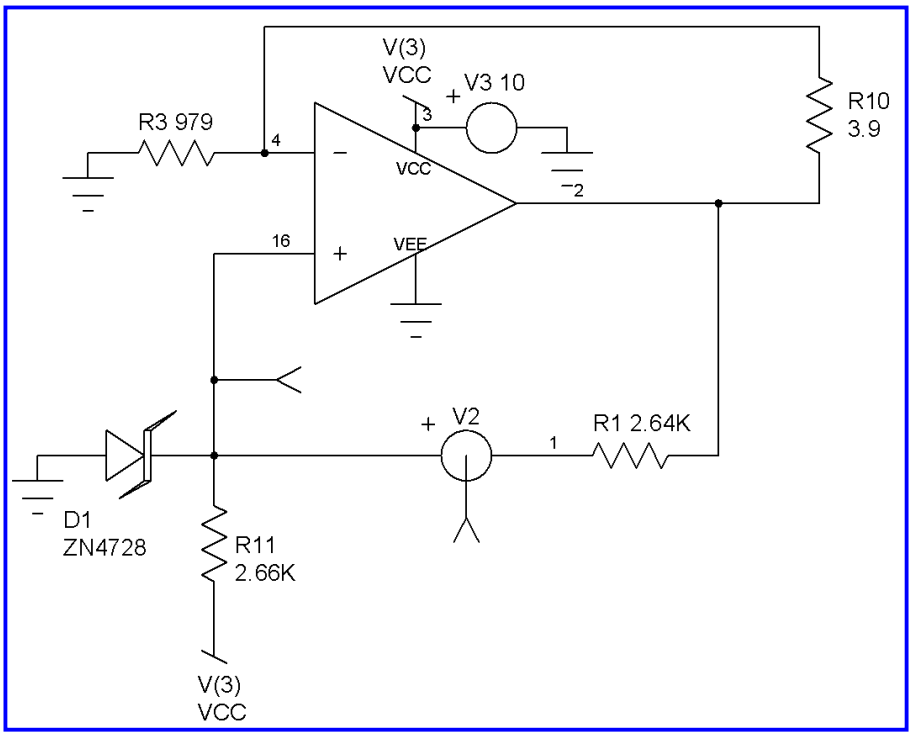


Figure 27-1: Simple resistance to voltage circuit

The zener diode used for this simulation is used in its "soft" region, which means that it is used below it recommended or test current. This region is often not defined in data books, and may not be correctly in some libraries. As an illustration of this point, the voltage across the zener diode was taken for all of the test situations. The results of these measurements are contained as Table

27-1.

1N4728 Soft Operation Zener Voltage Comparison				
Conditions	Measured Zener Voltage			
OHMs Tested	IsSpice	Pspice	Microcap	Measured Data
3.9	3.165	3.3	3.009	2.18
72.5	3.166	3.3	3.01	2.19
179	3.167	3.3	3.013	2.19
379	3.17	3.3	3.017	2.21
808	3.174	3.3	3.026	2.24

Table 27-1: Soft Zener Voltage Comparison

The evaluation version of Pspice did not have a similar zener diode in its library so a 3.3 voltage source is used in the place of the zener. This assumes that the zener is used at its test current which biases the evaluation version of Pspice results, however if asked to build this circuit using only the models that were contained in Pspice, this would be a natural assumption to make.

The output voltage used to determine the resistance will be measure across R1. This positions the curve so multiplying the output voltage by a scaler results in the resistance being measured. Using the voltage across R1 for our output does not correct the error caused by the incorrect zener voltage in the soft region. The results of the simulation and the measured data are shown as Figure 27-2.

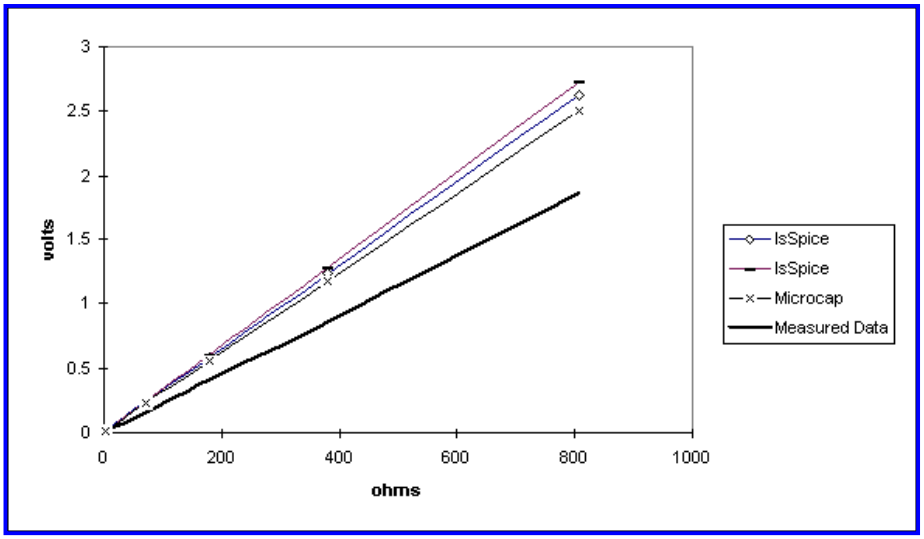


Figure 27-2: Resistance to Volts response using "Soft" zener

These results show that all three of the spice simulators were not equipped to handle simulations of this particular zener diode in its soft region. However, zener diodes are not well defined or tested in this region of operation, so it may just be that the circuit I tested had worst then average zener diode used in it. To further explore this problem, the experiment was modified to put more current then the specified test current in the zener diode. The circuit with these modifications made is shown in Figure 27-3. The measurements across the zener diode are shown in Table 27-2, and the results of the resistance to volts response are contained in Figure 27-4.

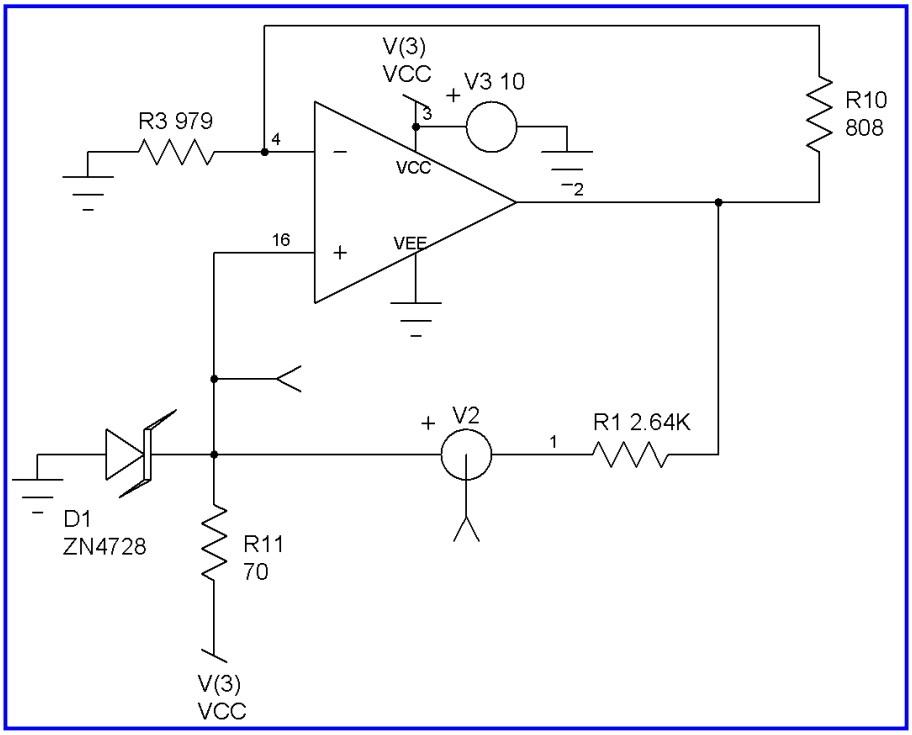


Figure 27-3: Resistance to voltage converter using "Hard" Zener

3.3 volt zener voltage				
Conditions	Measured Zener Voltage			
OHMs	IsSpice	Pspice	Microcap	Measured Data
3.9	3.32	3.3	3.939	3.41
72.5	3.32	3.3	3.94	3.4
179	3.32	3.3	3.941	3.41
379	3.32	3.3	3.944	3.41
808	3.321	3.3	3.95	3.41

Table 27-2: "Hard" Zener voltage comparison

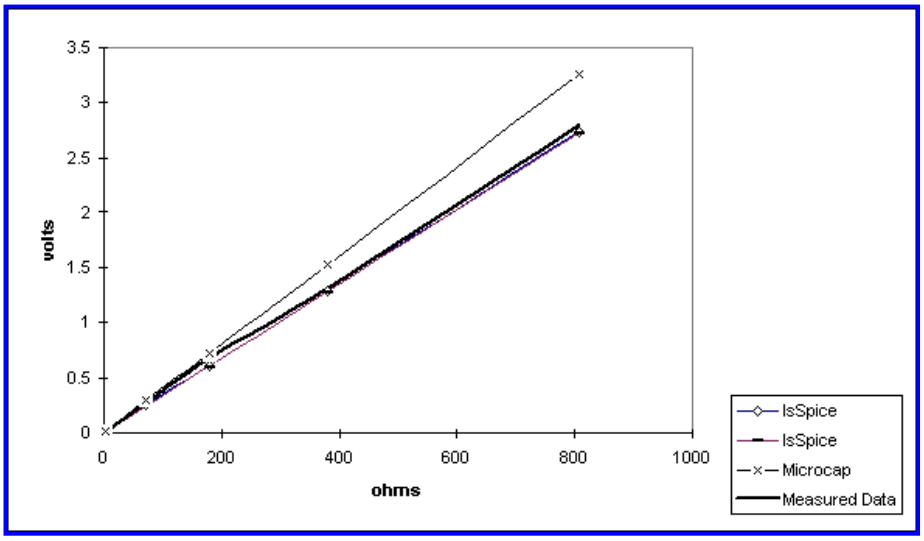


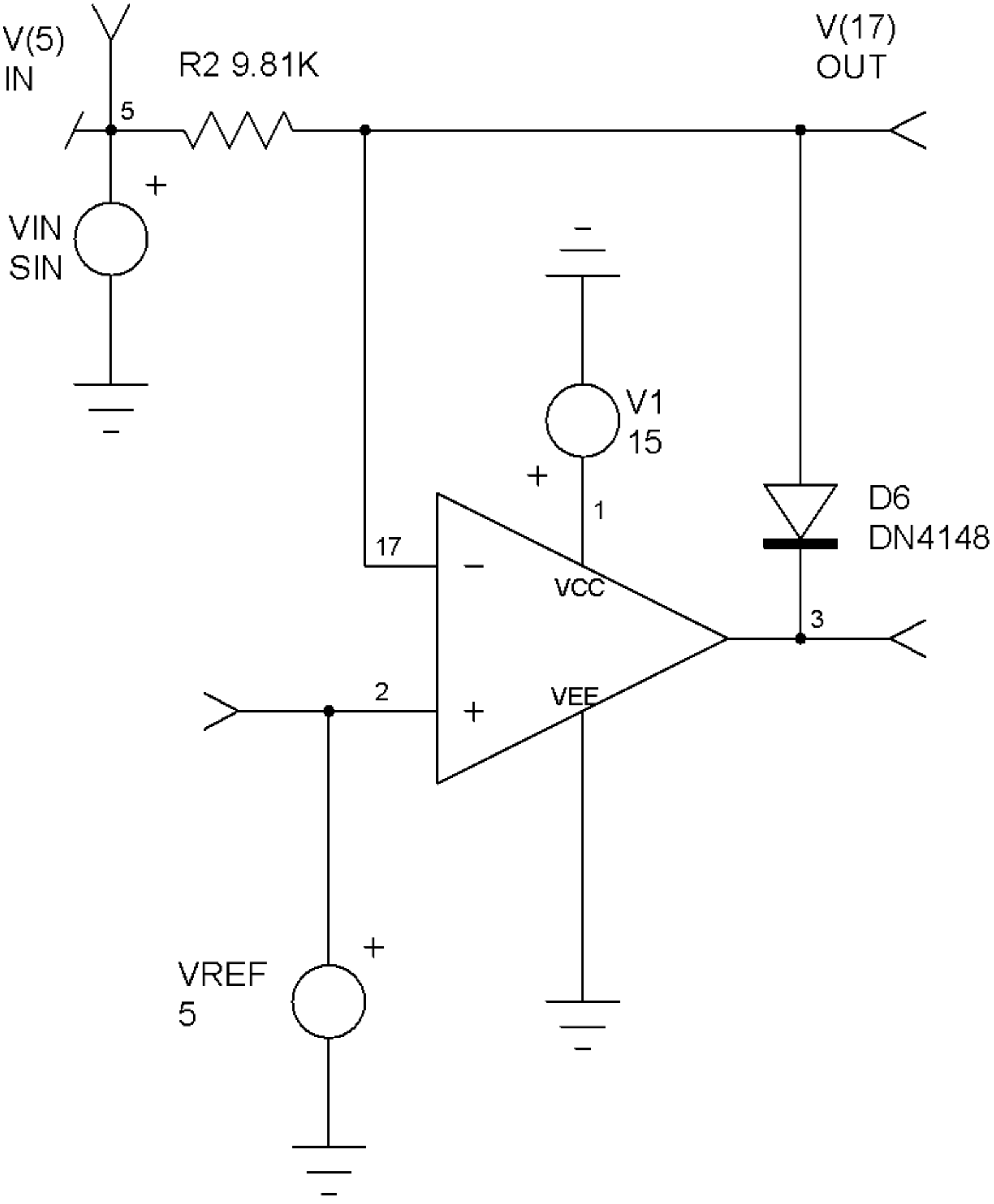
Figure 27-4: Resistance to Volts using "Hard" zener

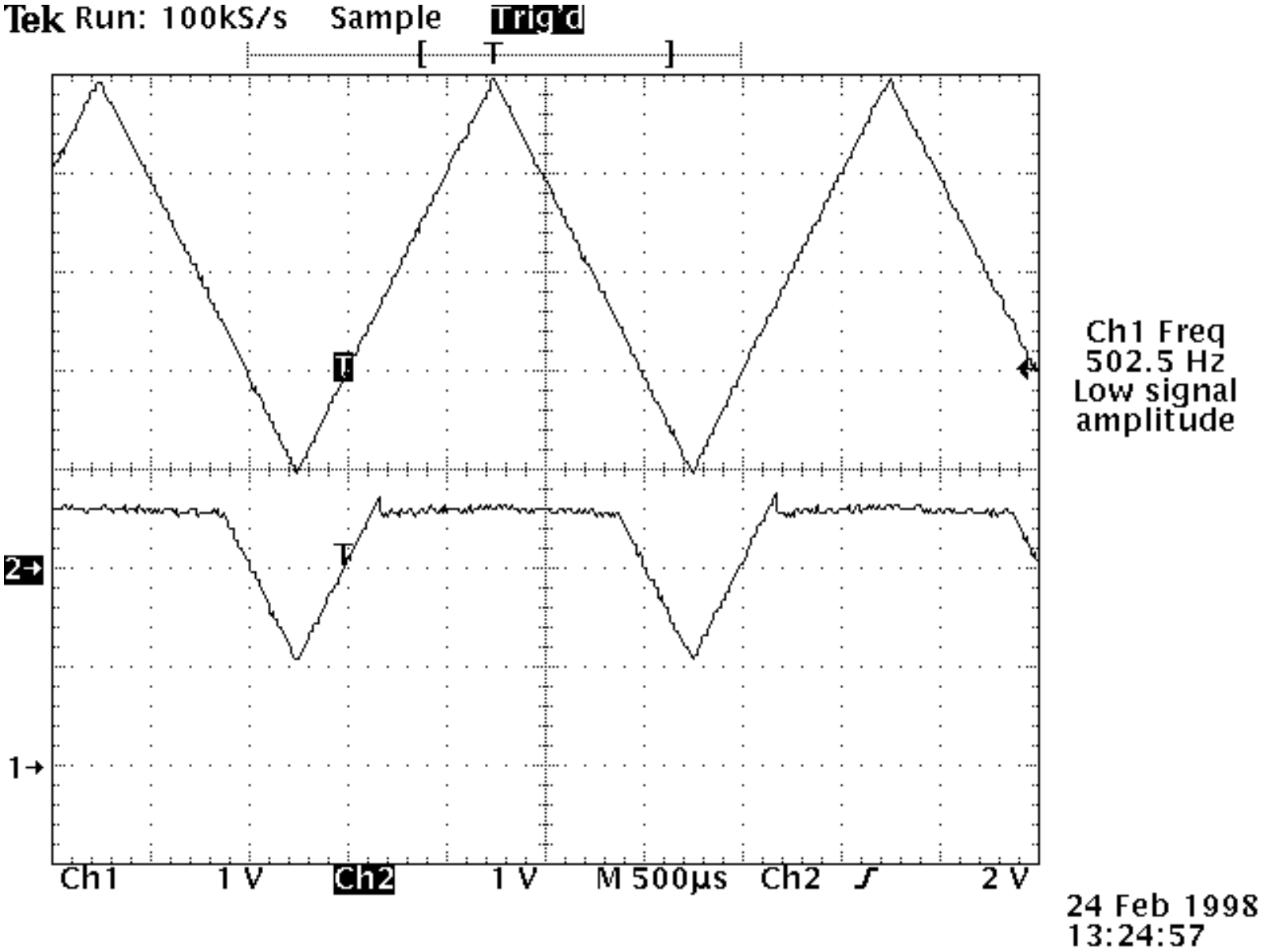
The 1N4728 has a test current of 78 mA, for the "Hard" case 98 mA were used

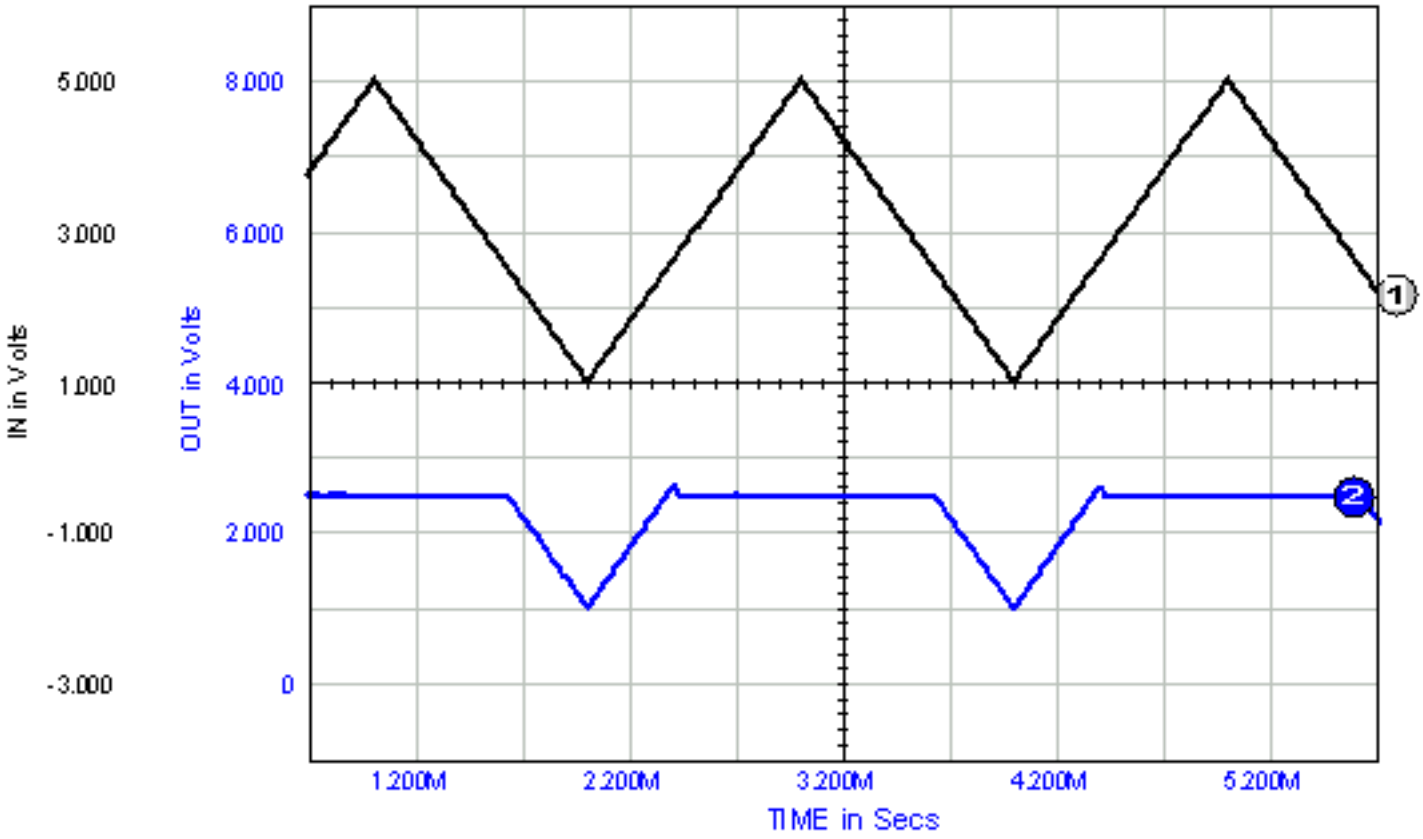
to drive it. For the soft case, the zener current was only about 3 mA. Using such a wide operating range for a zener diode invites the flaws of the models to show up. If we only looked at the operating point of the zener, nearly all of the zener models are likely to be correct. It is important to note that zener diodes can be modeled, but unless you have compared the response of a zener model to hardware, be careful whether you believe the modeled response.

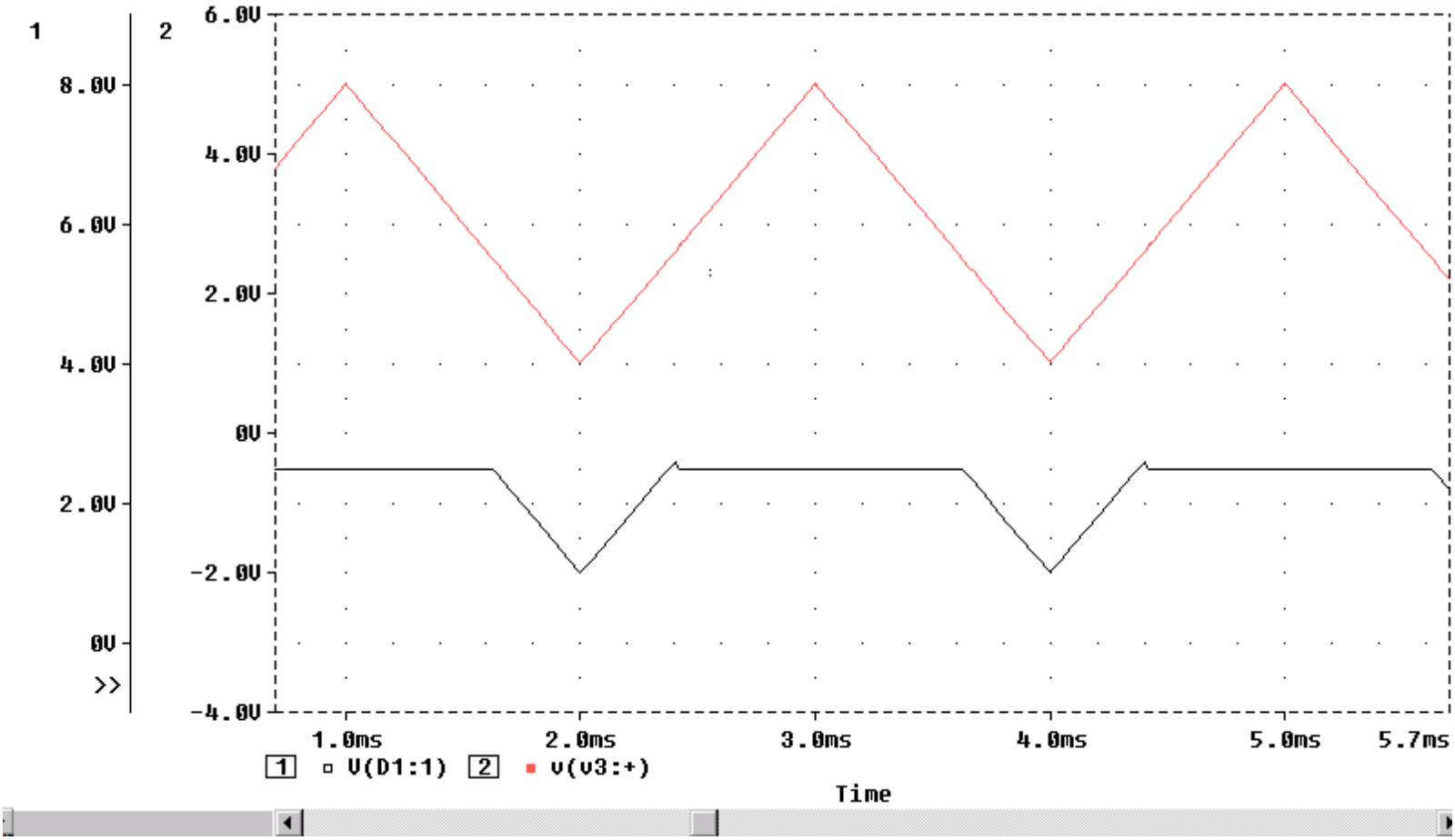
Run Time Summary		
IsSpice v 7.6	PsPice v 6.3	Micro-Cap V v2
Negligable	Negligable	Negligable
Advantages: Low parts count, adjustable range		
Disadvantages: Small range, enlarging range decreases resolution		

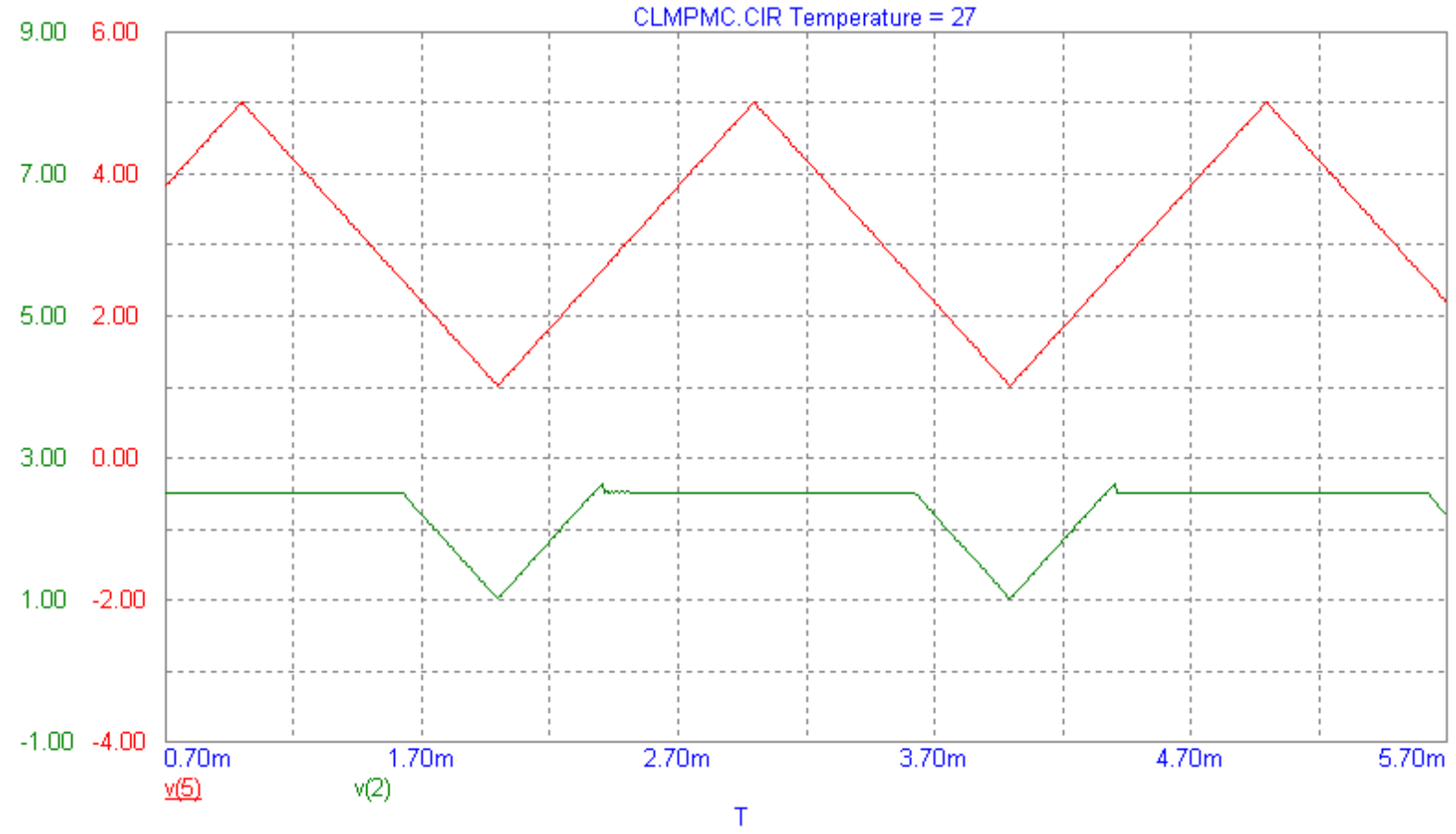
Filenames: ohm_met (IsSpice), ps_ohm (Pspice), mic_ohm (Micro-Cap V)

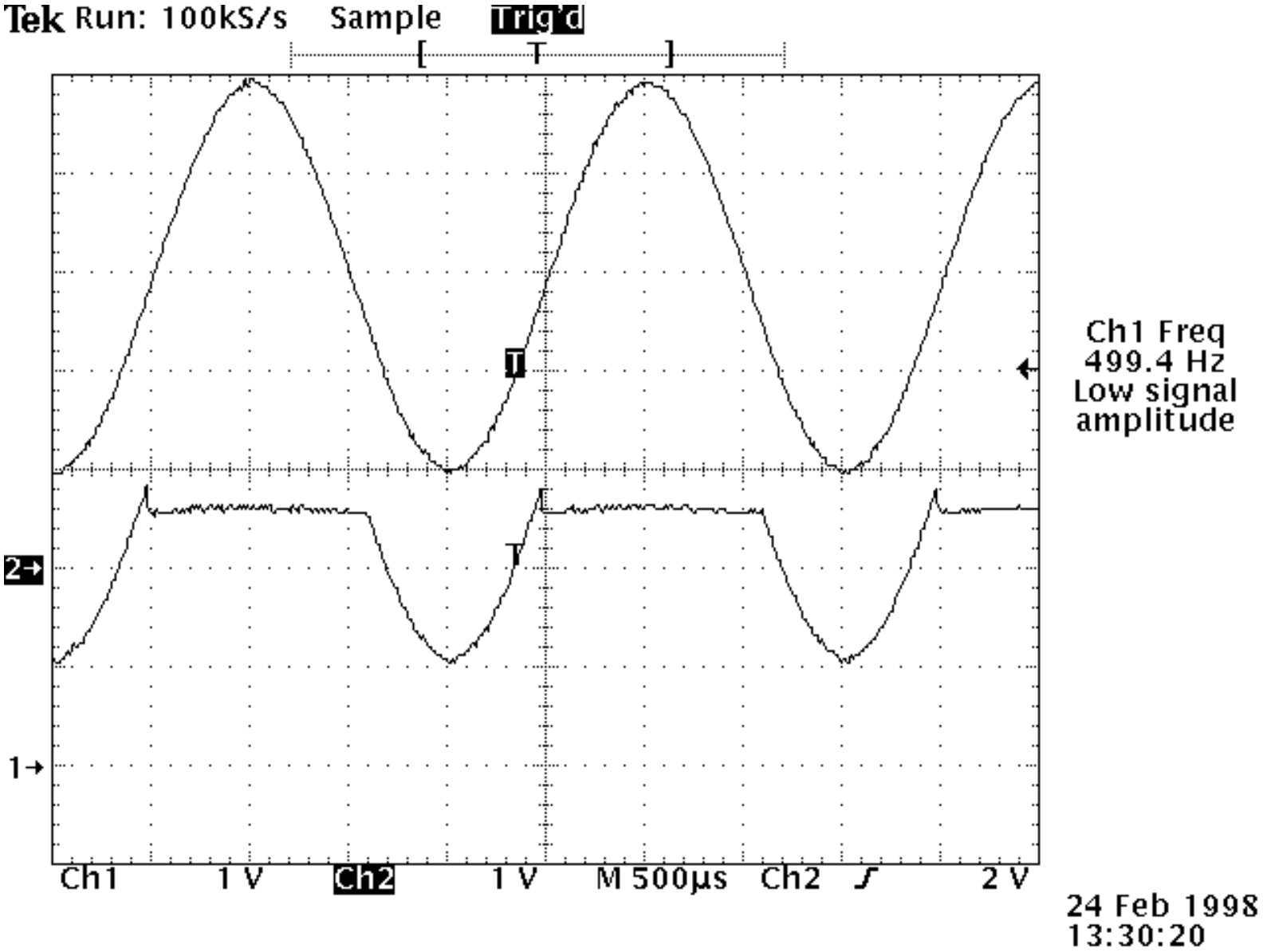

V(5)
IN
R2 9.81K
V(17)
OUT
5
+
VIN
SIN
–
–
V1
15
+
1
D6
DN4148
17
–
VCC
3
2
+
VEE
+
VREF
5
–
–

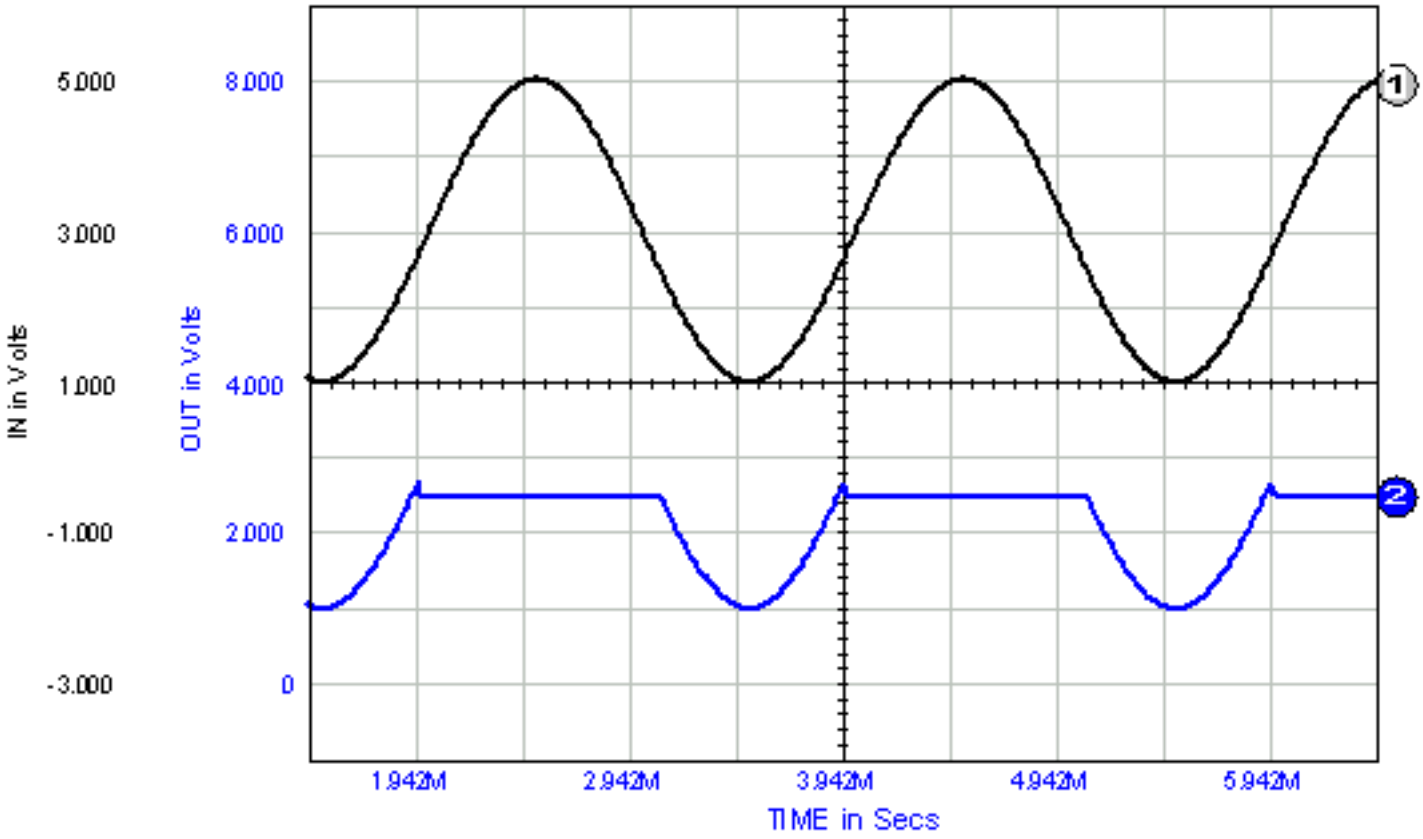

Tek Run: 100kS/s Sample Trig'd
Ch1 Freq
502.5 Hz
Low signal
amplitude
2→
1→
Ch1 1 V Ch2 1 V M 500µs Ch2 ∫ 2 V
24 Feb 1998
13:24:57

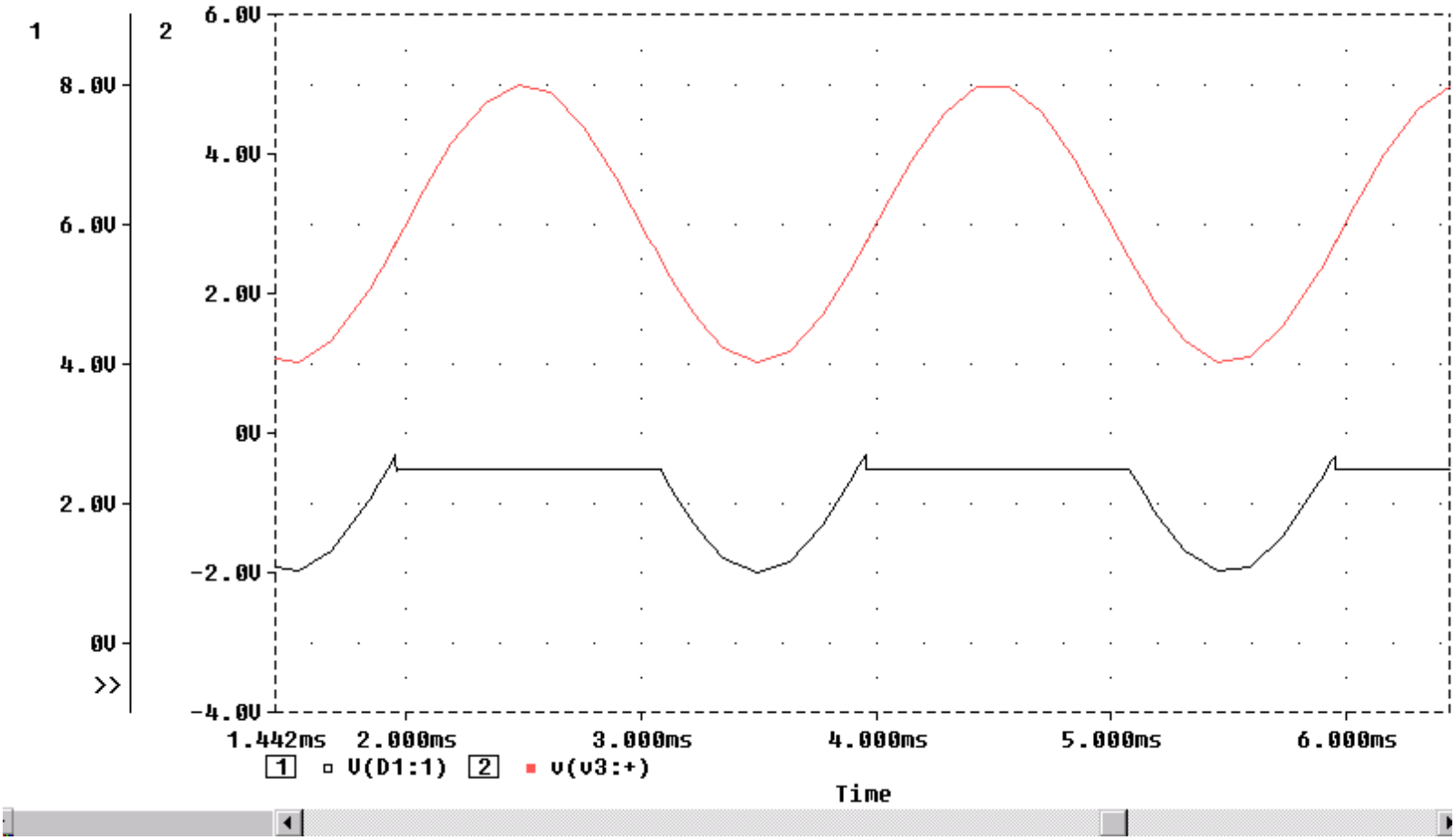

5.000
3.000
1.000
-1.000
-3.000
IN in Volts
8.000
6.000
4.000
2.000
0
OUT in Volts
1.200M
2.200M
3.200M
4.200M
5.200M
TIME in Secs
1
2

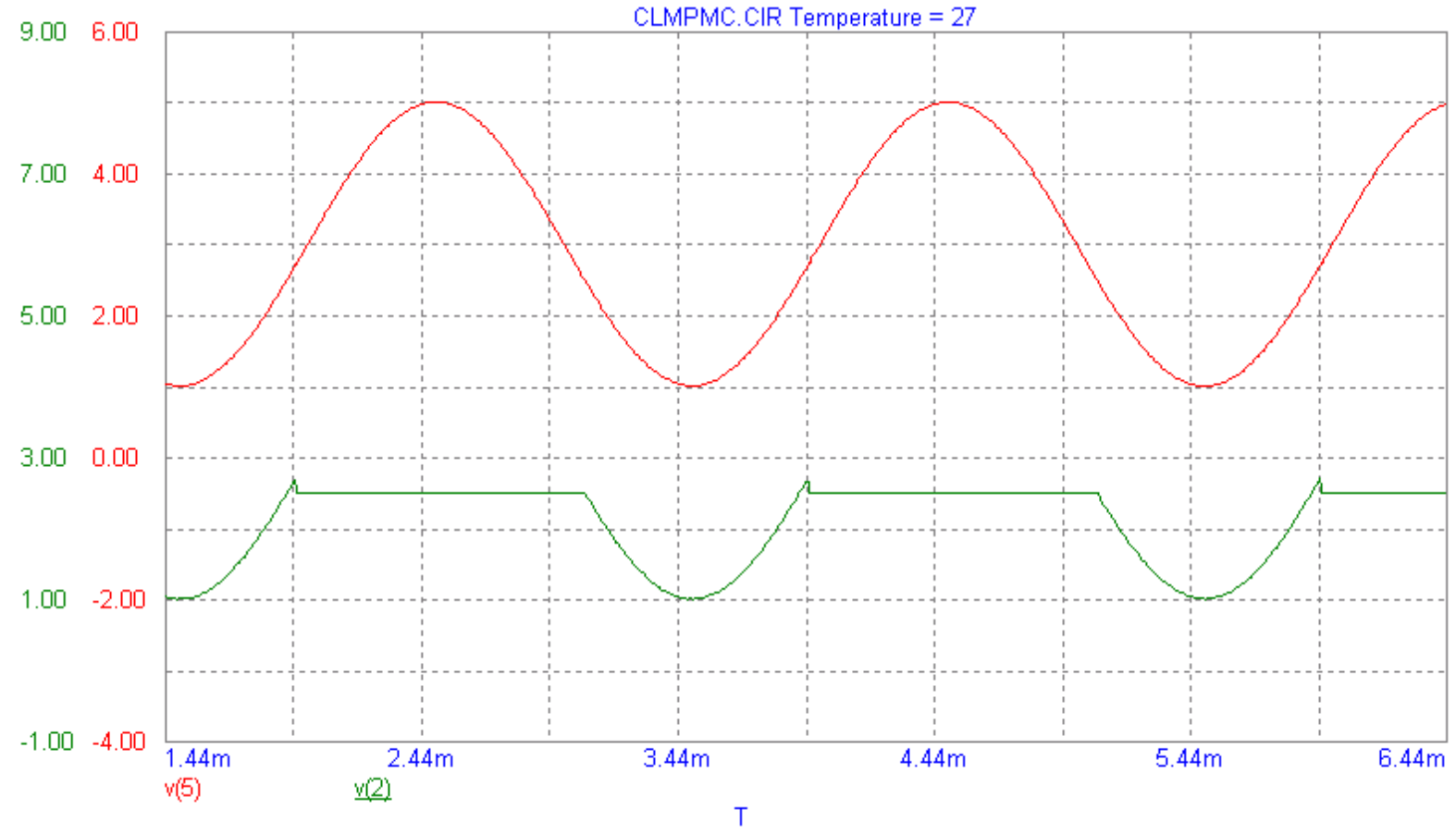

1
2
8.0V
6.0V
4.0V
2.0V
0V
>>
6.0V
4.0V
2.0V
0V
-2.0V
-4.0V
1.0ms
2.0ms
3.0ms
4.0ms
5.0ms
5.7ms
1 V(D1:1) 2 v(v3:+)
Time

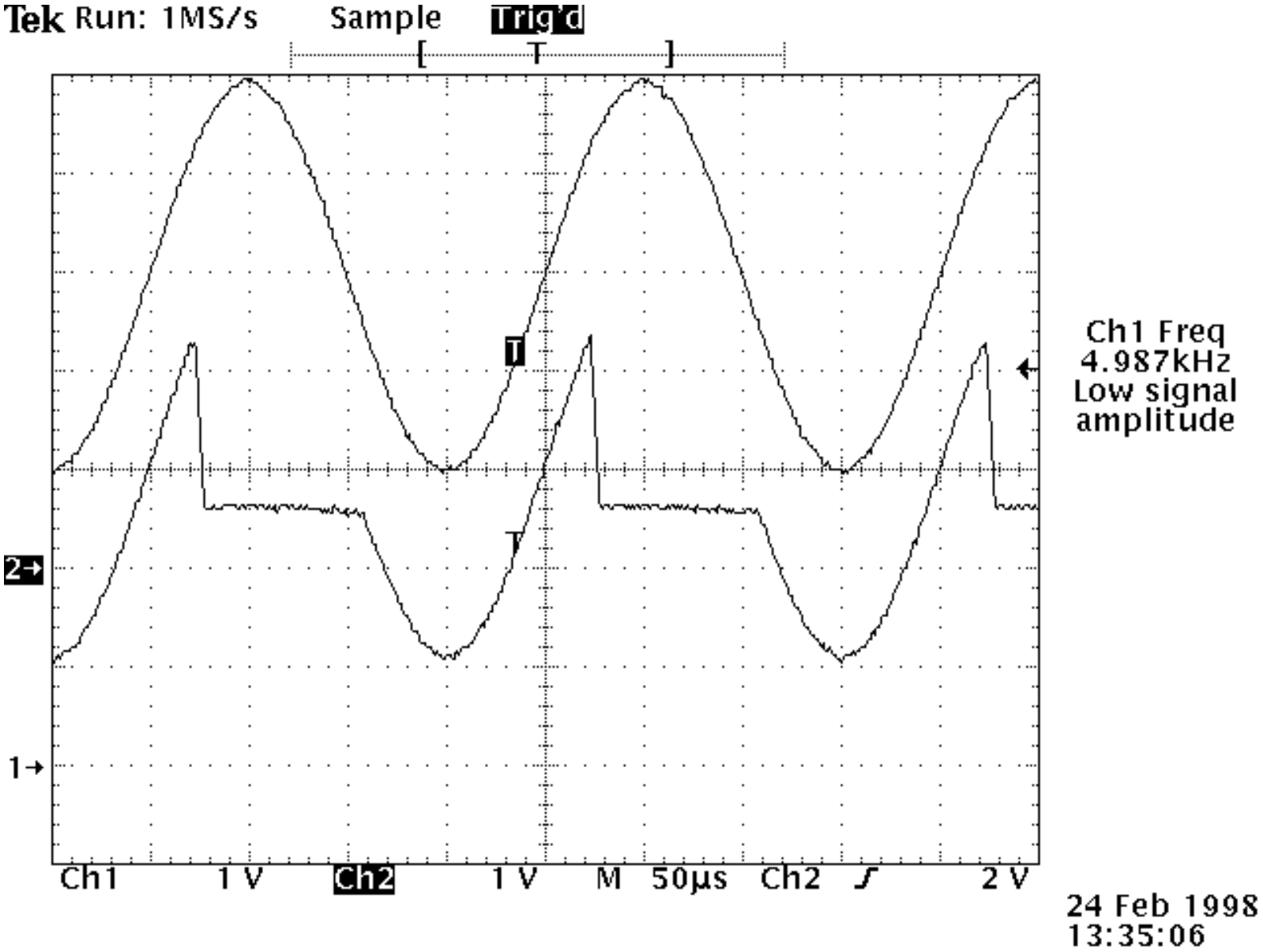

CLMPMC.CIR Temperature = 27
9.00
6.00
7.00
4.00
5.00
2.00
3.00
0.00
1.00
-2.00
-1.00
-4.00
0.70m
1.70m
2.70m
3.70m
4.70m
5.70m
v(5)
v(2)
T

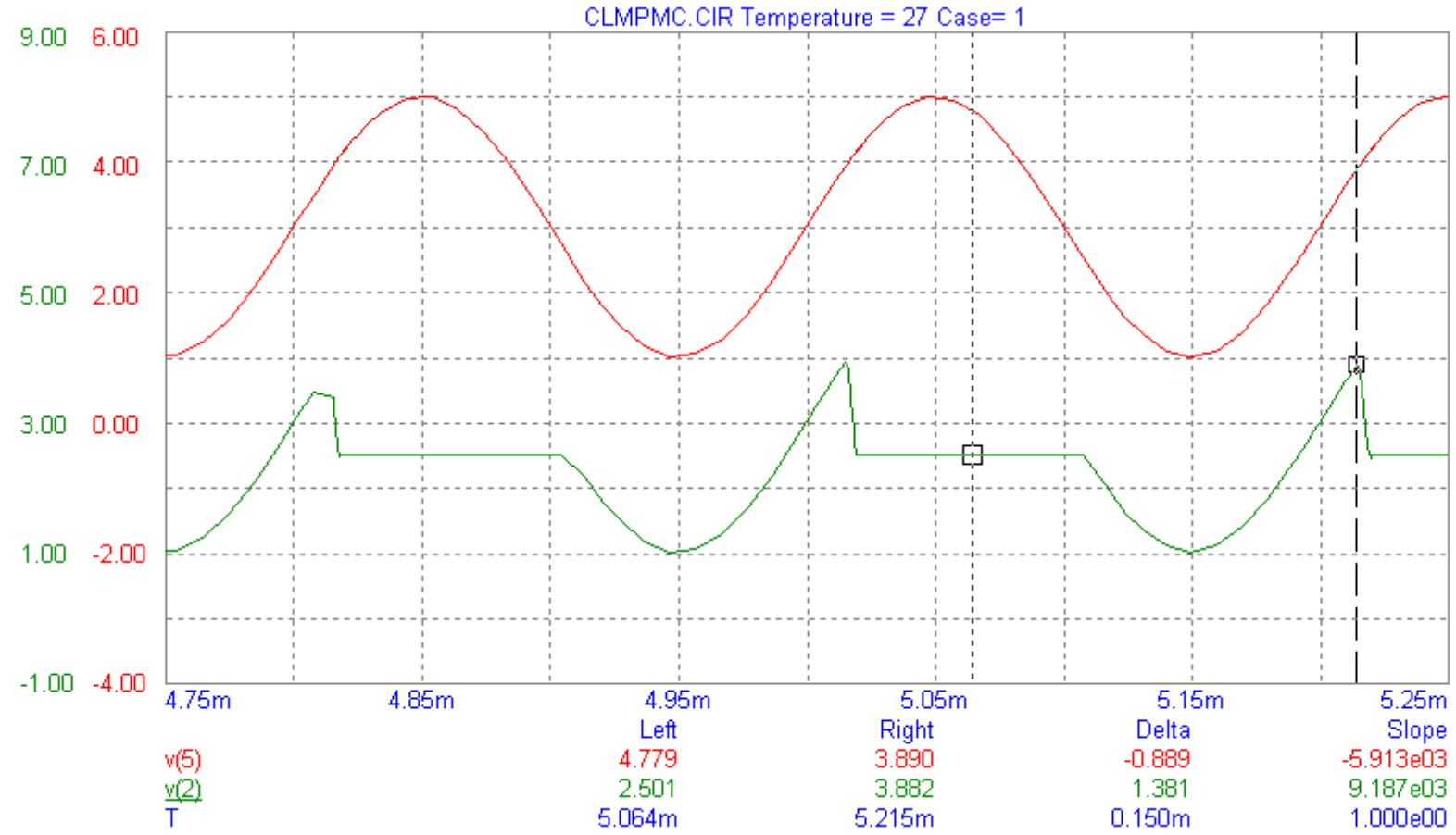

Tek Run: 100kS/s Sample Trig'd
Ch1 Freq
499.4 Hz
Low signal
amplitude
2→
1→
Ch1 1 V Ch2 1 V M 500µs Ch2 ∫ 2 V
24 Feb 1998
13:30:20

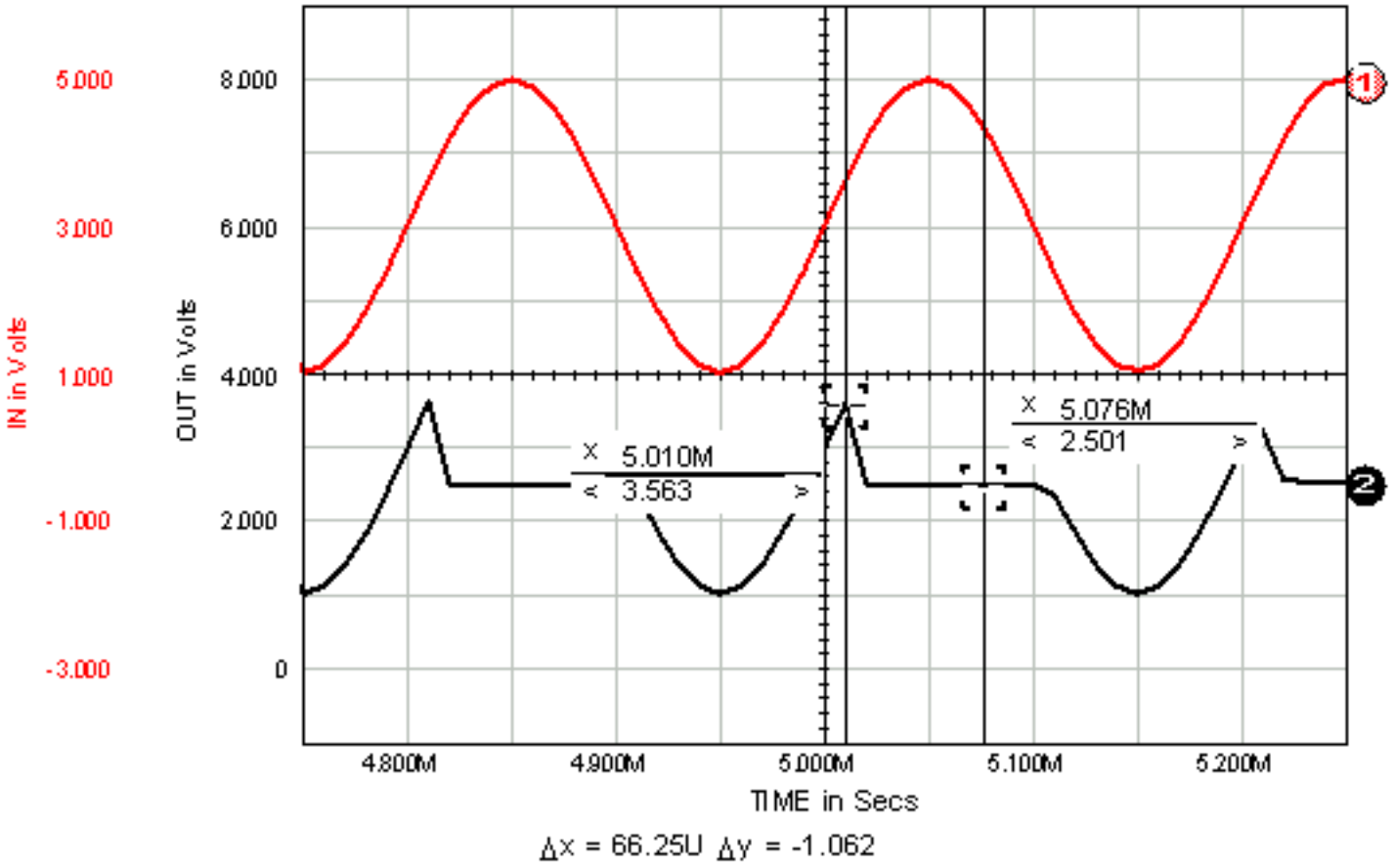

5.000
3.000
1.000
-1.000
-3.000
IN in Volts
8.000
6.000
4.000
2.000
0
OUT in Volts
1.942M
2.942M
3.942M
4.942M
5.942M
TIME in Secs
1
2

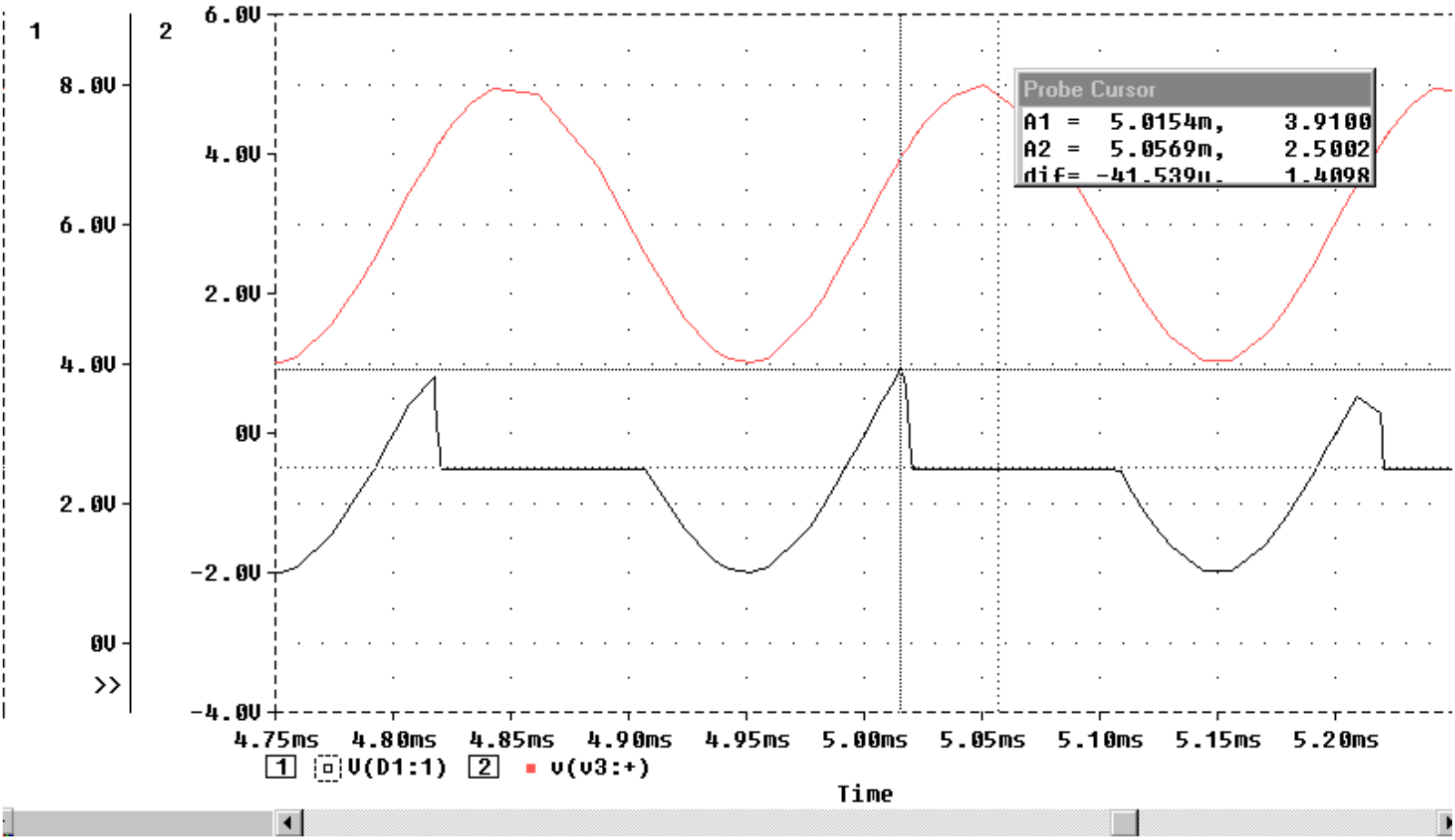

1
2
8.0V
6.0V
4.0V
2.0V
0V
>>
6.0V
4.0V
2.0V
0V
-2.0V
-4.0V
1.442ms
2.000ms
3.000ms
4.000ms
5.000ms
6.000ms
1 V(D1:1) 2 v(v3:+)
Time

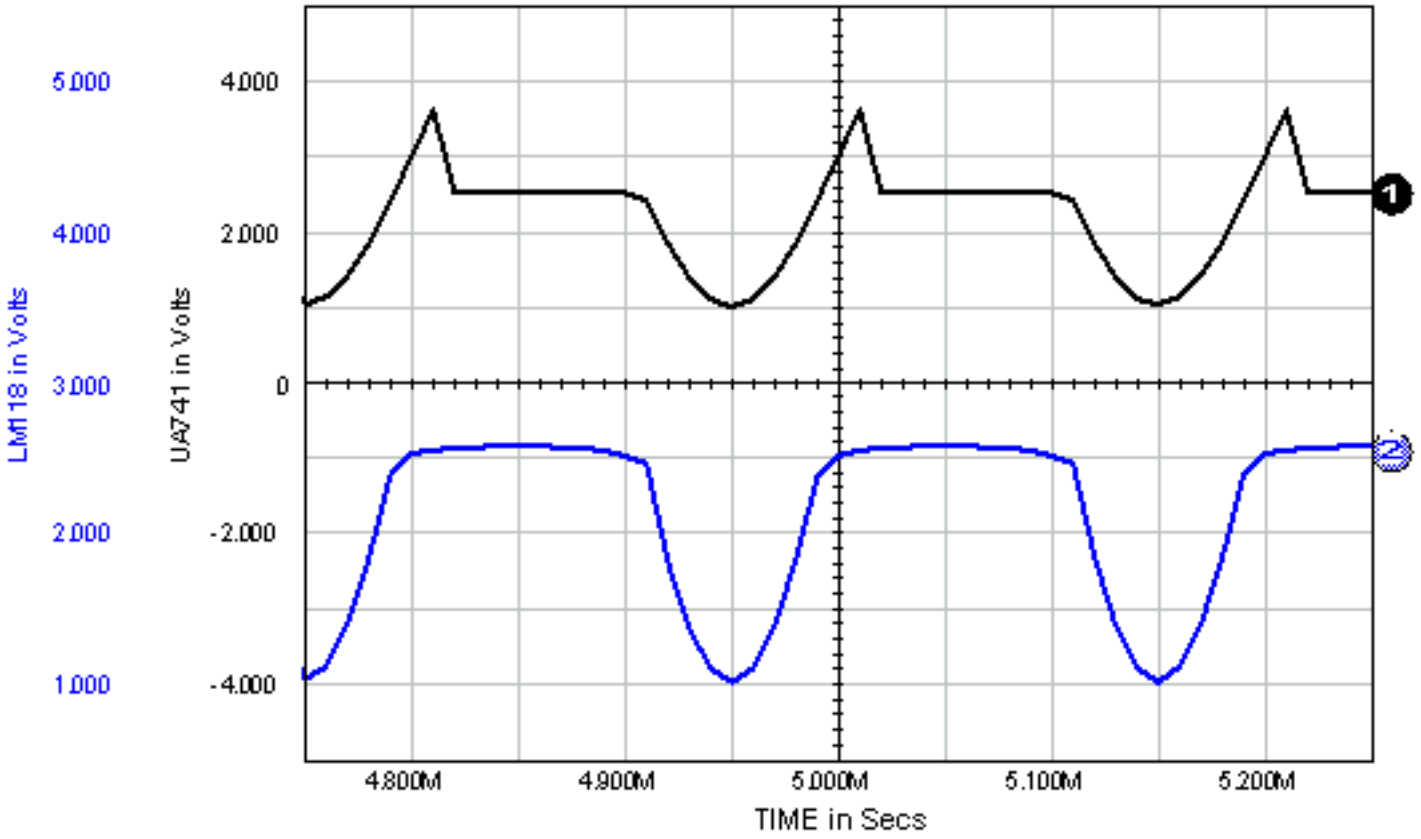

CLMPMC.CIR Temperature = 27
9.00
6.00
7.00
4.00
5.00
2.00
3.00
0.00
1.00
-2.00
-1.00
-4.00
1.44m
2.44m
3.44m
4.44m
5.44m
6.44m
v(5)
v(2)
T


Tek Run: 1MS/s Sample Trig'd
Ch1 Freq
4.987kHz
Low signal
amplitude
2→
1→
Ch1 1 V Ch2 1 V M 50µs Ch2 ∫ 2 V
24 Feb 1998
13:35:06


CLMPMC.CIR Temperature = 27 Case= 1
9.00
6.00
7.00
4.00
5.00
2.00
3.00
0.00
1.00
-2.00
-1.00
-4.00
4.75m
4.85m
4.95m
5.05m
5.15m
5.25m
Left
Right
Delta
Slope
v(5)
4.779
3.890
-0.889
-5.913e03
v(2)
2.501
3.882
1.381
9.187e03
T
5.064m
5.215m
0.150m
1.000e00


5.000
3.000
1.000
-1.000
-3.000
IN in Volts
8.000
6.000
4.000
2.000
0
OUT in Volts
X 5.010M
< 3.563 >
X 5.076M
< 2.501 >
1
2
4.800M
4.900M
5.000M
5.100M
5.200M
TIME in Secs
Δx = 66.25U Δy = -1.062


1
2
8.0V
6.0V
4.0V
2.0V
0V
>>
6.0V
4.0V
2.0V
0V
-2.0V
-4.0V
Probe Cursor
A1 = 5.0154m, 3.9100
A2 = 5.0569m, 2.5002
dif= -41.539u, 1.4098
4.75ms 4.80ms 4.85ms 4.90ms 4.95ms 5.00ms 5.05ms 5.10ms 5.15ms 5.20ms
1 V(D1:1) 2 v(v3:+)
Time


5.000
4.000
3.000
2.000
1.000
LM118 in Volts
4.000
2.000
0
-2.000
-4.000
UA741 in Volts
1
2
4.800M
4.900M
5.000M
5.100M
5.200M
TIME in Secs

#28: Polarity Gain

This circuit can be used to modify the amplitude and shift the phase of a given input wave form. This is accomplished by detecting the input wave form at the non-inverting input of U1, which is configured as a input buffer. This signal is then fed into operational amplifiers U2, and U3. U2 provides a positive gain, which can be varied by tuning resistor R1. U3 provides a fixed inverted gain of -2. The output of U2 and U3 are then added together by U4. The output resulting from a zero grounded triangle wave, having a peak voltage of five volts, can be varied from five through negative five volts. This includes the output being capable of being ground. The phase can also be shifted from 0 to 180 degrees.

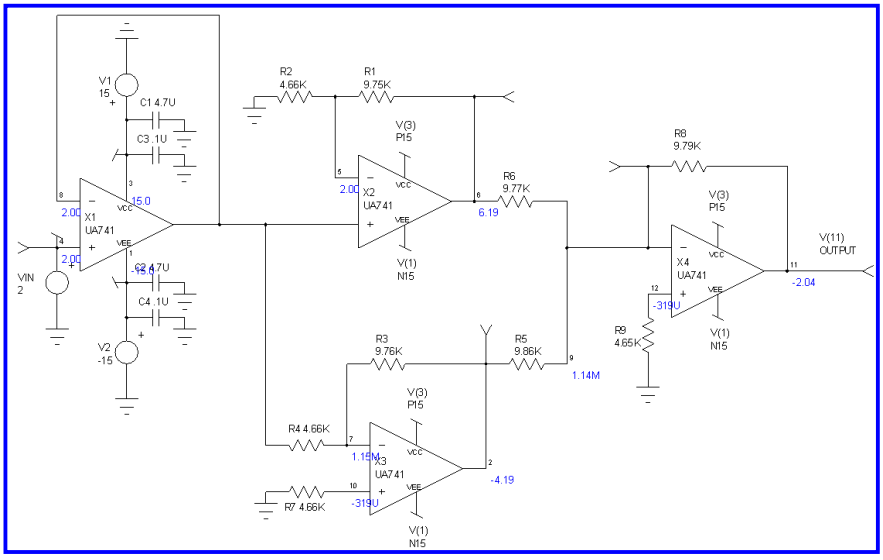


Figure 28-1: Schematic of Polarity Gain Circuit

The output of the polarity gain adjustment circuitry is determined by the following equations:

$$V_{in} := 2 \cdot volt$$

$R_1 := 9.84K\Omega$

$R_2 := 4.66K\Omega$

$R_3 := 9.76K\Omega$

$R_4 := 4.66K\Omega$

$R_6 := 9.77K\Omega$

$R_8 := 9.79K\Omega$

The output of operational amplifier X2 is determined by:

$$V_{out2} := V_{in}\left(\frac{R_1 + R_2}{R_2}\right)$$

$V_{out2} = 6.223\,volt$

The output of operational amplifier X3 is determined by:

$$V_{out3} := -V_{in}\left(\frac{R_3}{R_4}\right)$$

$V_{out3} = -4.189\,volt$

The output of the circuit is derived from the sum of the outputs of operational amplifiers X2 and X3.

$$V_{out} := -\left(V_{out2}\frac{R_8}{R_6} + V_{out3}\frac{R_8}{R_6}\right)$$

$V_{out} = -2.038\,volt$

The value of resistor R1 can be determined and set to invert the input signal.

$$V_{out} := -\left(V_{out2}\frac{R_8}{R_6} + V_{out3}\frac{R_8}{R_6}\right)$$

$$V_{out} = -V_{in}\frac{(R_1 + R_2)}{R_2}\cdot\frac{R_8}{R_6} + V_{in}\frac{R_3}{R_4}\cdot\frac{R_8}{R_6}$$

$V_{out} := -V_{in}$

$$R_1 := \frac{-\left(V_{out} + V_{in}\cdot\frac{R_8}{R_6} - V_{in}\cdot\frac{R_3}{R_4}\cdot\frac{R_8}{R_6}\right)}{V_{in}}\cdot\frac{R_2}{R_8}\cdot R_6$$

$$R_1 = 9.75\cdot K\Omega$$

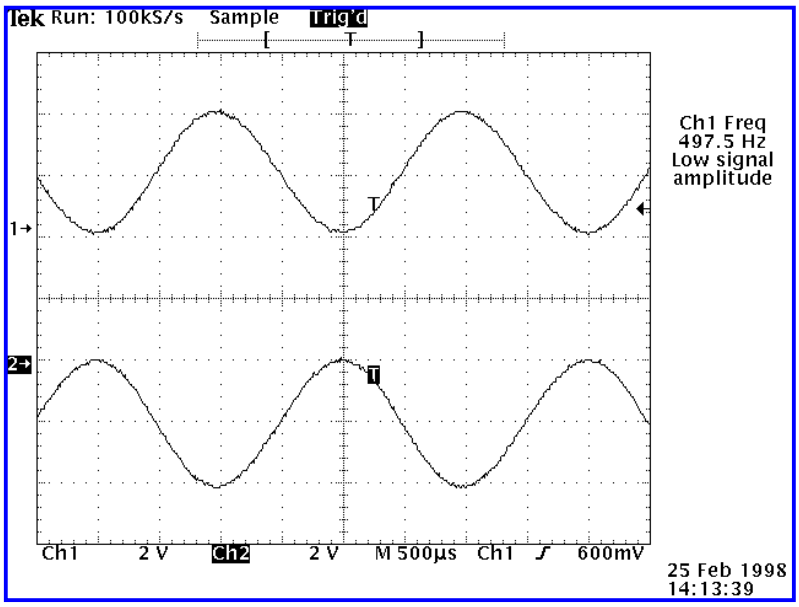


Figure 28-2: Measured Results (Top Waveform is Input, Bottom Waveform is Output)

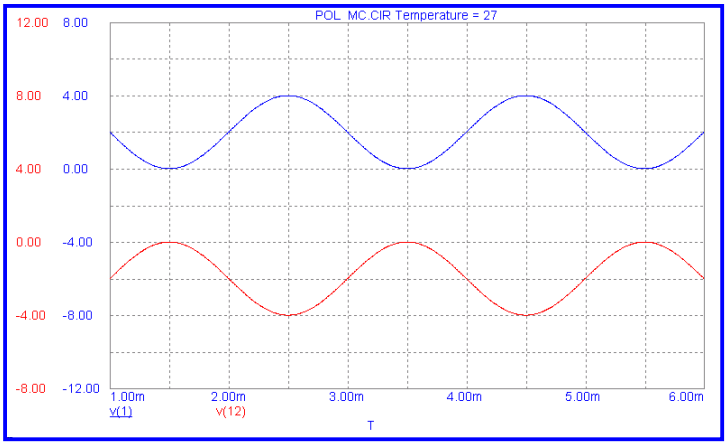


Figure 28-3: Micro-Cap V Simulated Results (Top Waveform is Input, Bottom Waveform is Output)

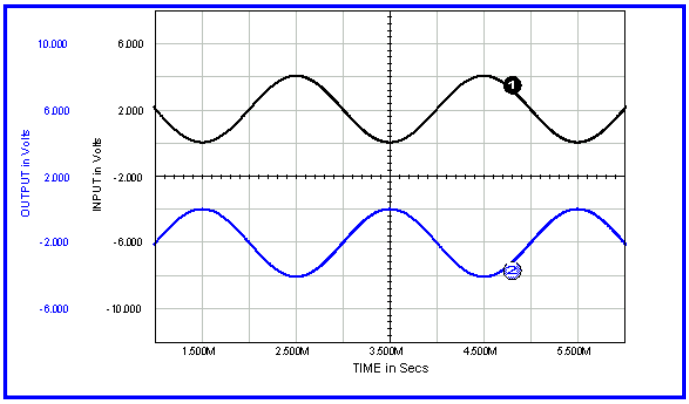


Figure 28-4: Micro-Cap V Simulated Results (Top Waveform is Input, Bottom Waveform is Output)

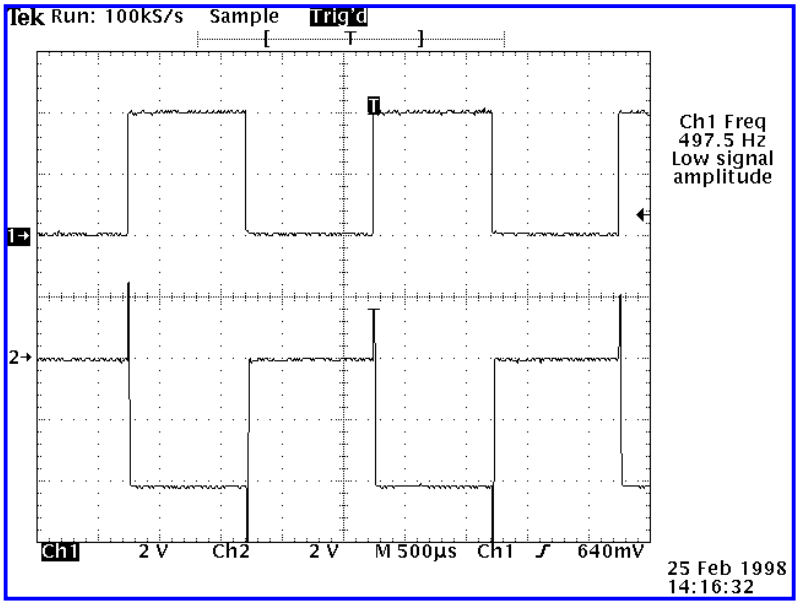


Figure 28-5: Measured Results (Top Waveform is Input, Bottom Waveform is Output)

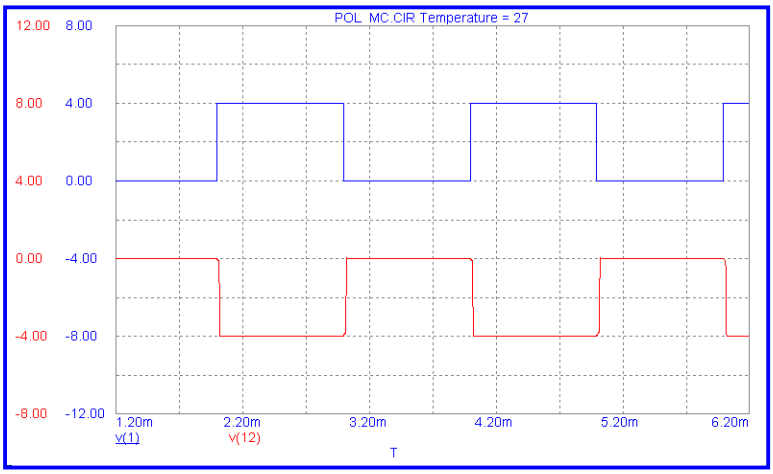


Figure 28-6: Micro-Cap V Simulated Results (Top Waveform is Input, Bottom Waveform is Output)

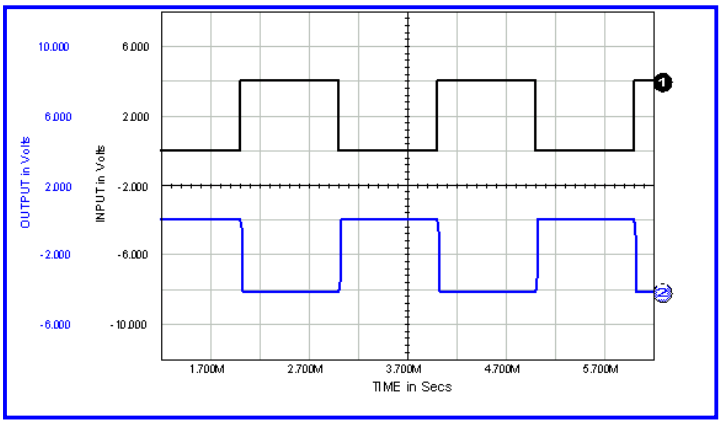


Figure 28-7: Ispice Simulated Results (Top Waveform is Input, Bottom Waveform is Output)

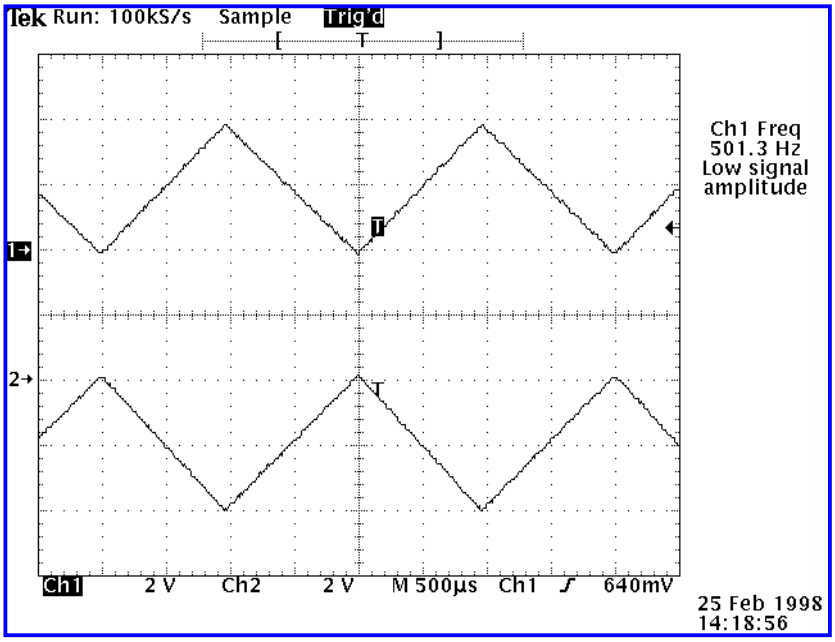


Figure 28-8: Measured Results (Top Waveform is Input, Bottom Waveform is Output)

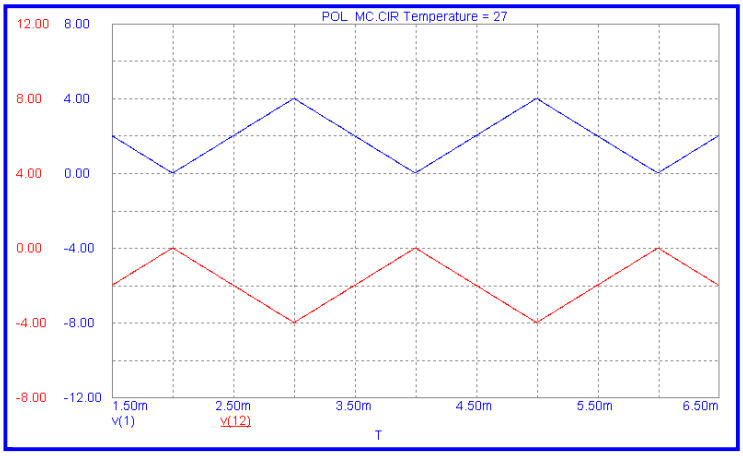


Figure 28-9: Micro-Cap V Simulated Results (Top Waveform is Input, Bottom Waveform is Output)

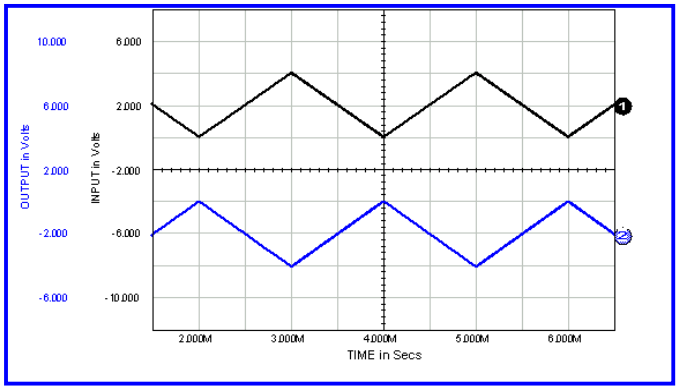


Figure 28-10: Ispice Simulated Results (Top Waveform is Input, Bottom Waveform is Output)

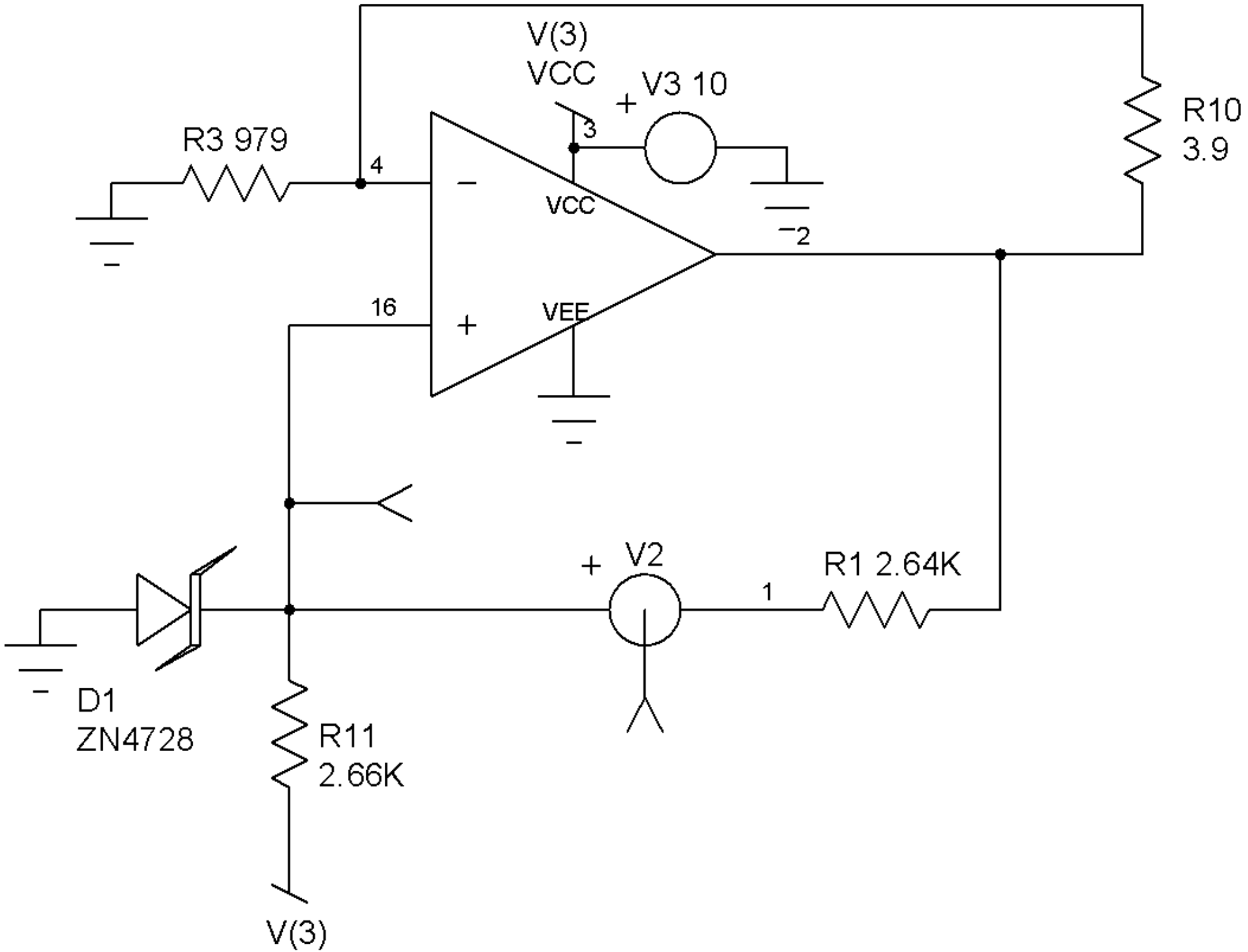
The simulation results were recorded for the analysis that had the following input voltage and transient statement.

Pulse 0 4 0 1n 1n 1m 12m

.TRAN 5u 7m 0 5u

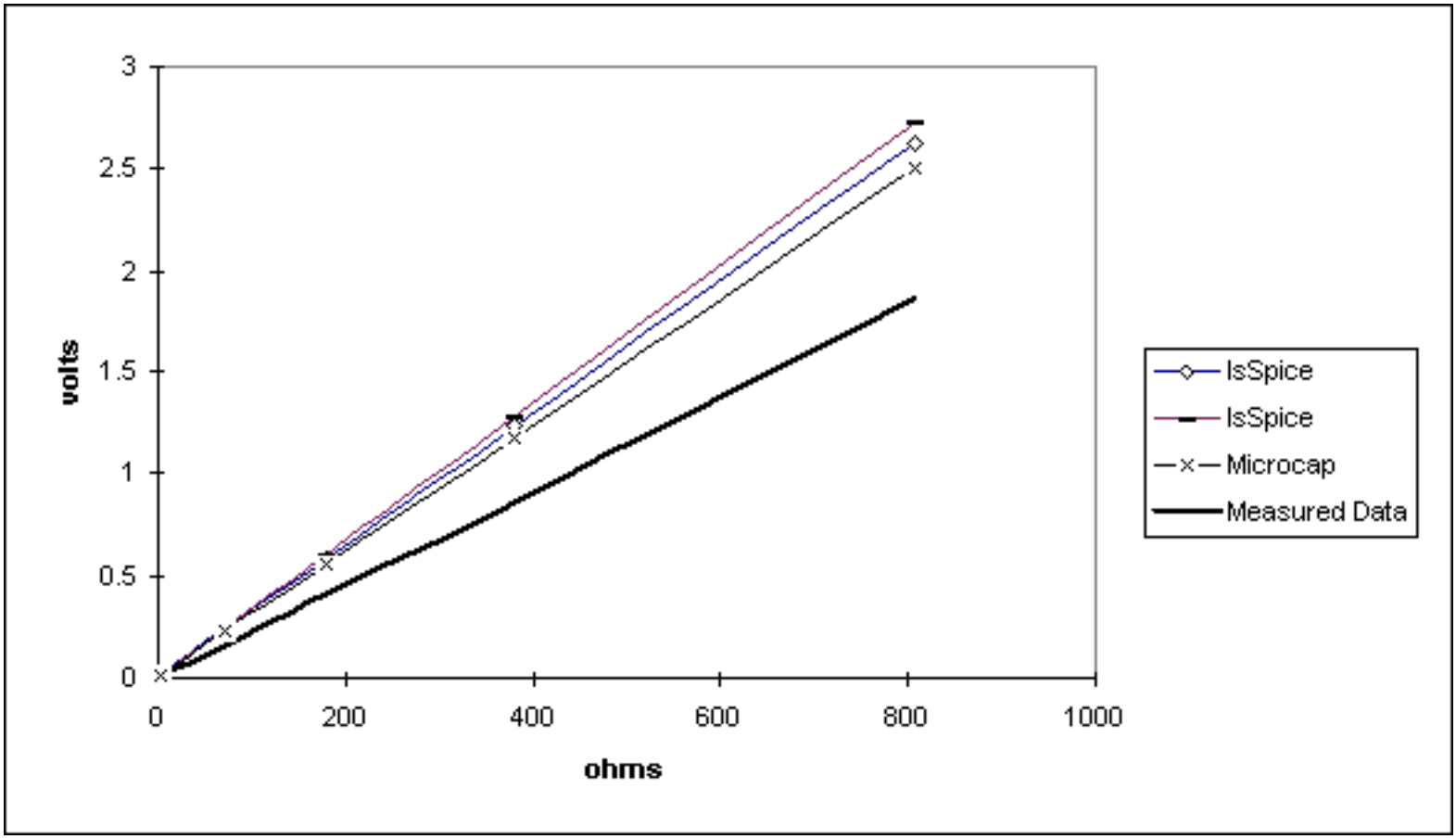
Table 28-1: Simulation Results

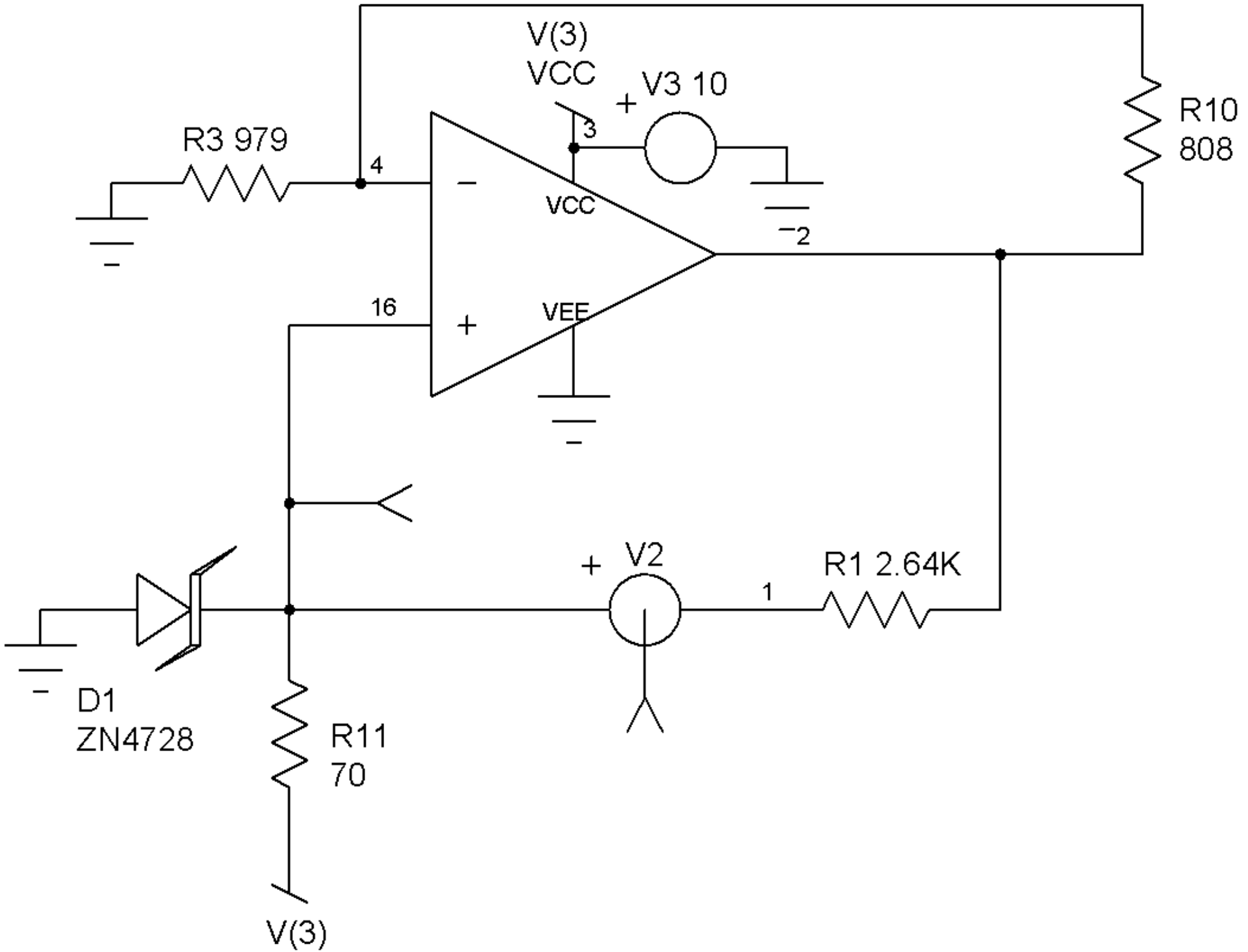
Simulator	File Name	Run Time
Micro-Cap V	Pol_mc	20.94 Sec
Ispice	Pol_ga	13.033 Sec


V(3)
VCC
V3 10
R10
3.9
R3 979
4
3
VCC
2
16
VEE
V2
R1 2.64K
1
D1
ZN4728
R11
2.66K
V(3)


VCC

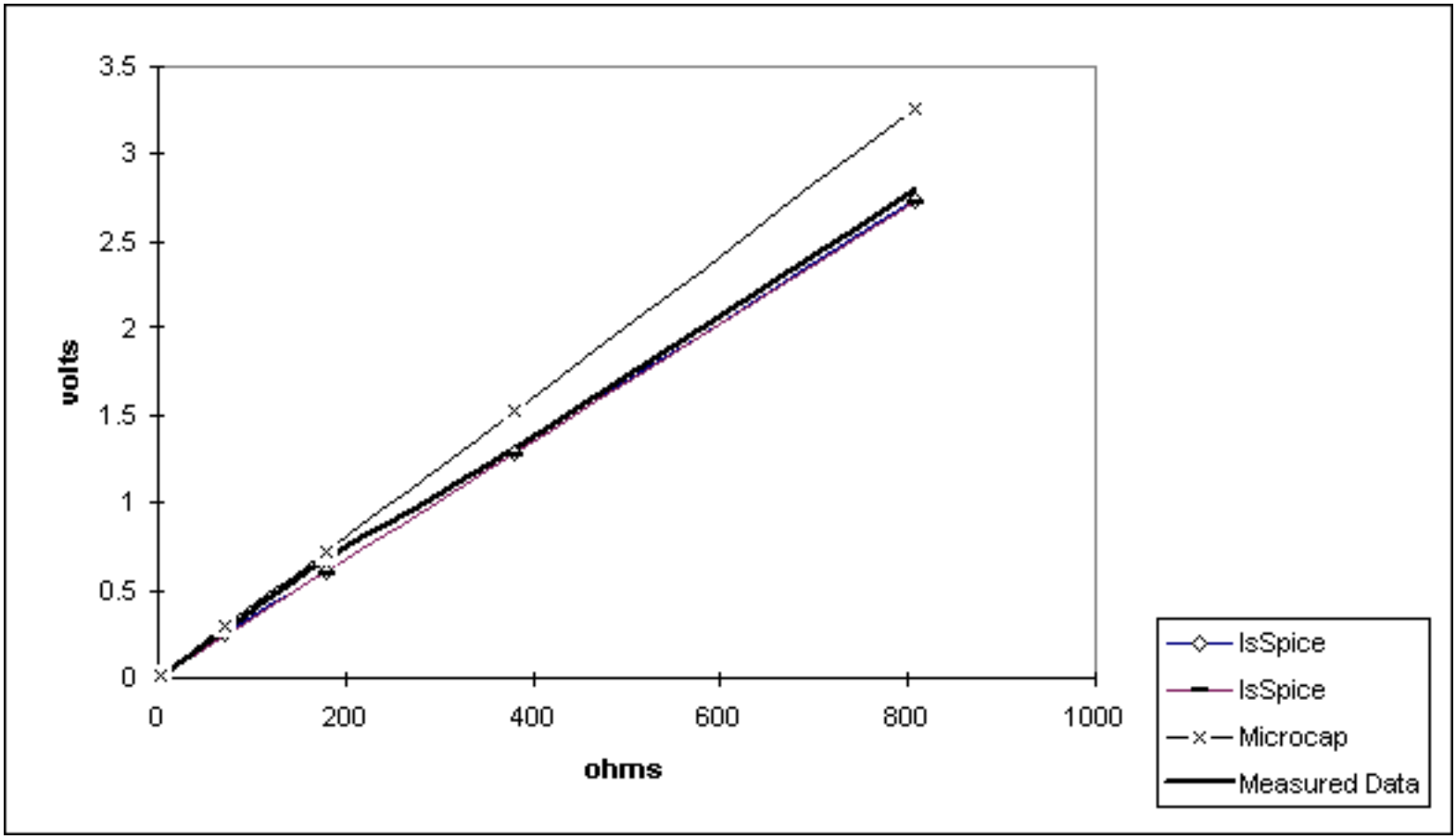
1N4728 Soft Operation Zener Voltage Comparison				
Conditions	Measured Zener Voltage			
OHMs Tested	IsSpice	Pspice	Microcap	Measured Data
3.9	3.165	3.3	3.009	2.18
72.5	3.166	3.3	3.01	2.19
179	3.167	3.3	3.013	2.19
379	3.17	3.3	3.017	2.21
808	3.174	3.3	3.026	2.24


3
2.5
2
1.5
1
0.5
0
volts
0
200
400
600
800
1000
ohms
IsSpice
IsSpice
Microcap
Measured Data


V(3)
VCC
V3 10
R10
808
R3 979
3
4
VCC
2
16
VEE
V2
R1 2.64K
1
D1
ZN4728
R11
70
V(3)


VCC

3.3 volt zener voltage				
Conditions	Measured Zener Voltage			
OHMs	IsSpice	Pspice	Microcap	Measured Data
3.9	3.32	3.3	3.939	3.41
72.5	3.32	3.3	3.94	3.4
179	3.32	3.3	3.941	3.41
379	3.32	3.3	3.944	3.41
808	3.321	3.3	3.95	3.41

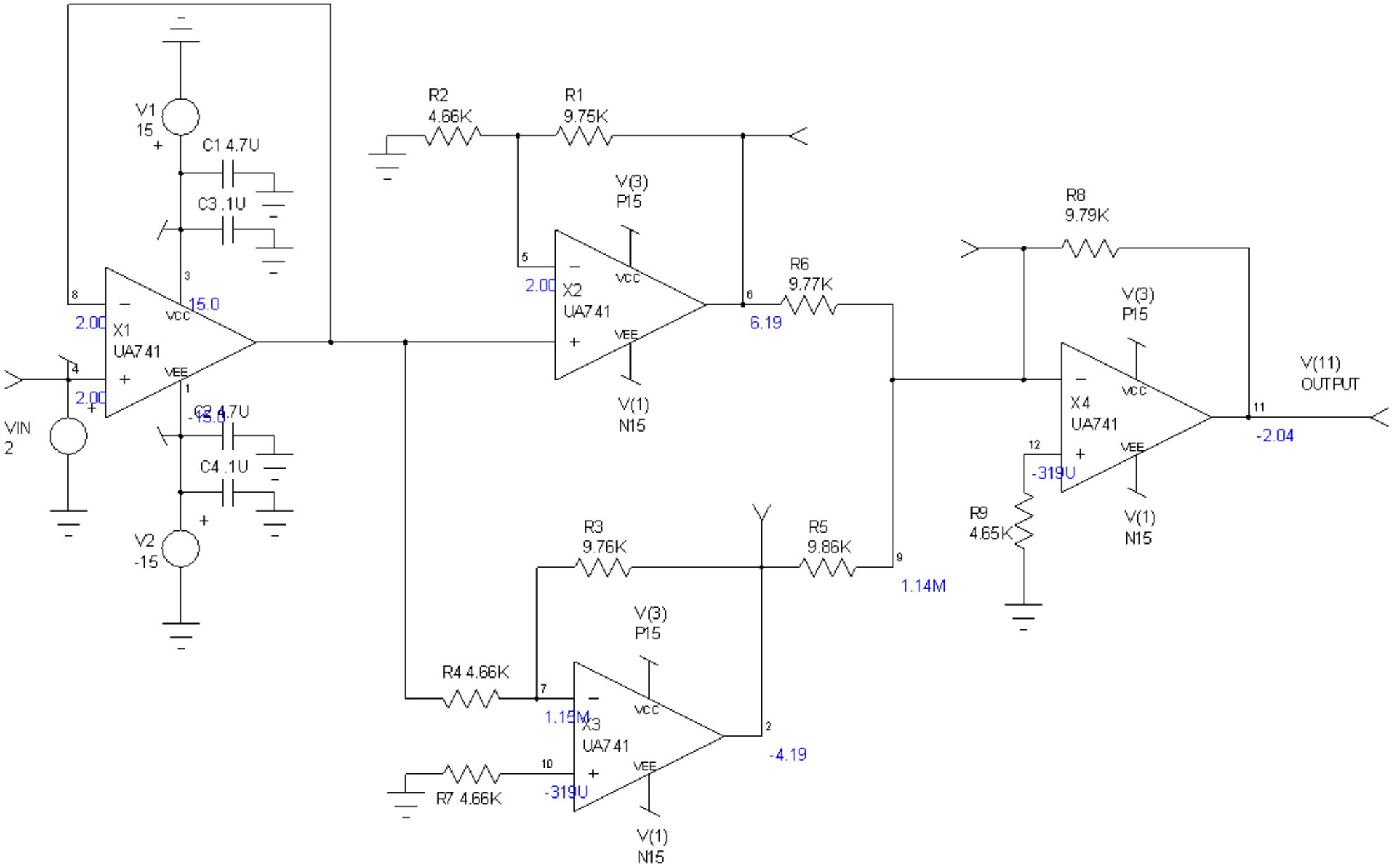

3.5
3
2.5
2
1.5
1
0.5
0
volts
0
200
400
600
800
1000
ohms
IsSpice
IsSpice
Microcap
Measured Data

7
Logic Circuits

The realm of digital signals is relatively new to the electrical world. The newness of digital signals has not slowed the impact of the digital phenomenon. Digital circuits are key in an incalculable amount of systems. The simplicity of ones and zeros can create the reality of computers, calculators, CD Roms, Fiber-optic transmissions, Digital Signal processors, and a host of other new technologies too numerous to mention.

The building blocks of digital circuits are straight forward. From these simple building blocks, the complex circuits of tomorrow are born. The manufacturers of SPICE have adapted to the digital revolution and as a result, all three of the simulators featured in this book have mixed mode simulation capabilities. The differences between analog and digital technologies create new and different concerns for engineers attempting to simulate digital circuits. Analog circuits have convergence problems, digital circuits have timing problems. Analog circuits are a time driven phenomenon, digital circuits are an event driven phenomenon.

In this chapter, we will give the simulation user the tools to utilize these building blocks to perform more complex functions. We will also attempt to aid the engineer in recognizing the potential pitfalls of both breadboard digital circuits, and simulated digital circuits.


V1
15
C1 4.7U
C3 .1U
R2
4.66K
R1
9.75K
V(3)
P15
R8
9.79K
R6
9.77K
6.19
X2
UA741
2.00
15.0
X1
UA741
2.00
VCC
VEE
V(1)
N15
V(3)
P15
V(11)
OUTPUT
X4
UA741
-2.04
-319U
R9
4.65K
VIN
2
C2 4.7U
-15.0
C4 .1U
V2
-15
R3
9.76K
R5
9.86K
1.14M
V(3)
P15
R4 4.66K
1.15M
X3
UA741
-4.19
R7 4.66K
-319U
V(1)
N15

$V_{in} := 2 \cdot volt$

$R_1 := 9.84K\Omega$

$R_2 := 4.66K\Omega$

$R_3 := 9.76K\Omega$

$$R_4 := 4.66K\Omega$$

$R_6 := 9.77K\Omega$

$R_8 := 9.79K\Omega$

$$V_{out2} := V_{in} \cdot \left(\frac{R_1 + R_2}{R_2} \right)$$

$$V_{out2} = 6.223\,\text{volt}$$

$$V_{out3} := -V_{in} \left(\frac{R_3}{R_4} \right)$$

$$V_{out3} = -4.189 \cdot volt$$

$$V_{out} := -\left(V_{out2}\frac{R_8}{R_6} + V_{out3}\cdot\frac{R_8}{R_6}\right)$$

$$V_{out} = -2.038 \text{ volt}$$

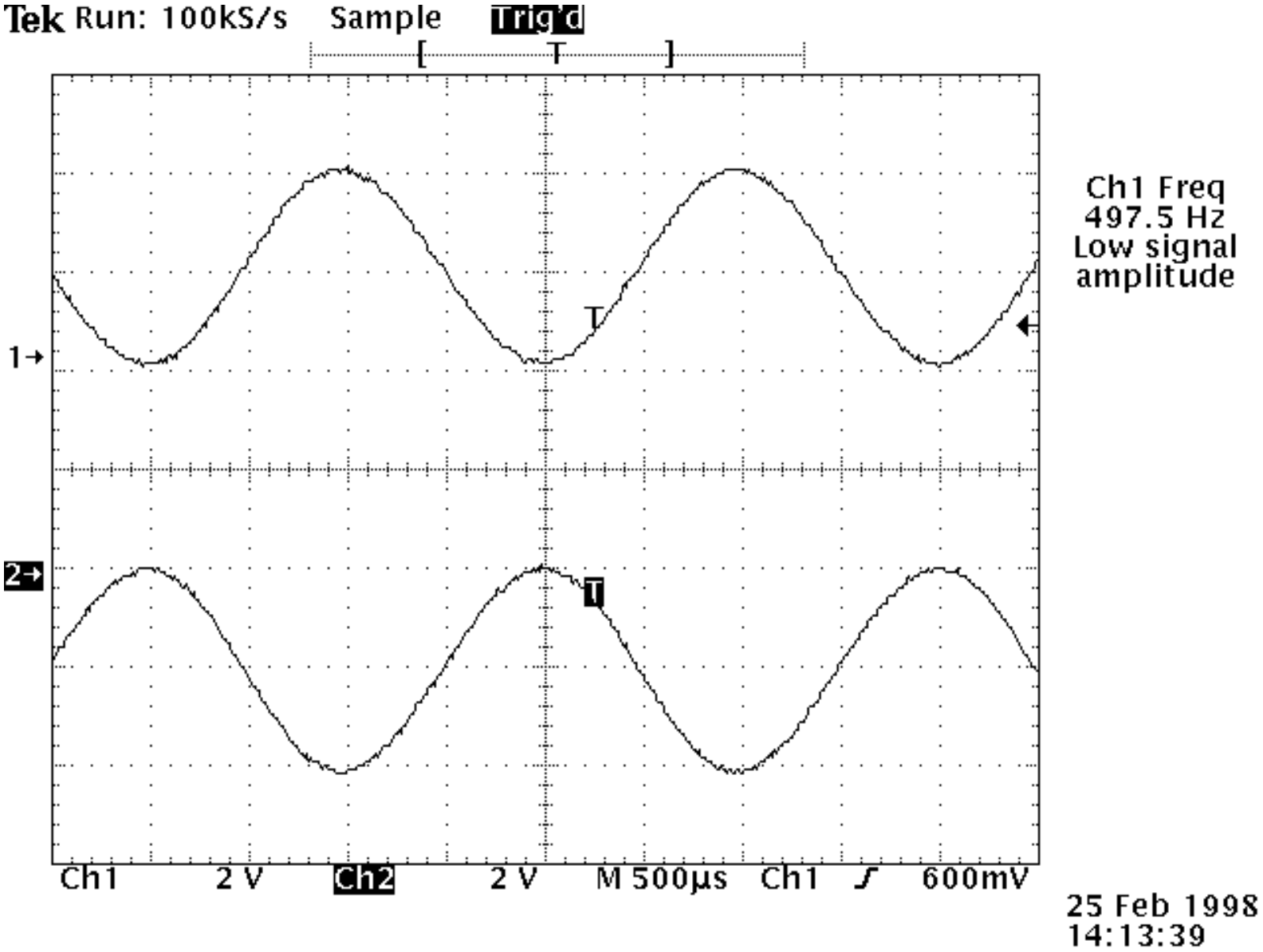
$$V_{out} := -\left(V_{out2}\frac{R_8}{R_6} + V_{out3}\cdot\frac{R_8}{R_6}\right)$$

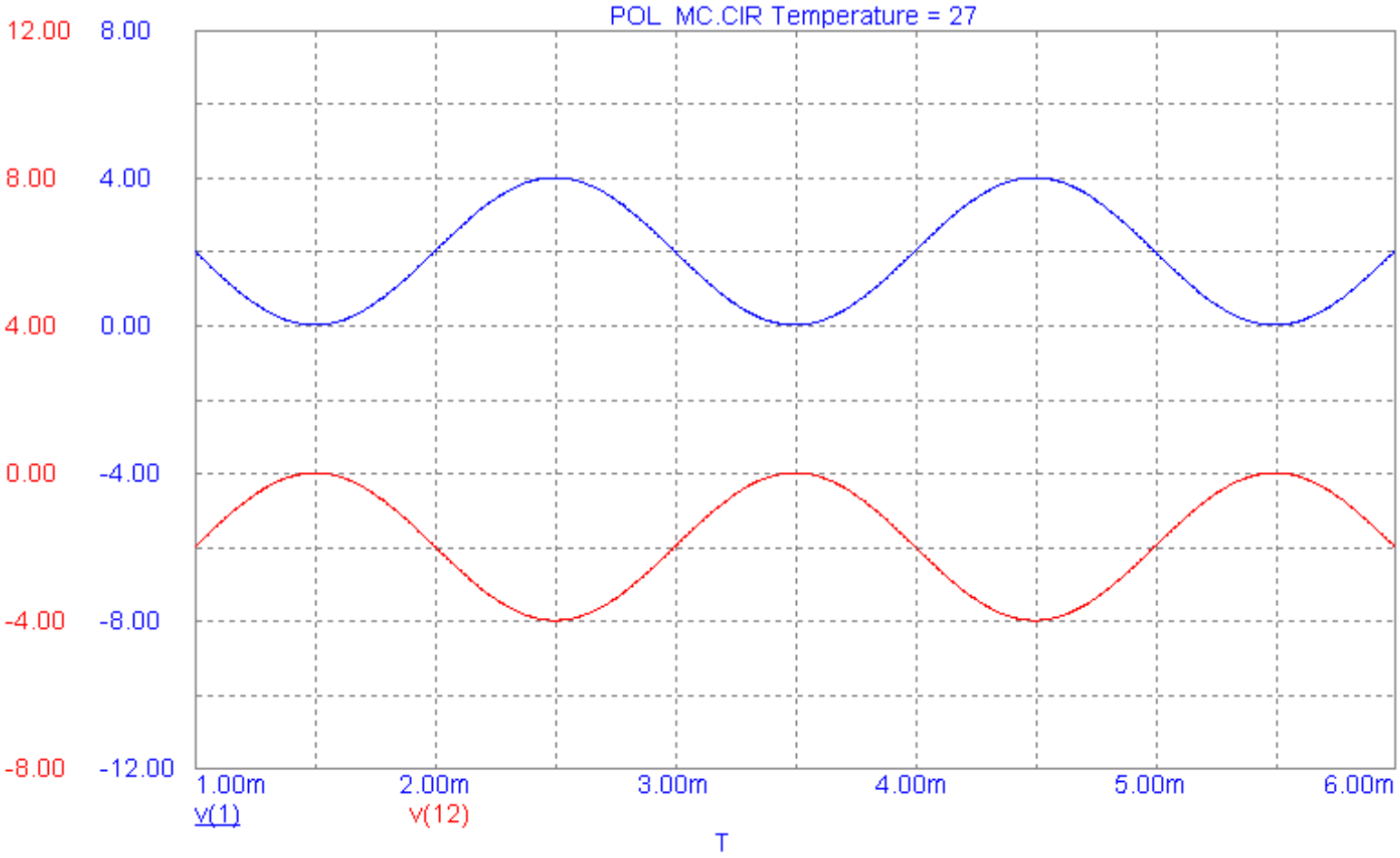
$$V_{out} = -V_{in} \cdot \frac{(R_1 + R_2)}{R_2} \cdot \frac{R_8}{R_6} + V_{in} \cdot \frac{R_3}{R_4} \cdot \frac{R_8}{R_6}$$

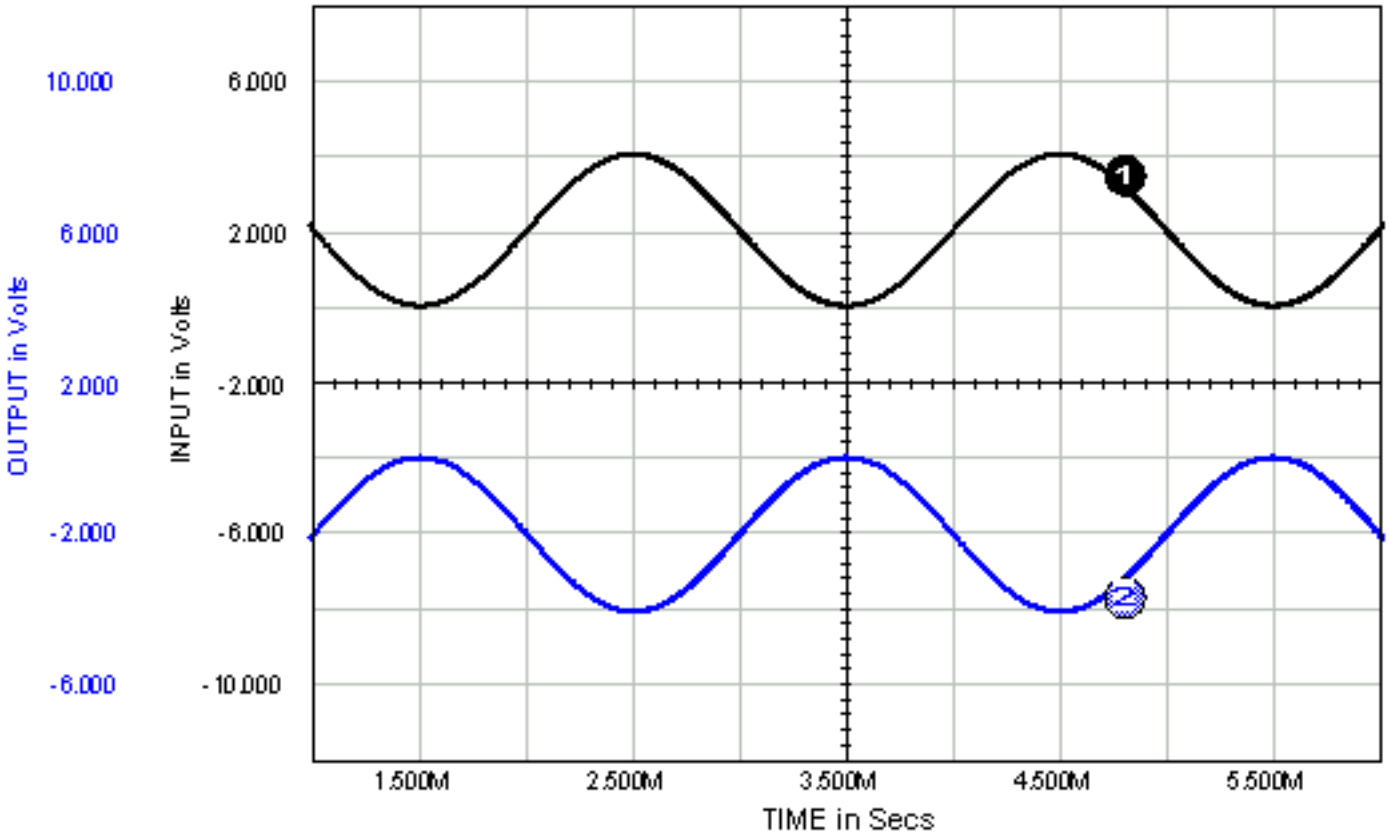
$$V_{out} := -V_{in}$$

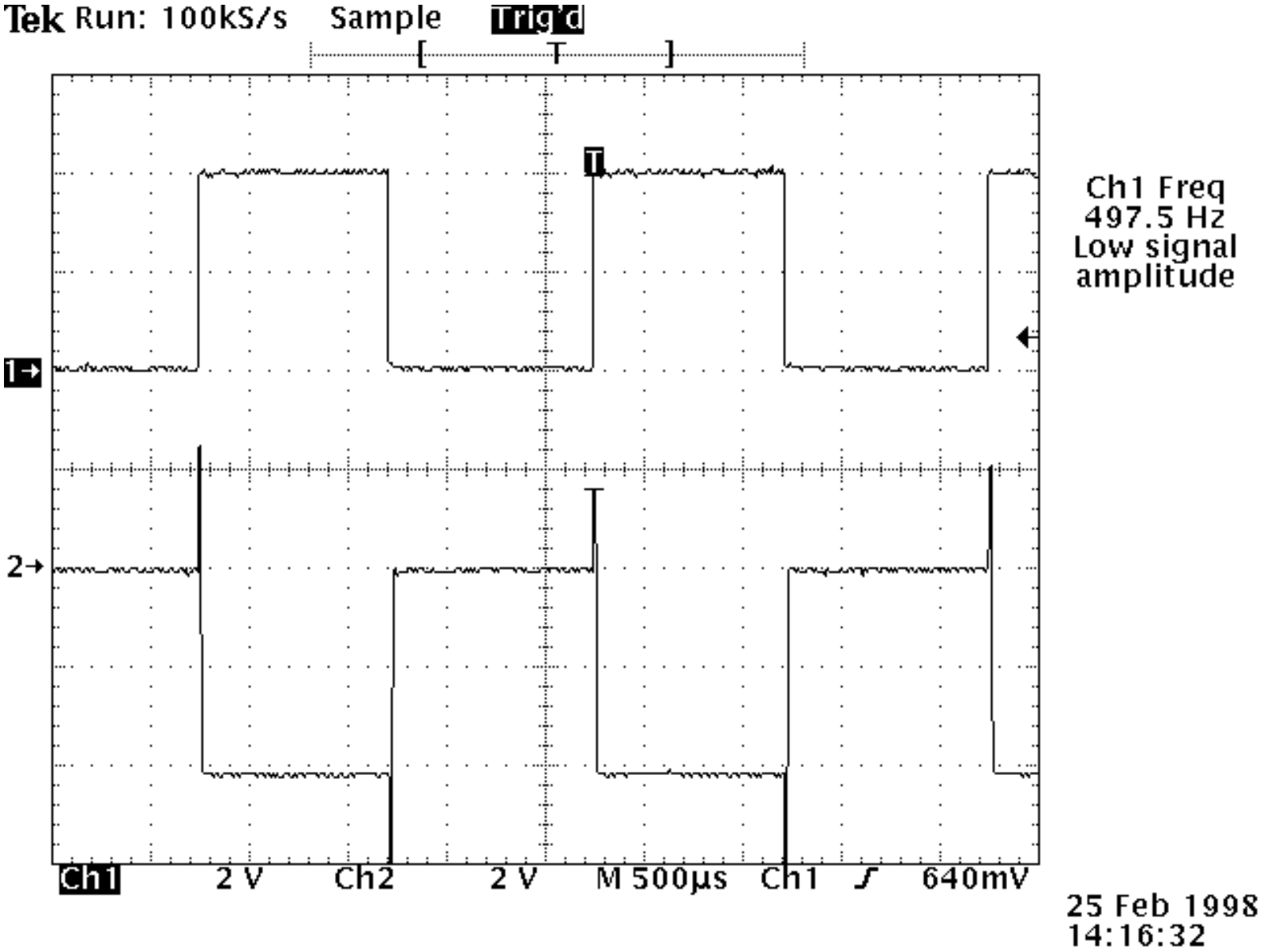
$$R_1 := \frac{-\left(V_{out} + V_{in}\cdot\frac{R_8}{R_6} - V_{in}\cdot\frac{R_3}{R_4}\cdot\frac{R_8}{R_6}\right)}{V_{in}}\cdot\frac{R_2}{R_8}\cdot R_6$$

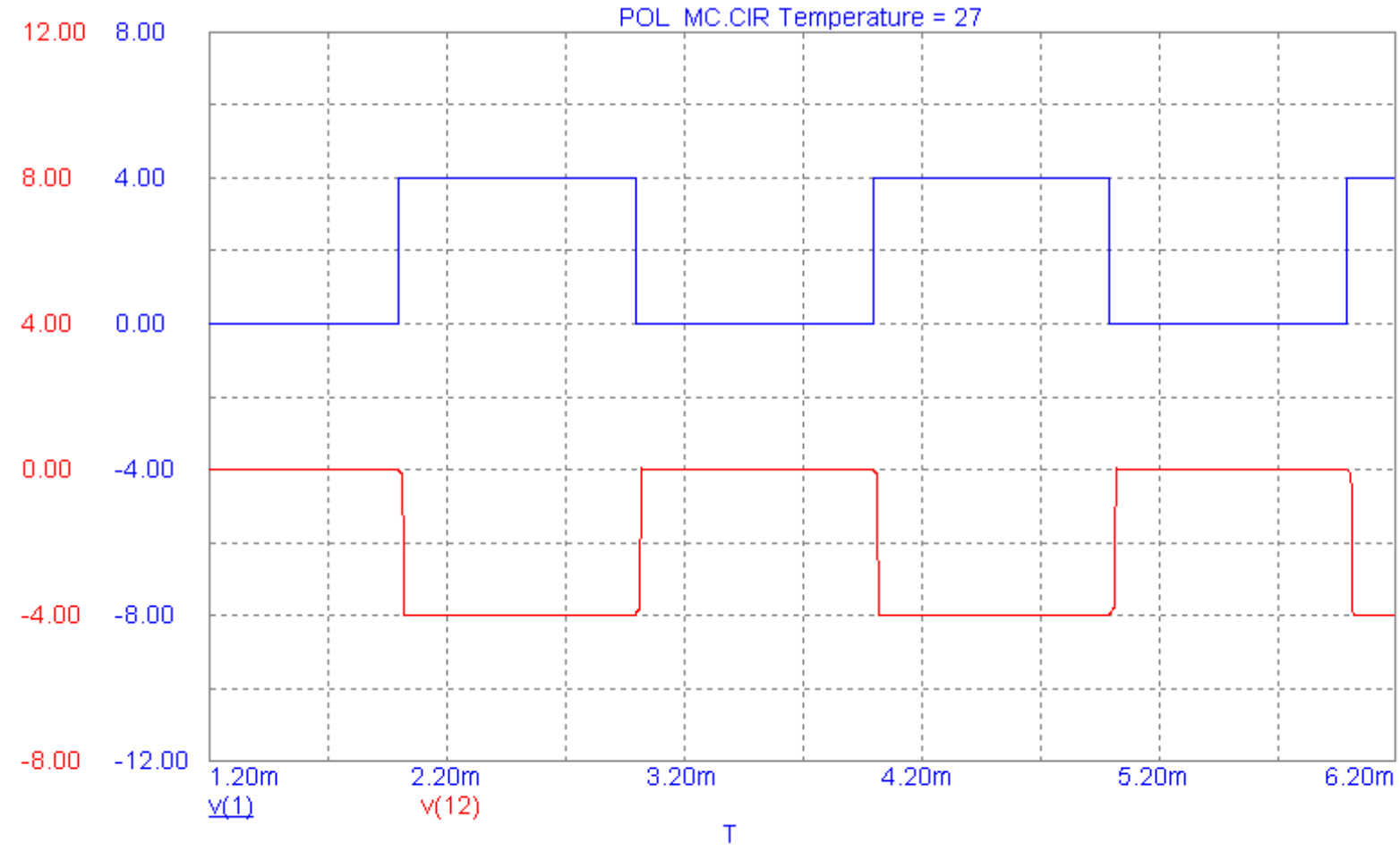
$$R_1 = 9.75 \cdot K\Omega$$

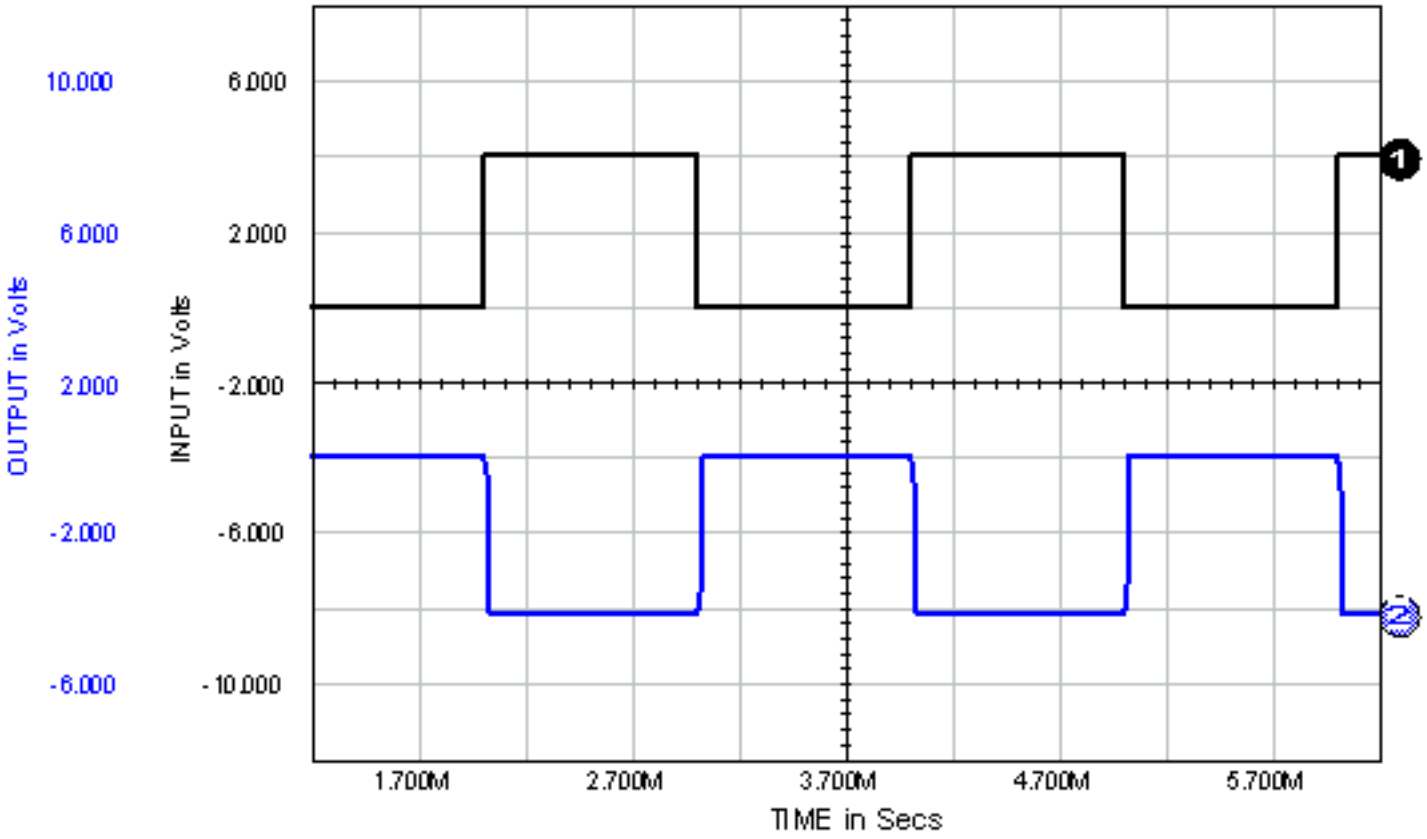

Tek Run: 100kS/s Sample Trig'd
Ch1 Freq
497.5 Hz
Low signal
amplitude
1→
2→
Ch1 2 V Ch2 2 V M 500µs Ch1 ∫ 600mV
25 Feb 1998
14:13:39

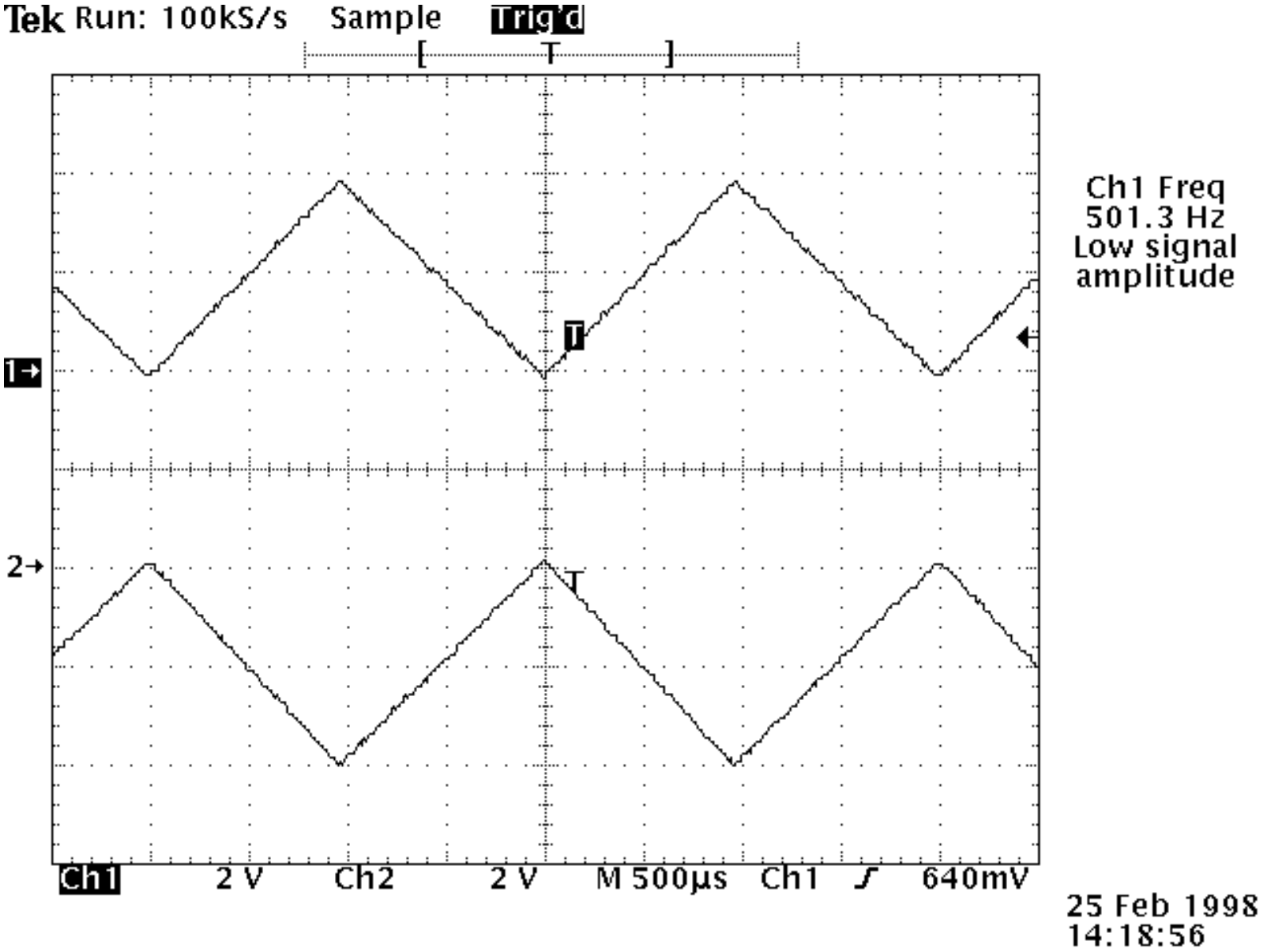

POL MC.CIR Temperature = 27
12.00
8.00
4.00
0.00
-4.00
-8.00
8.00
4.00
0.00
-4.00
-8.00
-12.00
1.00m
2.00m
3.00m
4.00m
5.00m
6.00m
V(1)
V(12)
T

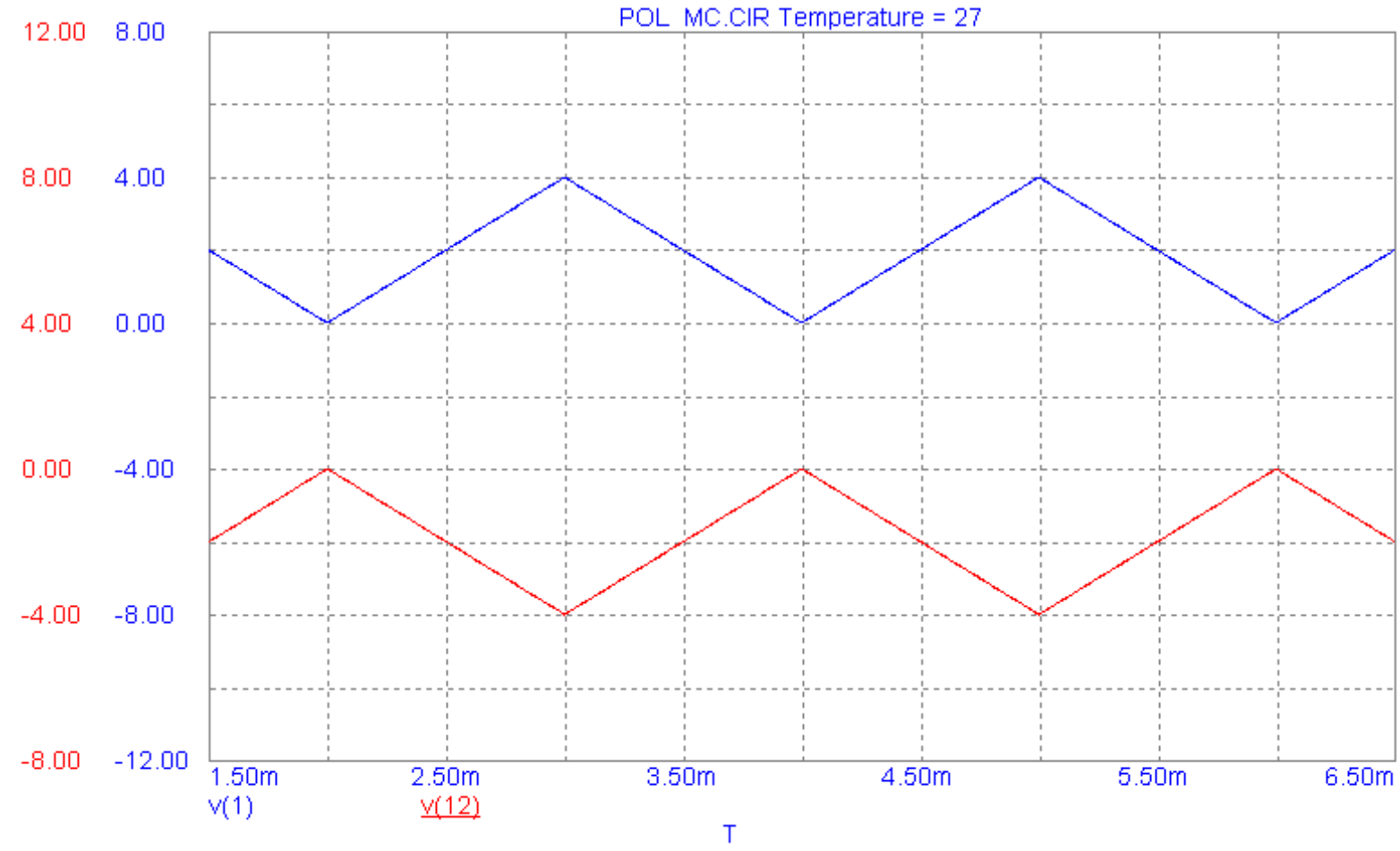

10.000
6.000
2.000
-2.000
-6.000
OUTPUT in Volts
6.000
2.000
-2.000
-6.000
-10.000
INPUT in Volts
1.500M
2.500M
3.500M
4.500M
5.500M
TIME in Secs
1
2

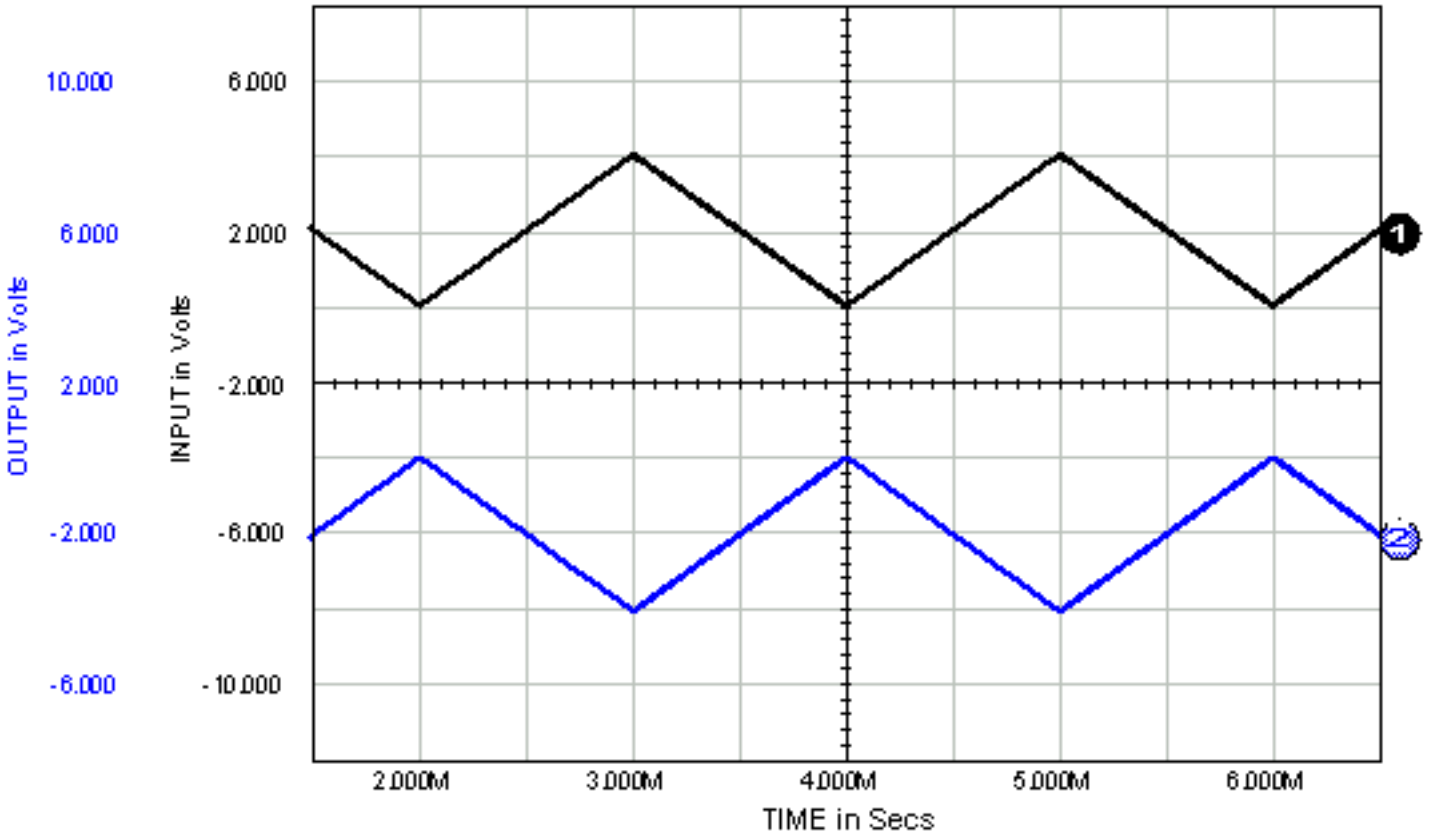

Tek Run: 100kS/s Sample Trig'd
Ch1 Freq
497.5 Hz
Low signal
amplitude
1→
2→
Ch1 2 V Ch2 2 V M 500µs Ch1 ∫ 640mV
25 Feb 1998
14:16:32


POL MC.CIR Temperature = 27
12.00
8.00
4.00
0.00
-4.00
-8.00
8.00
4.00
0.00
-4.00
-8.00
-12.00
1.20m
2.20m
3.20m
4.20m
5.20m
6.20m
V(1)
V(12)
T


10.000
6.000
2.000
-2.000
-6.000
OUTPUT in Volts
6.000
2.000
-2.000
-6.000
-10.000
INPUT in Volts
1.700M
2.700M
3.700M
4.700M
5.700M
TIME in Secs
1
2


Tek Run: 100kS/s Sample Trig'd
Ch1 Freq
501.3 Hz
Low signal
amplitude
1→
2→
Ch1 2 V Ch2 2 V M 500µs Ch1 ∫ 640mV
25 Feb 1998
14:18:56


POL MC.CIR Temperature = 27
12.00
8.00
8.00
4.00
4.00
0.00
0.00
-4.00
-4.00
-8.00
-8.00
-12.00
1.50m
2.50m
3.50m
4.50m
5.50m
6.50m
V(1)
V(12)
T


10.000
6.000
2.000
-2.000
-6.000
OUTPUT in Volts
6.000
2.000
-2.000
-6.000
-10.000
INPUT in Volts
2.000M
3.000M
4.000M
5.000M
6.000M
TIME in Secs
1
2

#29: Binary Counter

Using JK flip flops, we can design a circuit that will count a clock signal and provide a divided output of that clock signal.

This circuit is shown in figure 29-1. The circuit is powered by an external 5 volts (not shown on schematic). The clock is running at 100 Khz with a 50 % duty cycle. The J and K pins of the Flip Flop are tied high and the Clear and reset pins are tied low. This causes the Q output to change states when the clock goes from low to high. Because the circuit only transitions on the low to high clock, two clock cycles go by for one output cycle, thus creating a divide by two output. If this new signal is fed into another J-K flip flop configured the same way, this signal is also divided by 2, which is the original signal divided by 4. Using this method, and N more J-K flip flops, any division of 2^N can be realized.

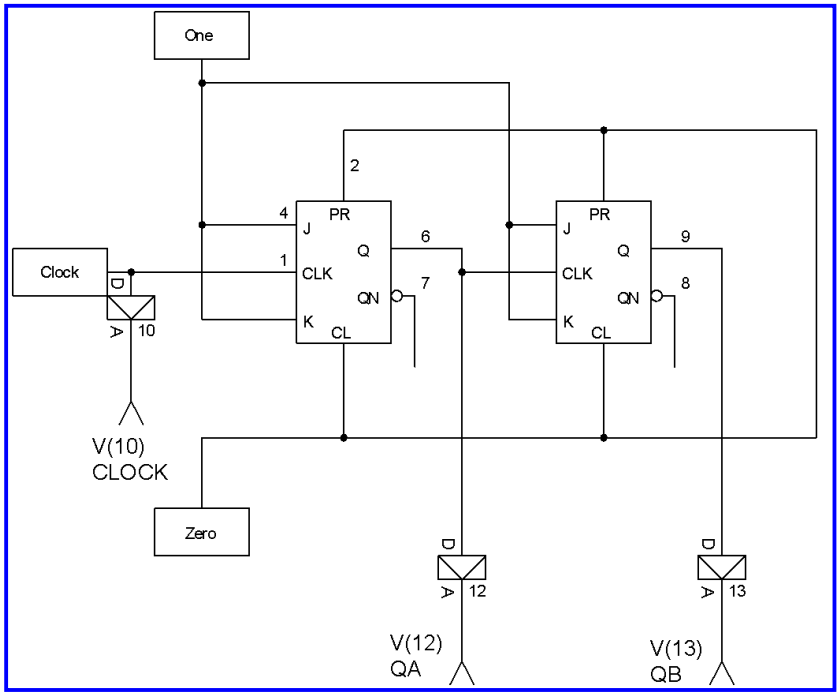


Figure 29-1: Schematic of Binary Counter Circuit

The resulting breadboard waveforms are shown in Figure 29-2. The top waveform is the 100 Khz clock. The middle waveform is the Q output of the first J-K flip flop stage (divide by 2). The bottom waveform is the Q output of the second J-K flip flop stage (divide by 4). This circuit was simulated using IsSpice, Pspice, and Microcap. The results of each of these simulators are shown in

Figure 29-3 through 29-5.

- Breadboard tip: Bypass capacitors may be necessary (and are recommended) from the Vdd pin to ground in order to minimize signal jitter and noise effects.

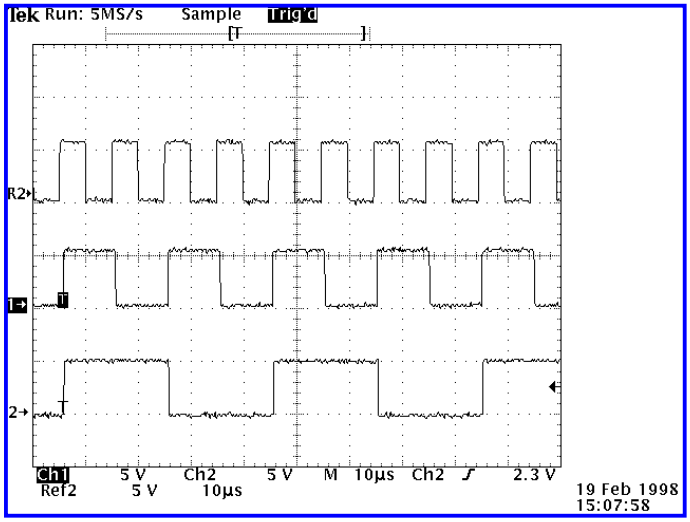


Figure 29-2: Breadboard waveforms of Binary Counter Circuit

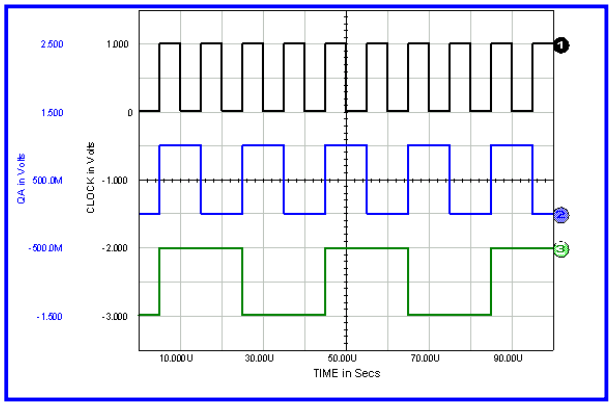


Figure 29-3: IsSpice waveform results of Binary Counter Circuit

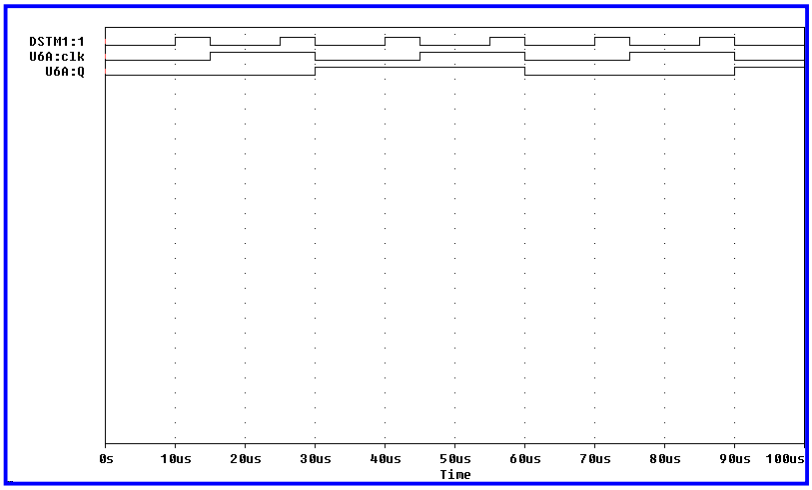


Figure 29-4: Pspice waveform results of Binary Counter Circuit

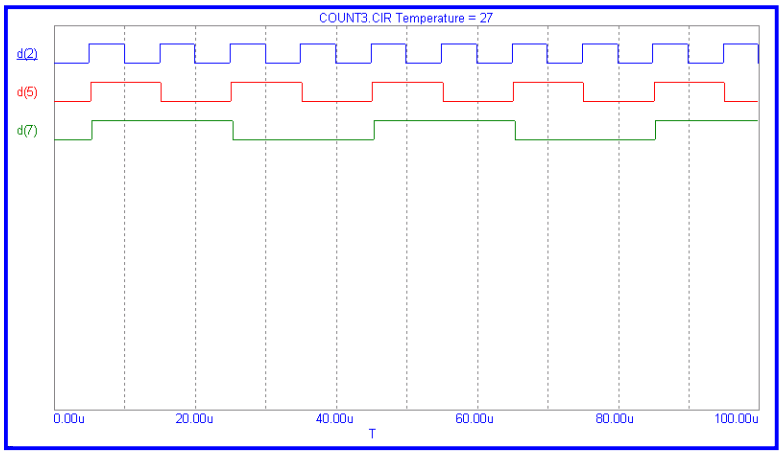


Figure 29-5: Pspice waveform results of Binary Counter Circuit

For circuits that count to values higher than four, a counter IC is the more logical choice. Parts such as the CD4017 contain any number of these J-K counter stages that can be used to count to any number required.

Run Time Summary		
IsSpice v 7.6	PsPice v 6.3	Micro-Cap V v2
5.35 Sec	4.05 Sec	1.536 Sec
Advantages: Accurate, very low propagation delay		
Disadvantages: can be realized with fewer parts		

Filenames: Count (IsSpice) Count_2 (Pspice) Count3 (Microcap)

#30: Binary Decoder

Using the characteristics of circuit #29, we can add AND gates and create a Binary Decoder circuit. The Binary Decoder circuit looks at two input signals and determines whether the signal corresponds to a 0, 1, 2, or 3. The truth table for the Binary Decoder is shown in Table 30-1.

Input Signal Q A QB		Output of Decoder
Low	Low	0
High	Low	1
Low	High	2
High	High	3

Table 30-1: Truth Table for the Binary Decoder

The total circuit schematic that provides this logic function is shown in Figure 30-1. The binary counter circuit (circuit #29) provides the input signals and the AND gates provide the Decoder logic.

The clock signal is 100 Khz at 50 % duty cycle.

- Breadboard tip: Bypass capacitors may be necessary (and are recommended) from the Vdd pin to ground in order to minimize signal jitter and noise effects.

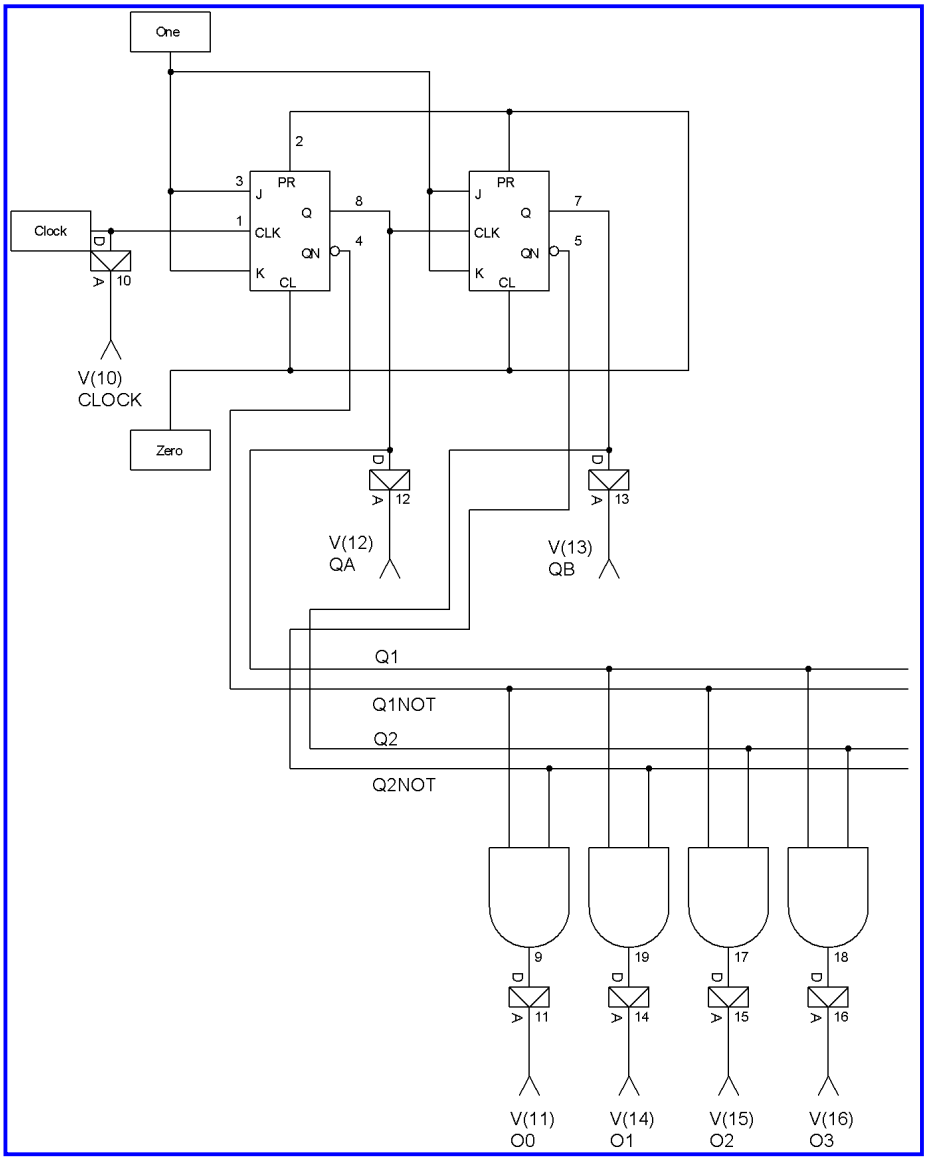


Figure 30-1: Schematic for the Binary Decoder

The breadboard results are shown in Figure 30-2. Due to the limitations of the Oscilloscope we used, only four traces may be shown on one plot. The top trace of Figure 30-2 is the QA output. The second trace from the top is the QB output. The third trace from the top is the zero code. The bottom trace is the one code. The results of Figure 30-2 illustrate the decoding properties. Figure 30-3 shows the Microcap results.

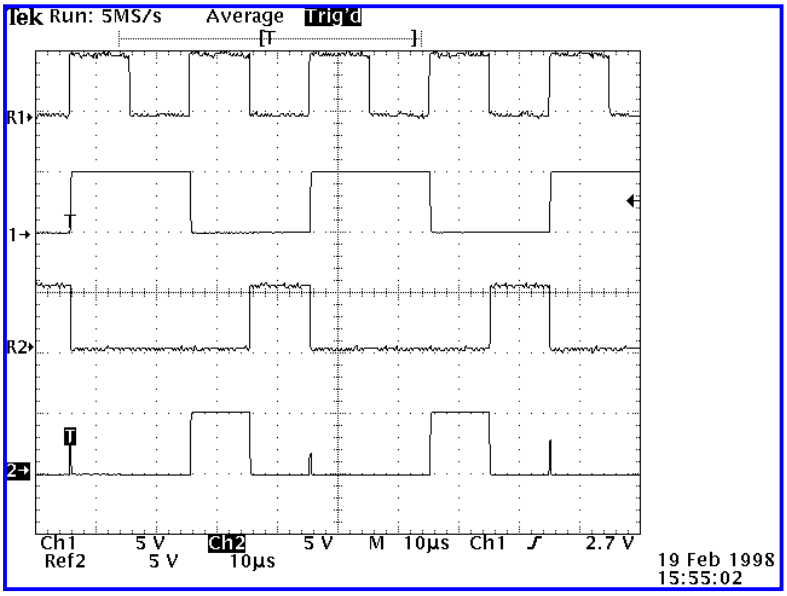


Figure 30-2: Breadboard results of the Binary Decoder circuit (0 and 1)

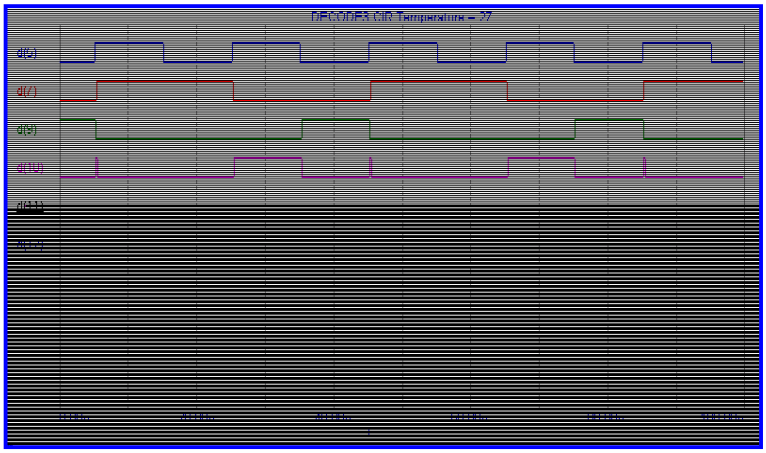


Figure 30-3: Microcap results of the Binary Decoder circuit (0 and 1)

The breadboard results of the two and three code cases are shown in Figure 30-4. The top two traces are QA and QB, while the bottom two traces are the two and three codes. The Microcap simulation results are shown in Figure 30-5.

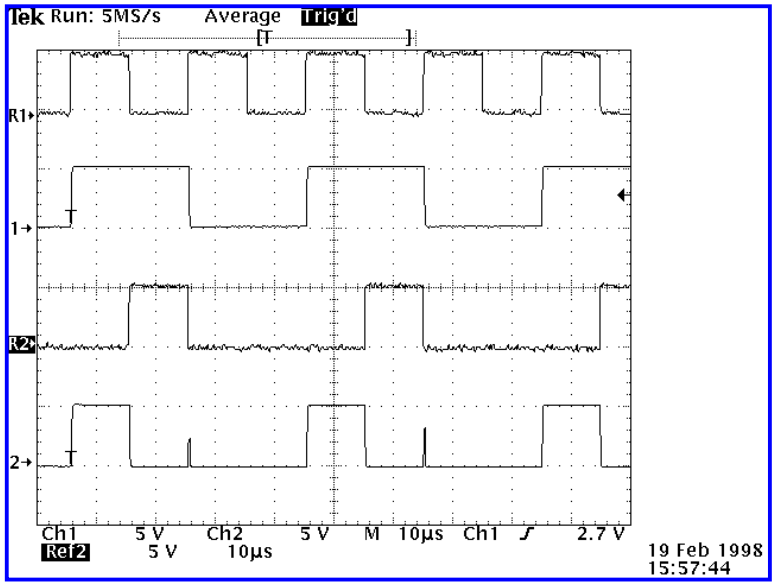


Figure 30-4: Breadboard results of the Binary Decoder circuit (2 and 3)

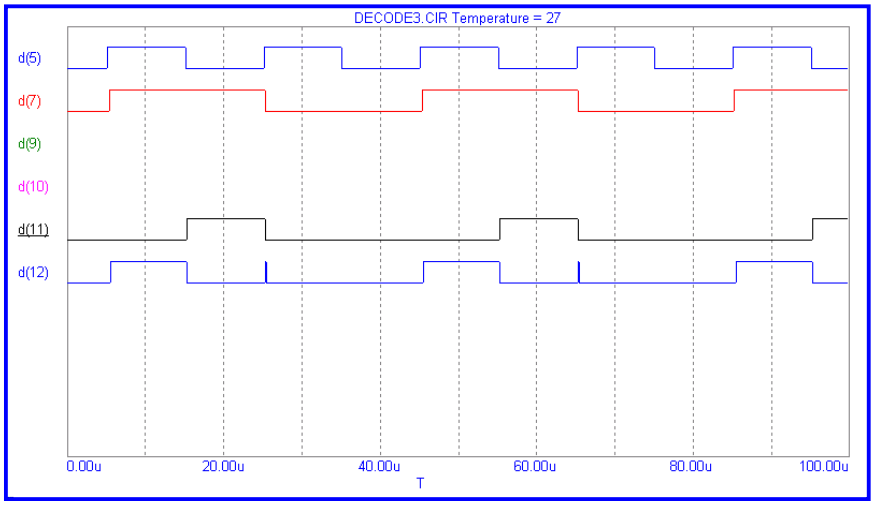


Figure 30-5: Microcap results of the Binary Decoder circuit (2 and 3)

The Microcap simulator was exact enough to show the slight overlap of the decoder after the 1 code and the 3 code. This is a result of the race condition that exists in this circuit. Parameters such as rise and fall times must be accurate in order to represent the true behavior of the digital circuitry.

The IsSpice and Pspice simulation results are shown in Figures 30-6 and 30-7. The simulation results from the IsSpice and Pspice are in the same format as the results from the breadboard and the Microcap simulator.

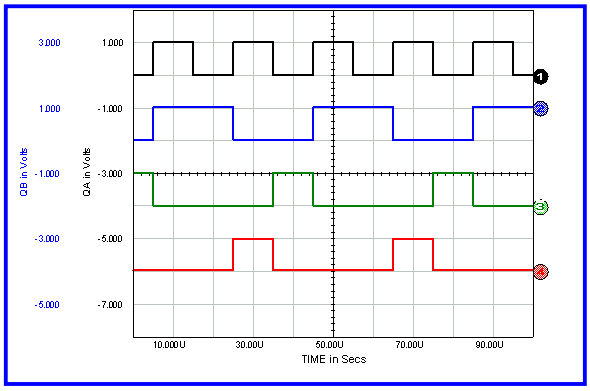


Figure 30-6A: IsSpice results of the Binary Decoder circuit (0 and 1)

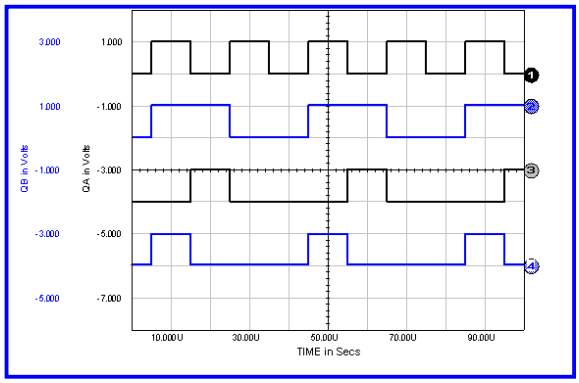


Figure 30-6B: IsSpice results of the Binary Decoder circuit (2 and 3)

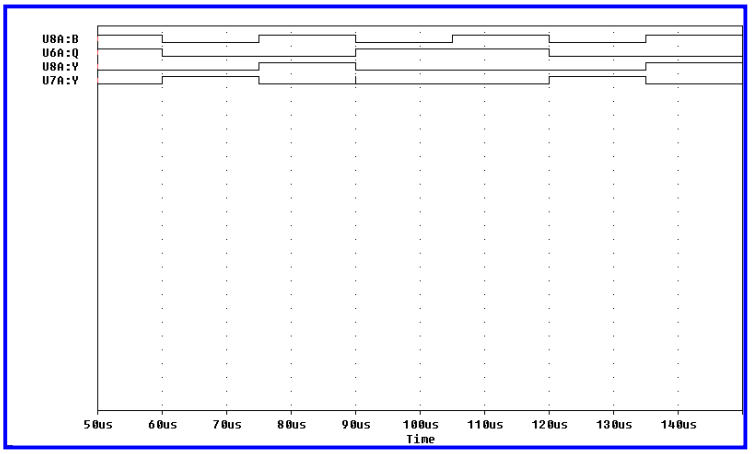


Figure 30-7A: Pspice results of the Binary Decoder circuit (0 and 1)

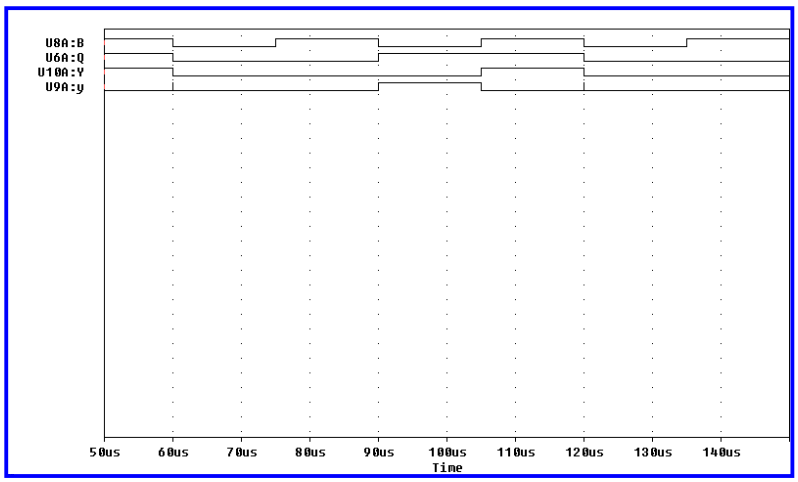


Figure 30-7B: Pspice results of the Binary Decoder circuit (2 and 3)

Run Time Summary		
IsSpice v 7.6	PsPice v 6.3	Micro-Cap V v2
23.883 Sec	6.71 Sec	2.304 Sec
Advantages: Accurate, very low propagation delay		
Disadvantages: can be realized with fewer parts		

Filenames: Decode (IsSpice) Decode2 (Pspice) Decode3 (Microcap)

References

DeMassa, Thomas A. Electrical and Electronic Devices, Circuits and Instruments. West Publishing Co. 1989.

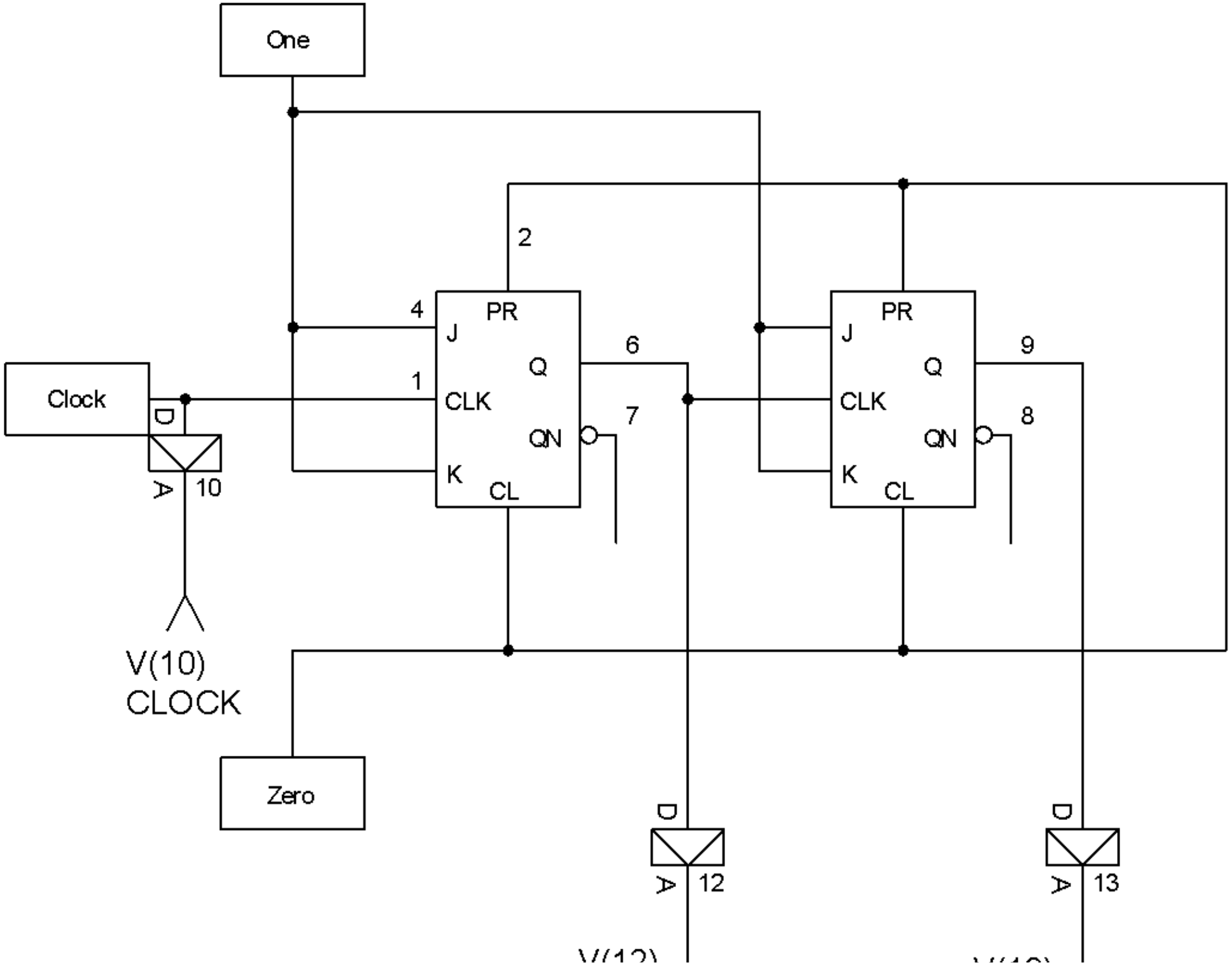
Gibilisco, Stan. Ed. 1994. Amateur Radio Encyclopedia. TAB Books, PA

Gibilisco, Stan. Ed. 1995. Encyclopedia of Electronics. TAB Books, PA

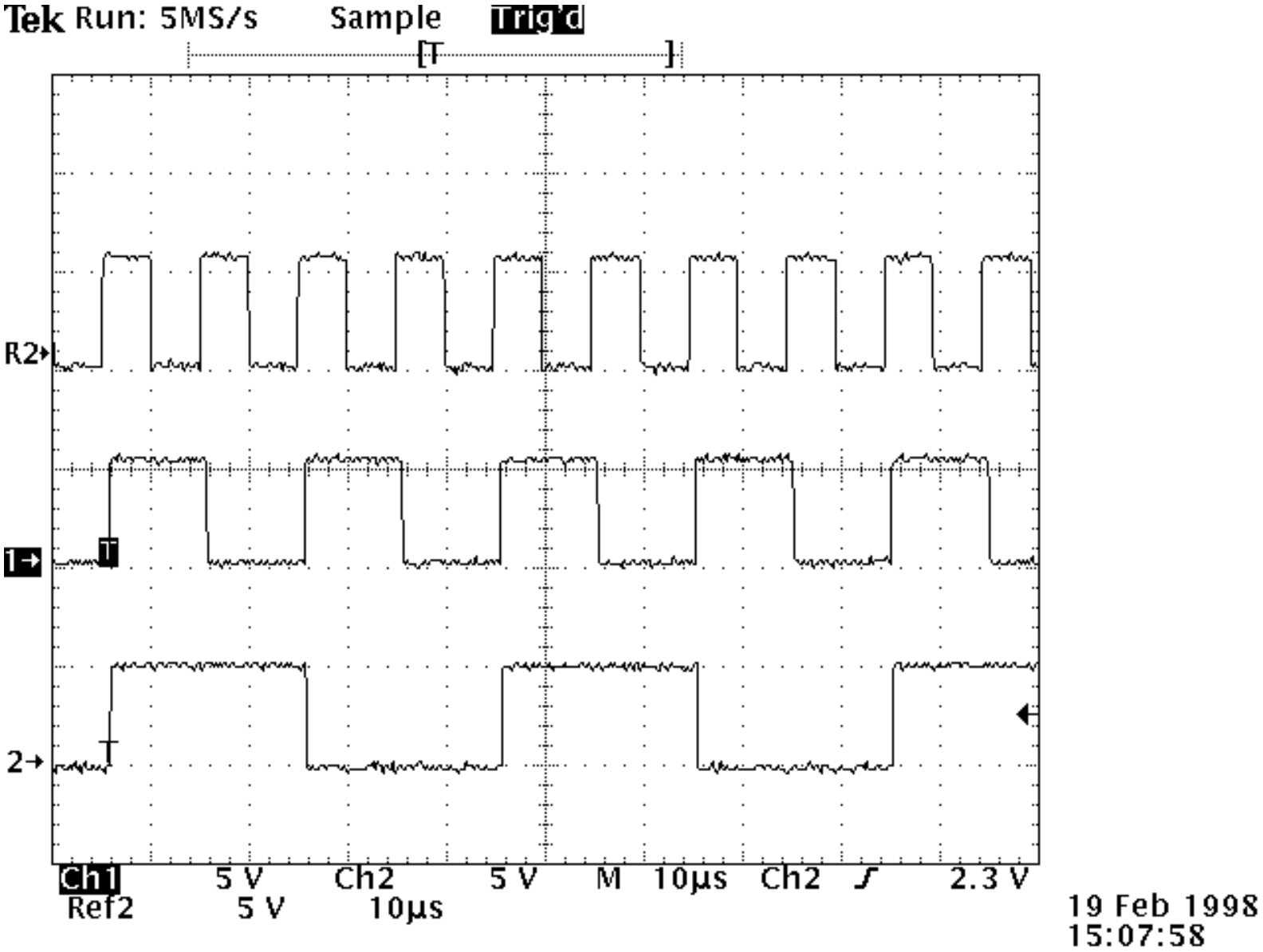
Kimbler, Will. Practical Digital Electronics for Technicians. BH Newnes, Oxford. 1994.

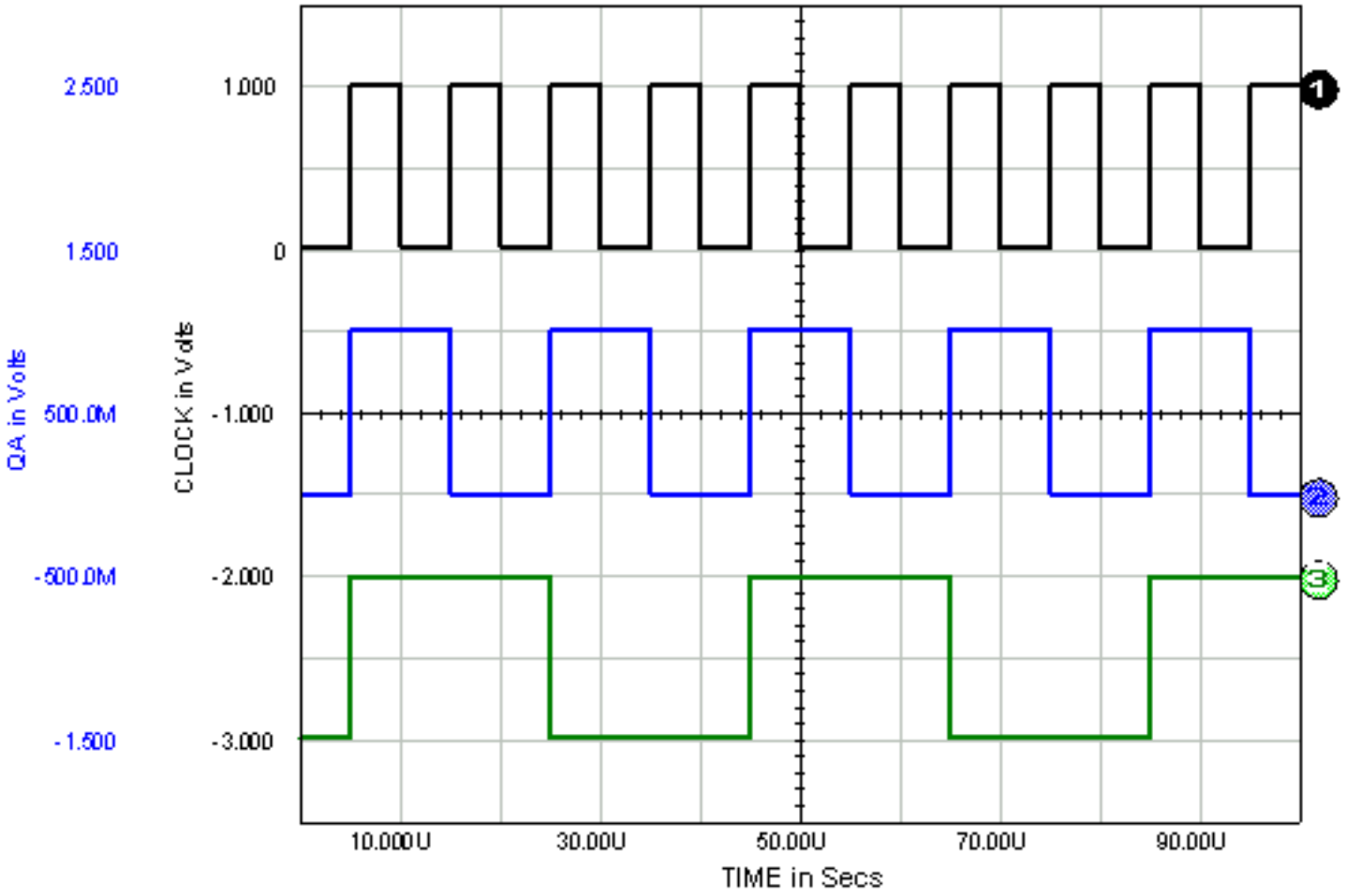
Markus, John, Ed. 1980. Modern Electric Circuit Reference Manual. McGraw Hill

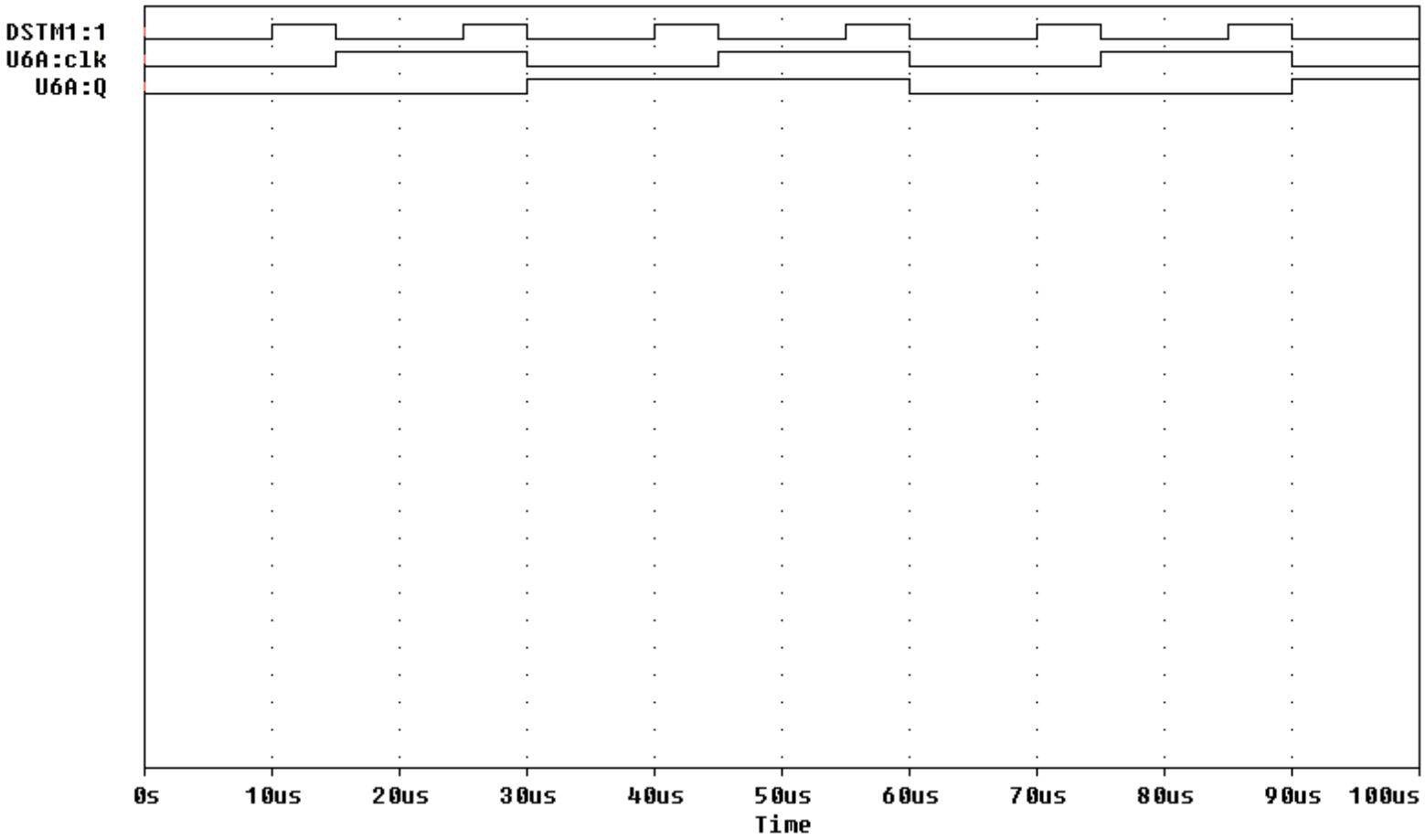
Radiation Hardened Product Databook 1993. Harris Semiconductor.

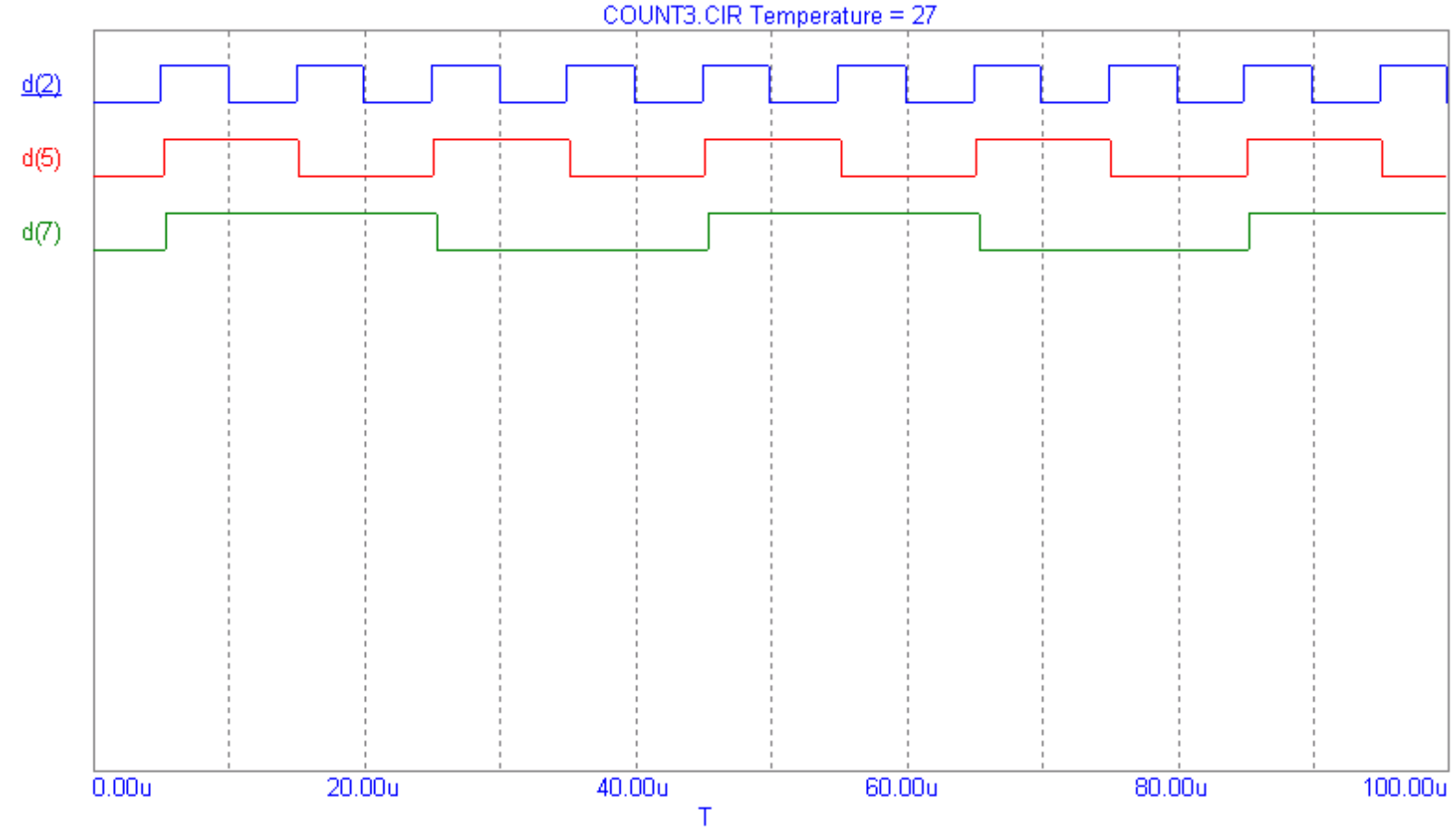

One
2
4
PR
J
Q
6
1
CLK
7
QN
K
CL
PR
J
Q
9
CLK
8
QN
K
CL
Clock
D
A
10
V(10)
CLOCK
Zero
D
A
12
D
A
13


V(12)
QA
V(13)
QB


Tek Run: 5MS/s Sample Trig'd
R2
1
2
Ch1 5 V Ch2 5 V M 10µs Ch2 ƒ 2.3 V
Ref2 5 V 10µs
19 Feb 1998
15:07:58


2.500
1.500
500.0M
-500.0M
-1.500
QA in Volts
1.000
0
-1.000
-2.000
-3.000
CLOCK in Volts
10.000U
30.00U
50.00U
70.00U
90.00U
TIME in Secs
1
2
3


DSTM1:1
U6A:clk
U6A:Q
0s
10us
20us
30us
40us
50us
60us
70us
80us
90us
100us
Time


COUNT3.CIR Temperature = 27
d(2)
d(5)
d(7)
0.00u
20.00u
40.00u
60.00u
80.00u
100.00u
T

#31: Set-Reset Latch

A latching circuit waits for an event to occur. Once that event occurs, the latch output changes state, and will ignore any further events until reset. This can be described as a memory element. The latch has many applications in the system. For example, if a failure mode in the system occurs, a shutdown signal may be sent to the latch circuit, which will shut down the system and prevent any further possible damage. The system will remain shut down until the power to the system is recycled.

The circuitry representation of the Set-Reset latch is shown in Figure 31-1. Not shown in the schematic is the power to the latch. A + 5 volt DC input was used to power the digital ICs.

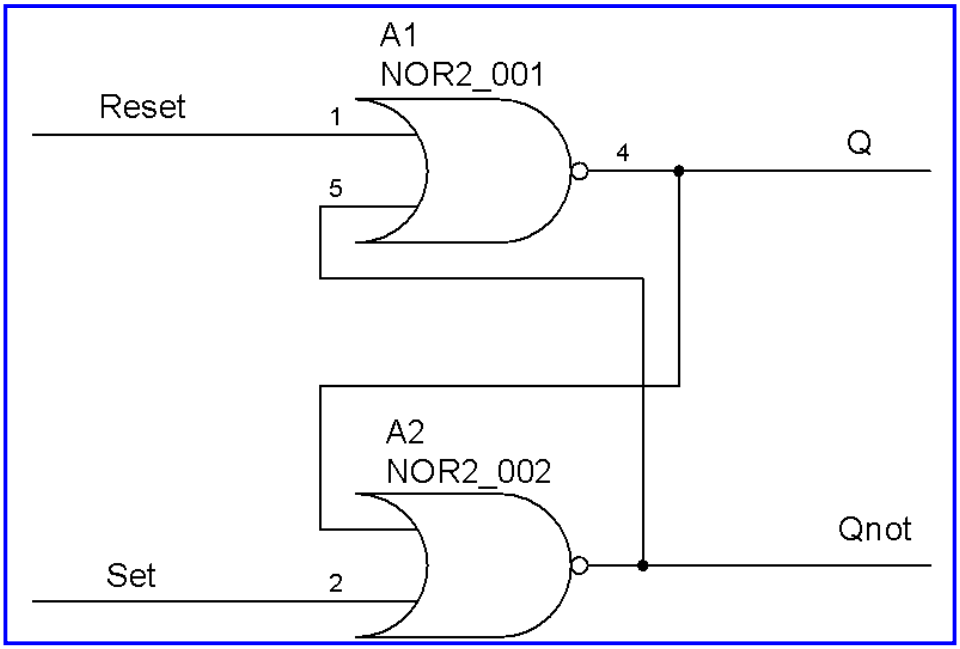


Figure 31-1: Schematic of a set-reset latch

The truth table for the set reset latch is shown in Table 31-1.

S	R	Q	Qnot	State
0	0	Q	Qnot	Unchanged

0	1	0	1	Reset
1	0	1	0	Set
1	1	0	0	Not allowed

Table 31-1: Truth table for set-reset flip flop

In order to show the performance of the set-reset flip flop, a series of were initiated. First, the reset pin of the flip flop was set high, then low. This allows the flip flop to read and react to a change of state event on the set pin. A pulse was then applied to the set pin. When the set pin transitioned from low to high, the output (Q) of the flip flop changed state from zero to one. Subsequent transitions on the set pin are now ignored by the flip flop. This is shown in the breadboard waveforms of Figure 31-2. The results of the IsSpice, Pspice, and Microcap simulations are shown in Figure 31-3 through 31-5.

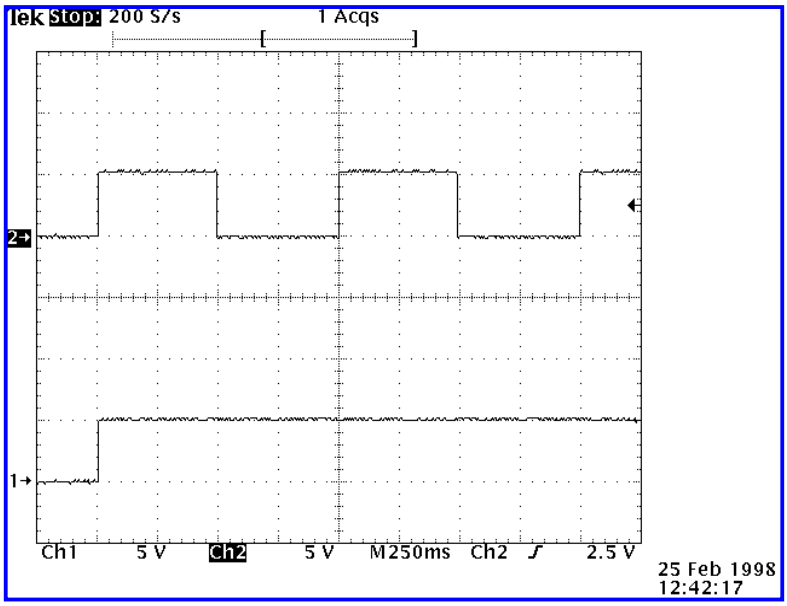


Figure 31-2: Breadboard output results (top - Set input, bottom - Q)

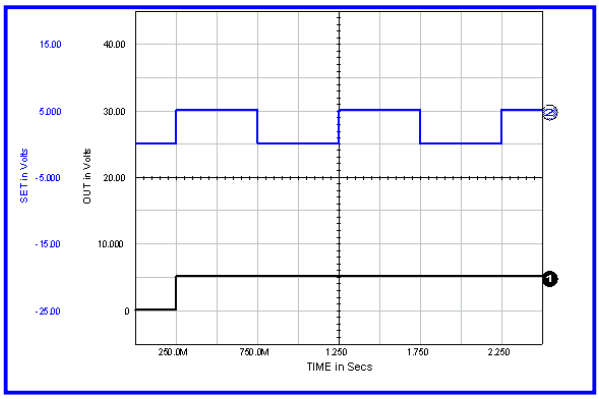


Figure 31-3: IsSpice output results (top - Set input, bottom - Q)

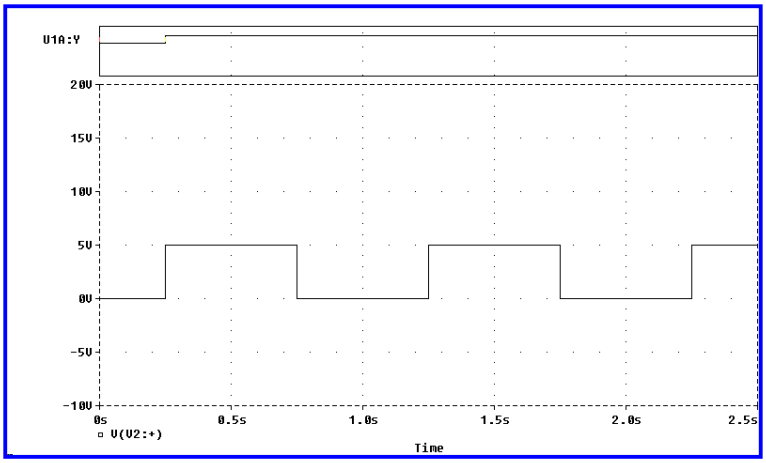


Figure 31-4: Pspice output results (top - Q, bottom - Set input)

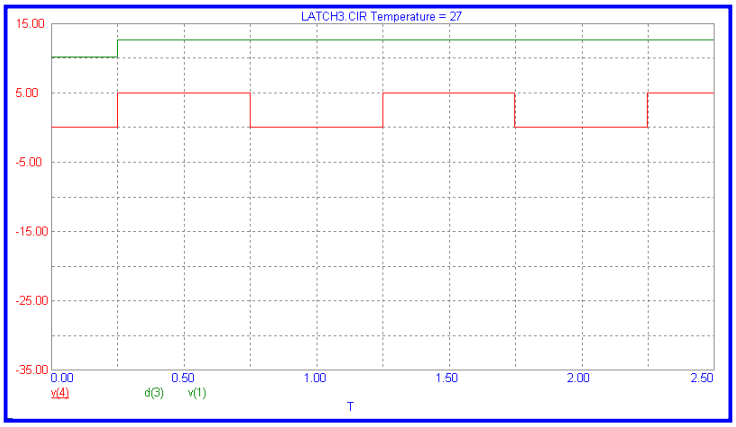


Figure 31-5: Microcap output results (top - Q, bottom - Set input)

Examining the results of Figure 31-2, we see the Q output transitioned from low to high when a low to high transition was detected on the set input. After being set high, the flip flop ignored any further activities of the Set pin. In order to return the Flip-Flop to the read state, the reset pin must be transitioned from low to high, then back to low again. This action will reset the Q output to zero and the flip flop will be ready to respond to the set input.

In order to model this in the SPICE programs, the set input was pulsed using an independent voltage source and the following command:

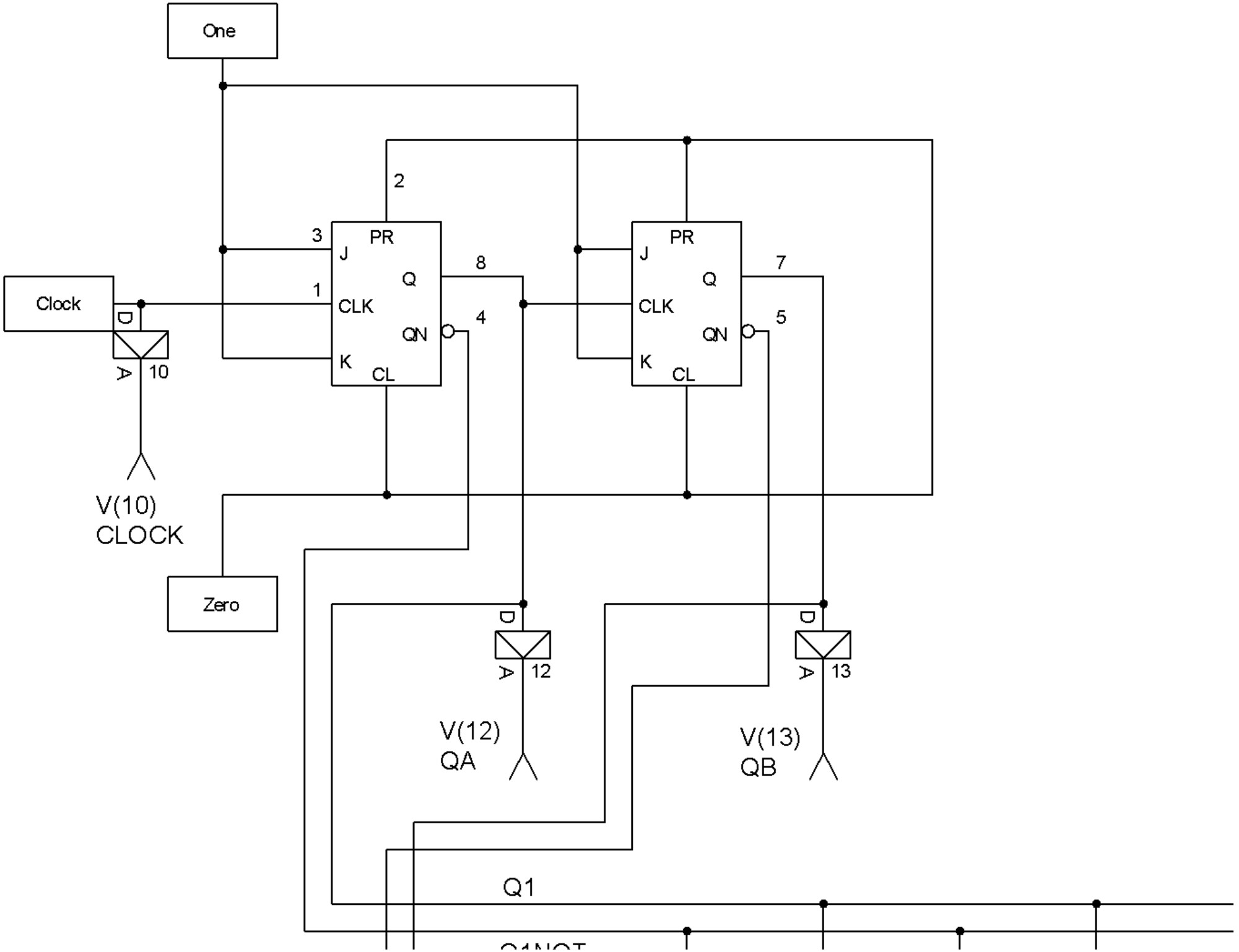
PULSE 0 5 250M 100U 100U 500M 1

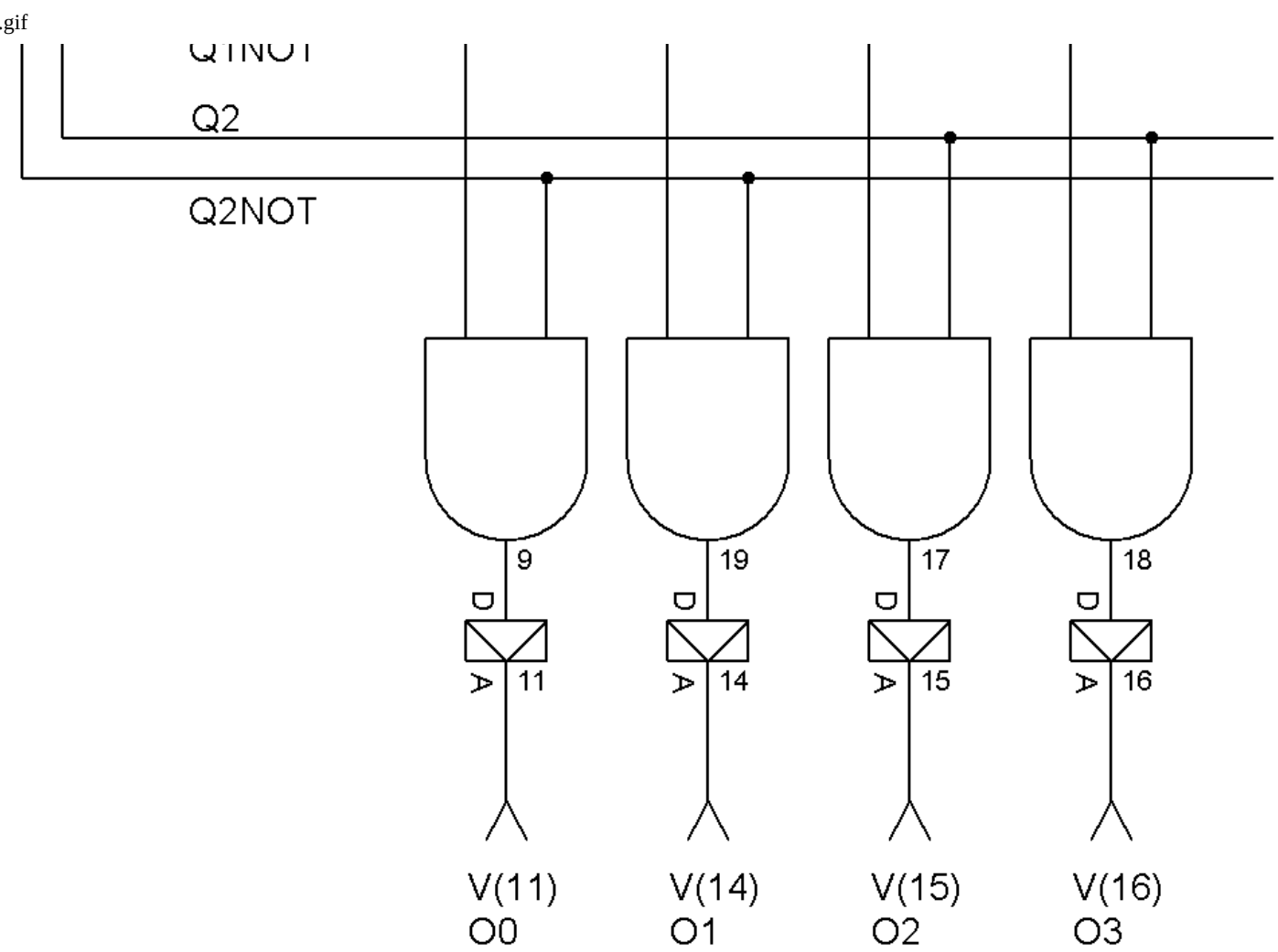
One interesting result of these simulations is the need for the digital circuits to be initialized. Each of the three simulators were run at different time lengths in order to accommodate this requirement of the simulators. If the initialization is not performed, some of the simulators will not be able to determine the output state.

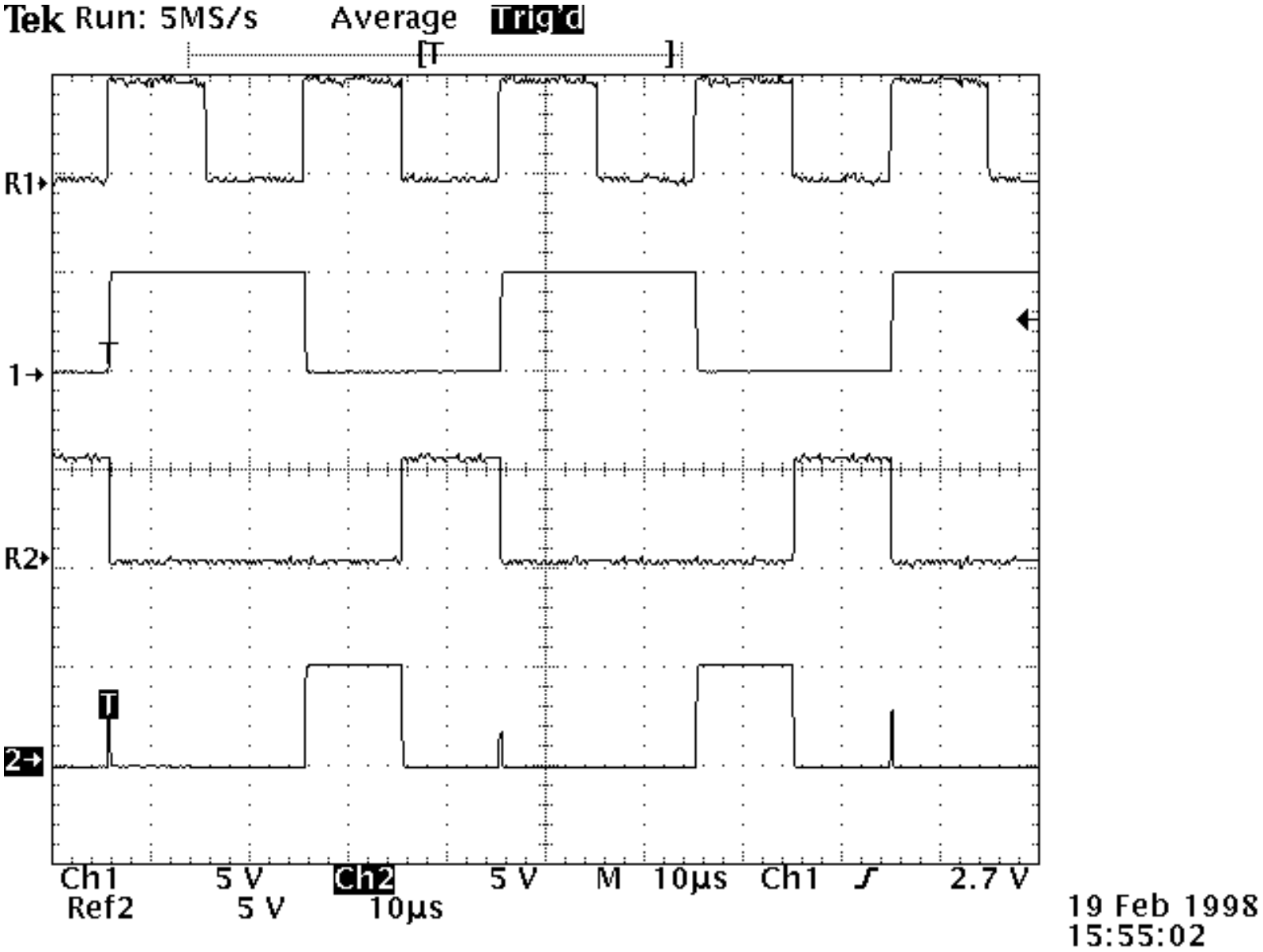
Run Time Summary		
IsSpice v 7.6	Pspice v 6.3	Micro-Cap V v2

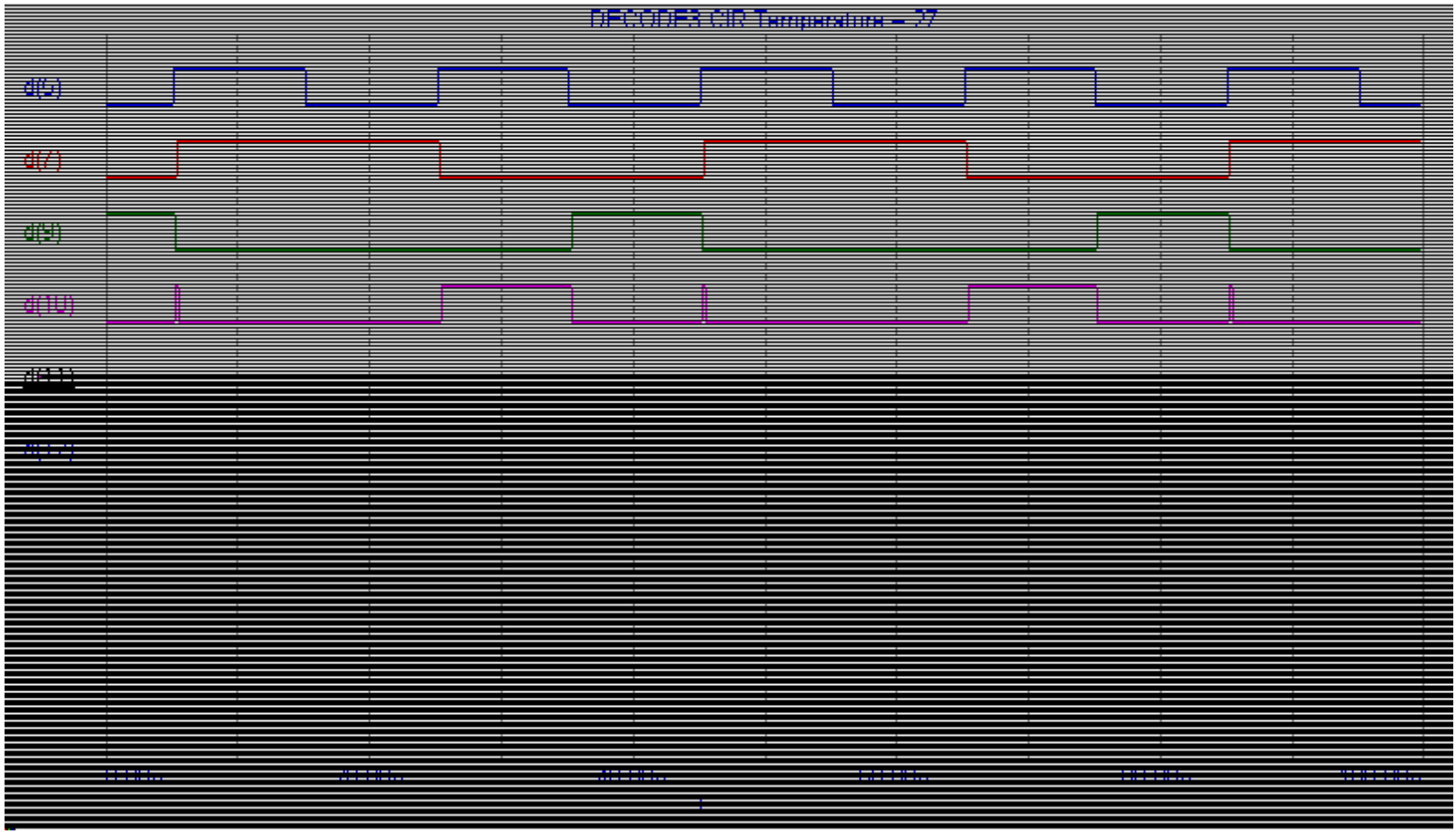
3.033 Sec	6.02 Sec	6.72 Sec
Advantages: Multiple applications		
Disadvantages: Set and Reset high state not allowed		

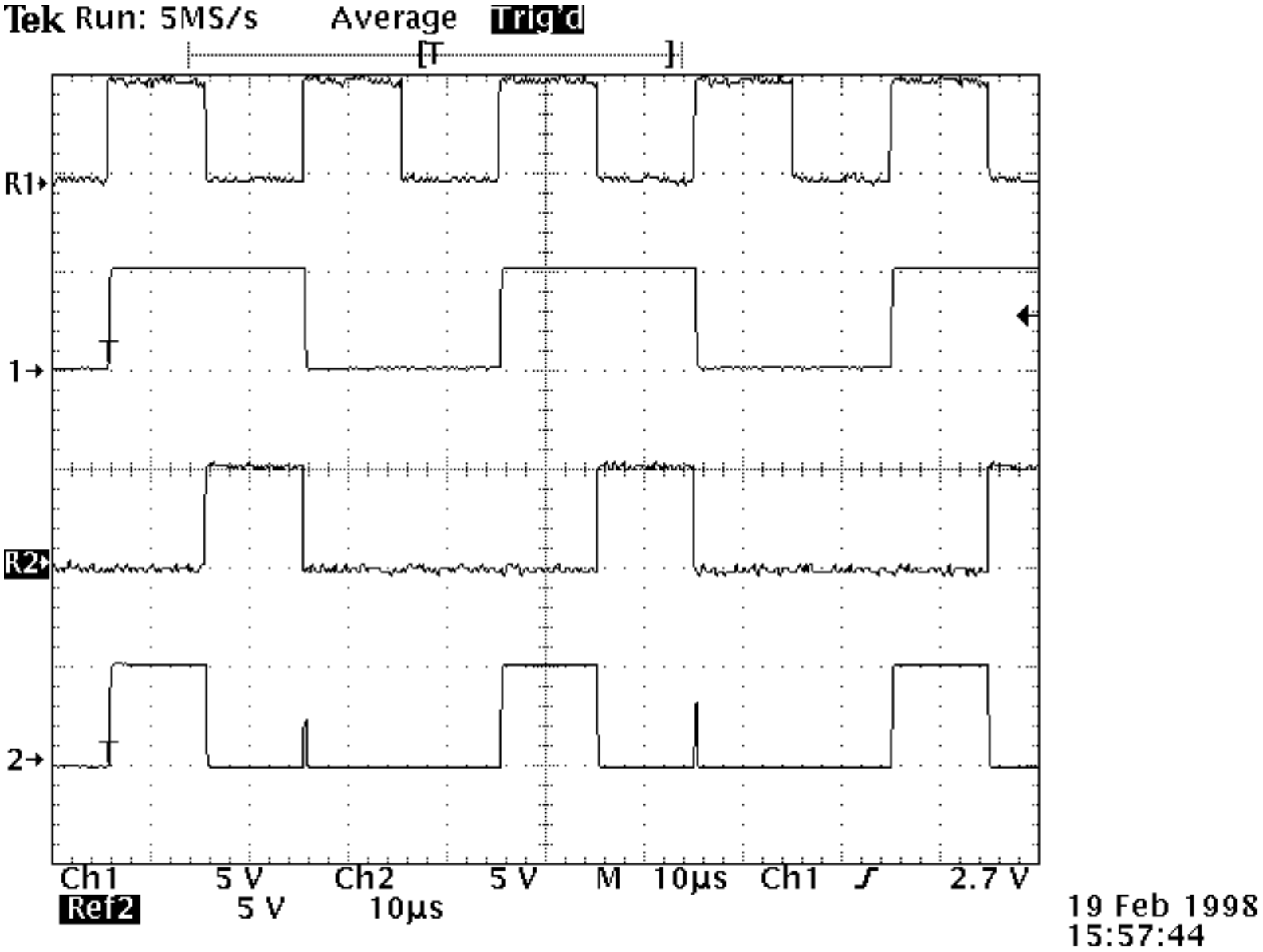
Filenames: latch (IsSpice) latch3 (Microcap) latch2 (Pspice)

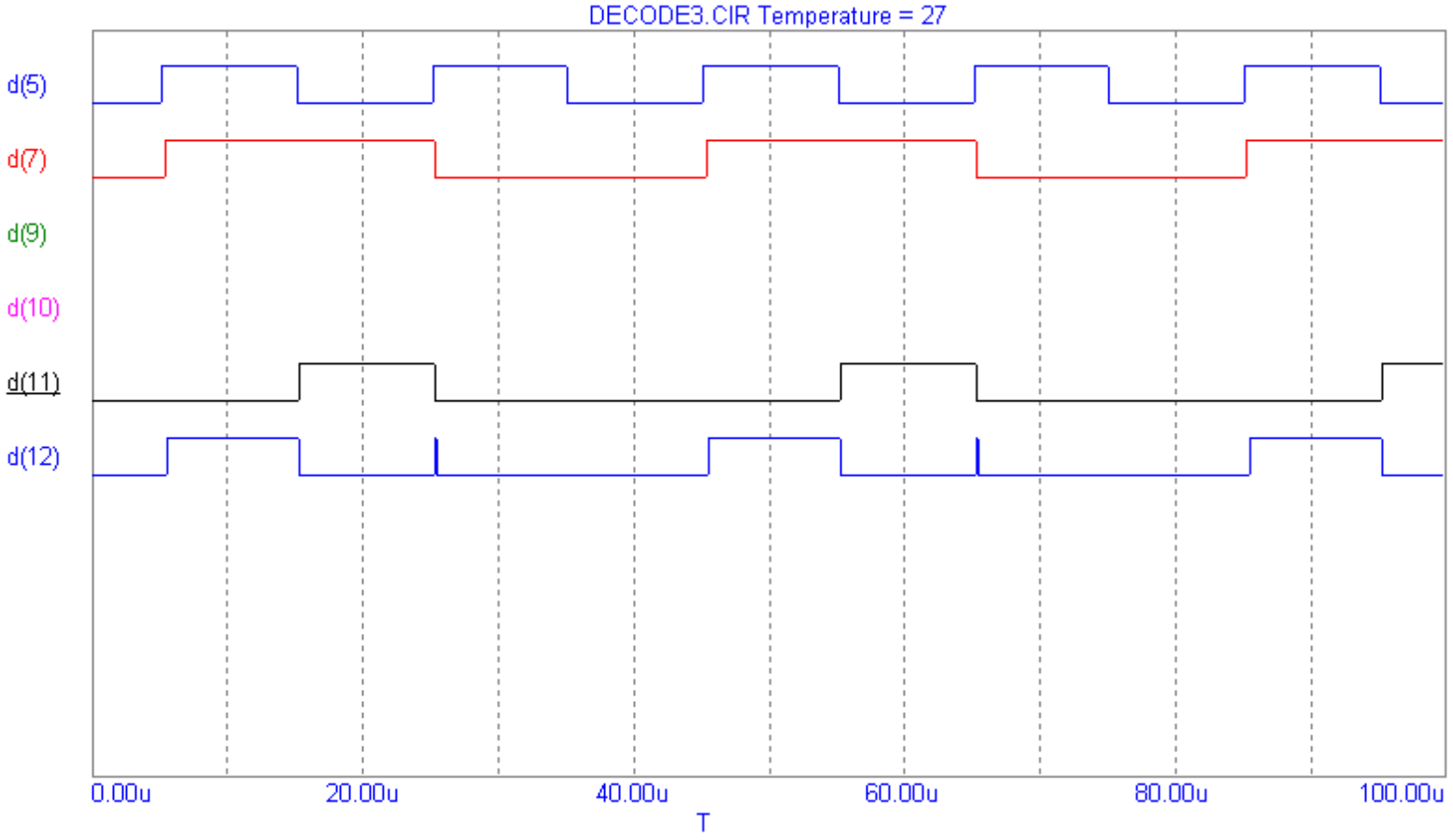

One
2
3
PR
J
Q
8
1
CLK
4
QN
K
CL
PR
J
Q
7
CLK
5
QN
K
CL
Clock
10
V(10)
CLOCK
Zero
12
13
V(12)
QA
V(13)
QB
Q1

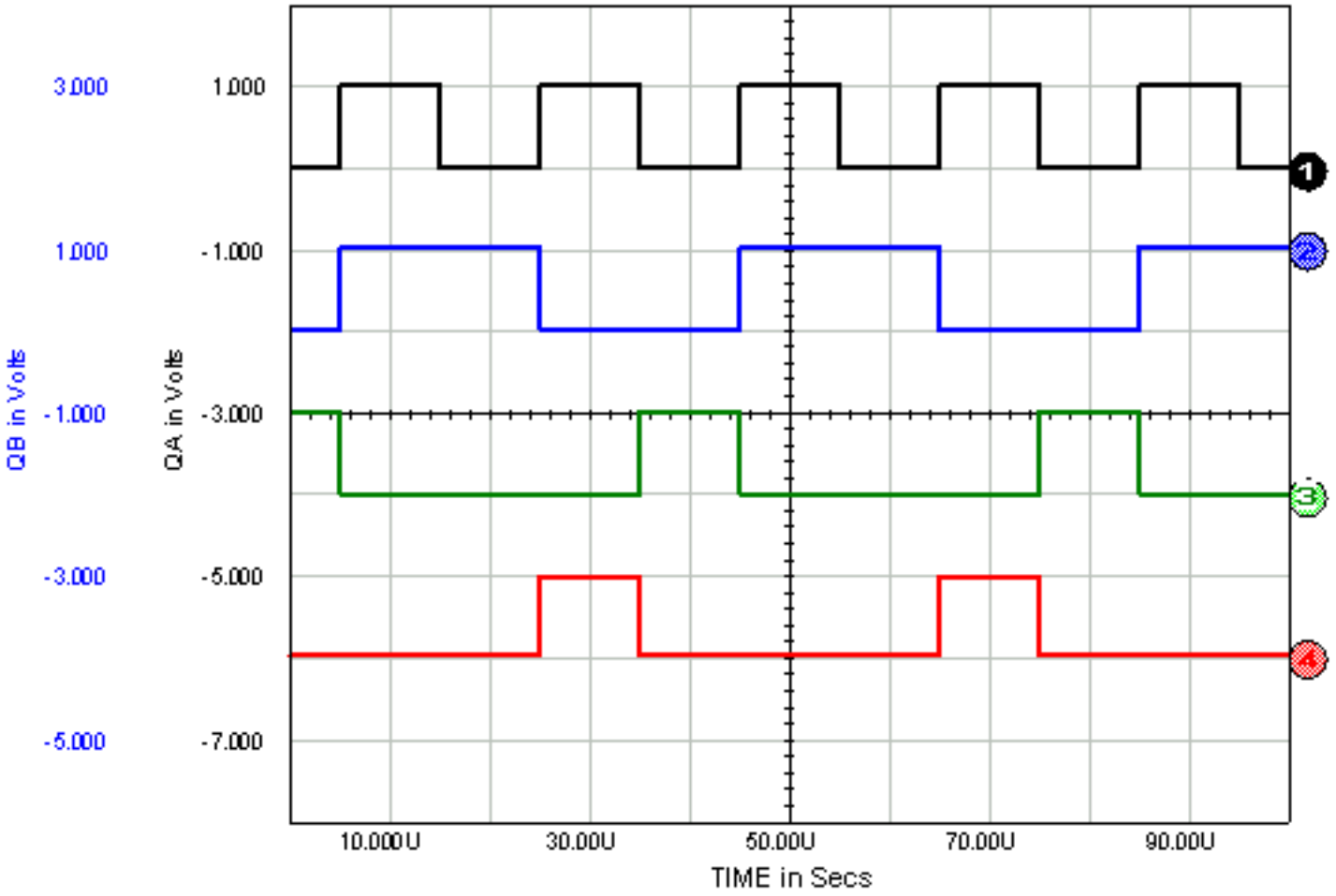

Q1NOT
Q2
Q2NOT
9
19
17
18
D
A
11
14
15
16
V(11)
O0
V(14)
O1
V(15)
O2
V(16)
O3

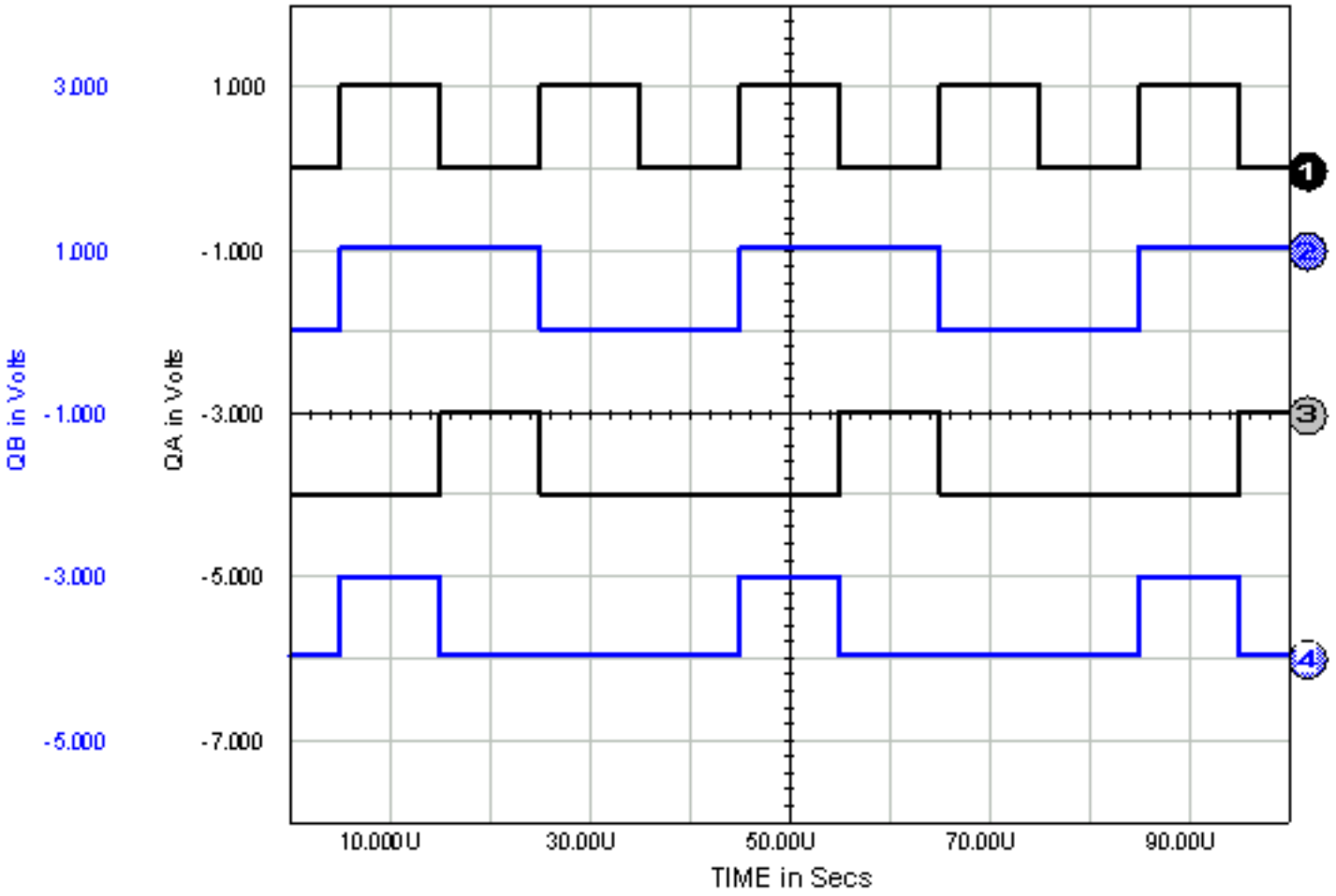

Tek Run: 5MS/s Average Trig'd
R1
1
R2
2
Ch1 5 V Ch2 5 V M 10µs Ch1 2.7 V
Ref2 5 V 10µs
19 Feb 1998
15:55:02

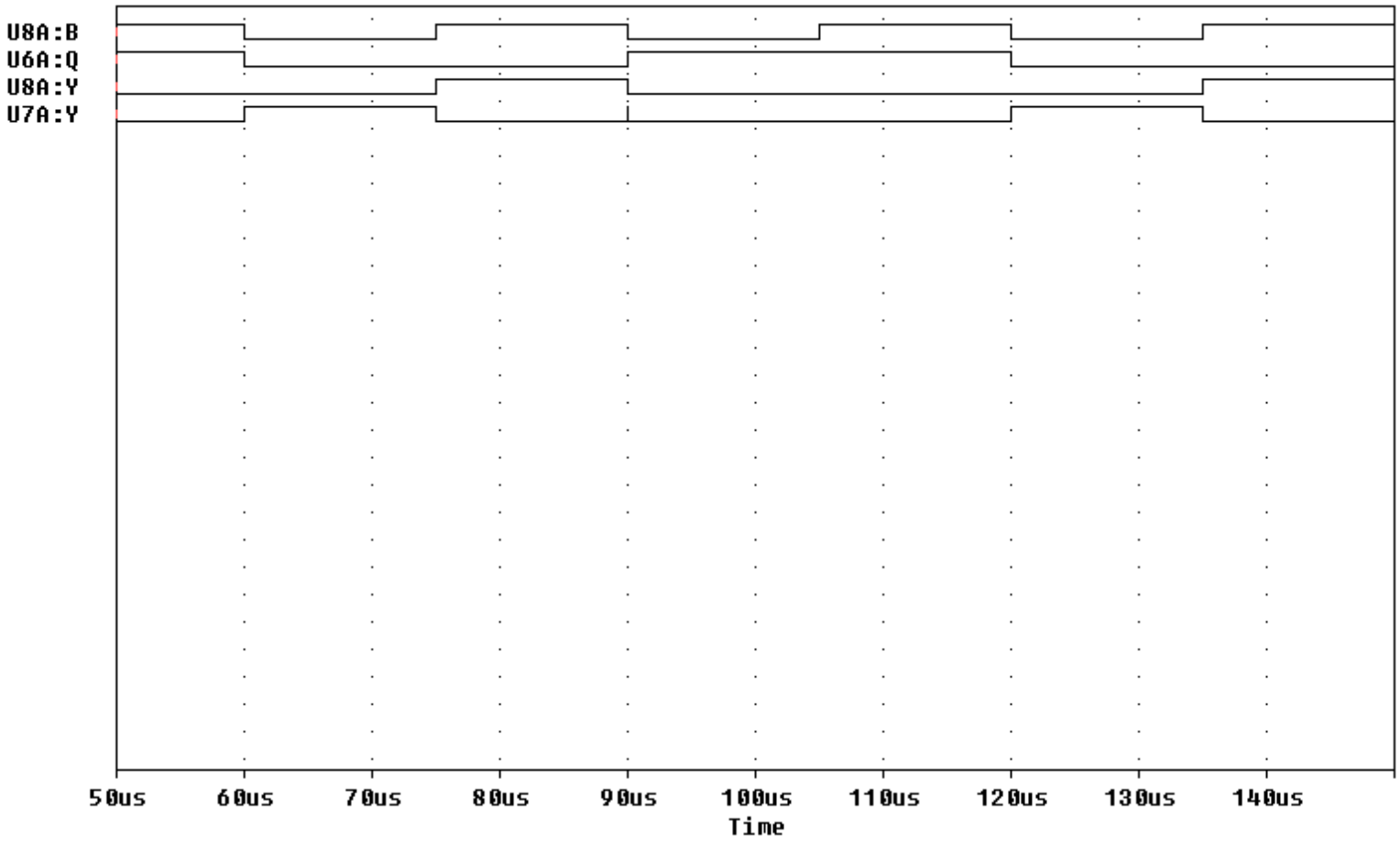

d(5)
d(7)
d(9)
d(10)

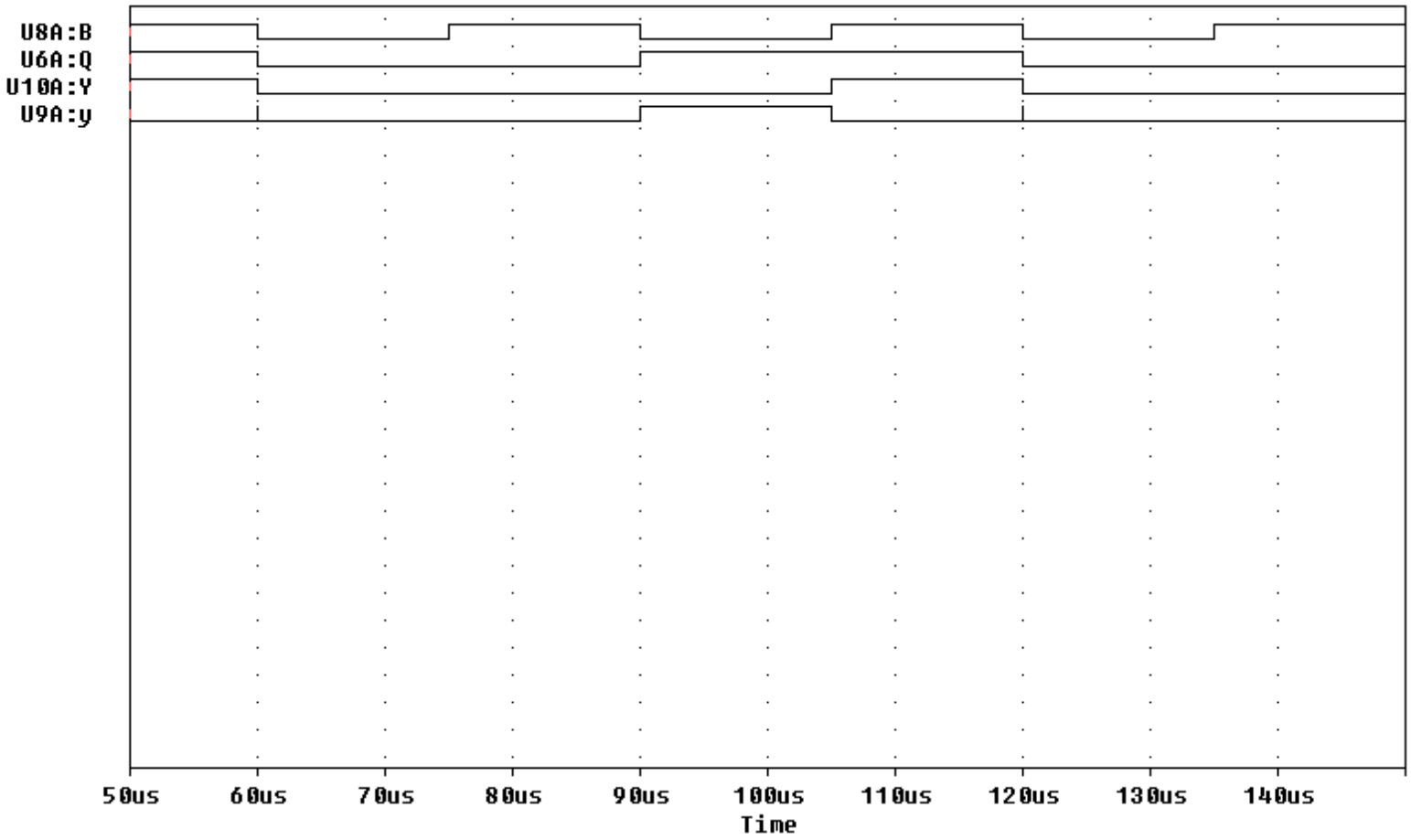

Tek Run: 5MS/s Average Trig'd
R1
1
R2
2
Ch1 5 V Ch2 5 V M 10µs Ch1 2.7 V
Ref2 5 V 10µs
19 Feb 1998
15:57:44


DECODE3.CIR Temperature = 27
d(5)
d(7)
d(9)
d(10)
d(11)
d(12)
0.00u
20.00u
40.00u
60.00u
80.00u
100.00u
T


3.000
1.000
-1.000
-3.000
-5.000
QB in Volts
1.000
-1.000
-3.000
-5.000
-7.000
QA in Volts
10.000U
30.00U
50.00U
70.00U
90.00U
TIME in Secs
1
2
3
4


3.000
1.000
-1.000
-3.000
-5.000
QB in Volts
1.000
-1.000
-3.000
-5.000
-7.000
QA in Volts
10.000U
30.00U
50.00U
70.00U
90.00U
TIME in Secs
1
2
3
4


U8A:B
U6A:Q
U8A:Y
U7A:Y
50us
60us
70us
80us
90us
100us
110us
120us
130us
140us
Time


U8A:B
U6A:Q
U10A:Y
U9A:y
50us
60us
70us
80us
90us
100us
110us
120us
130us
140us
Time

#32: Staircase Generator

Staircase generator circuits have important applications in video systems. There are several ways to generate staircase waveforms, using either analog or digital design methods. This circuit investigates the digital solution to the staircase generator.

The schematic for the staircase generator circuit is shown in Figure 32-1. Not shown in the schematic is the power to the J-K flip flops and the AND gate. A + 5 volt DC input was used to power the digital ICs.

The staircase waveform starts after the clear signal is received by the J-K flip flops. The clear signal sets all Q outputs to a zero state and all QNOT outputs to a one state. With the set pin tied low and the J pin tied high, when a low to high clock transition is detected, the Q output will transition from low to high. The Q output is tied to the J pin of the next flip flop, so one clock cycle later, the Q output transitions from low to high, and so on. When the final J-K flip flop stage Q output transitions high, the AND gate clears the flip flops and starts the cycle over again. The four staggered signals from the Q output of the first four flip flops are summed in an Op-amp adder circuit and the result is the repeating staircase waveform.

The clock in Figure 32-1 is set at 1 Khz with a 50 % duty cycle.

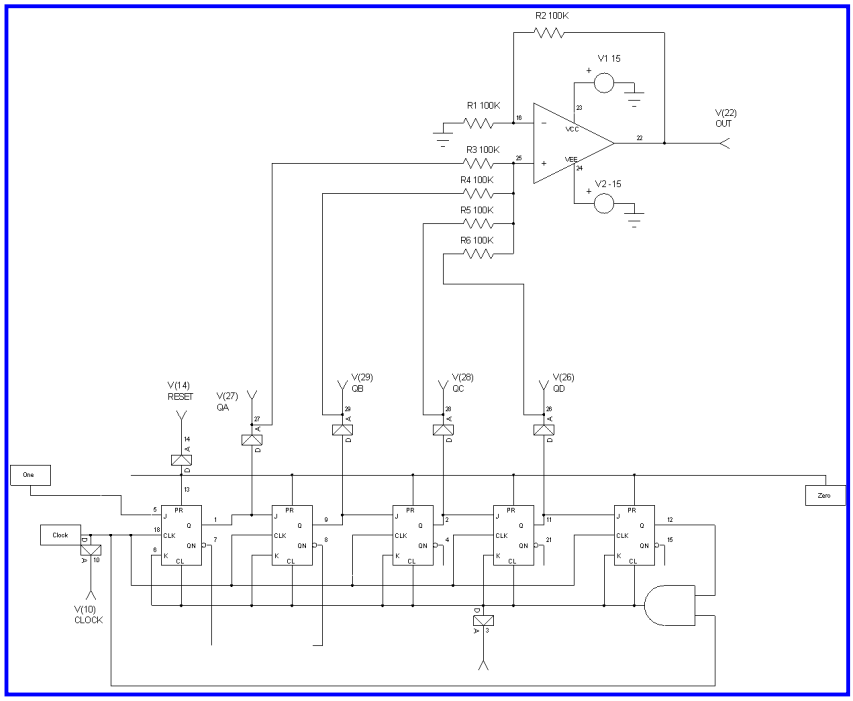


Figure 32-1: Schematic of Staircase Generator

The staircase generator circuit was constructed in all three simulators and in the lab using real components. The breadboard used a UA723 for the Op-amp, CD4027 for the J-K flip flops, and a CD4081 for the AND gate.

The breadboard staggered Q outputs of the first four J-K flip flops are shown in Figure 32-2. The results of the IsSpice simulator are shown in Figure 32-3. The Microcap results are shown in Figure 32-4, and the Pspice results are shown in Figure 32-5.

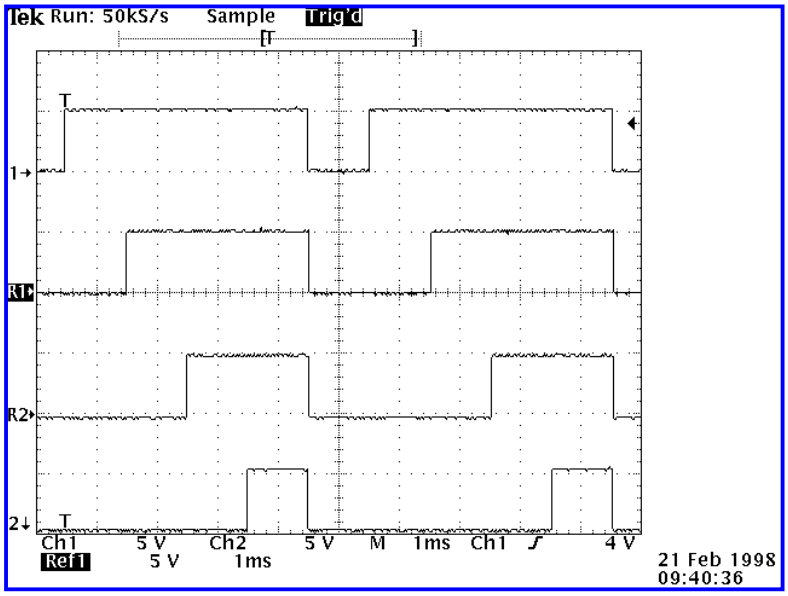


Figure 32-2: Breadboard output results (Q outputs)

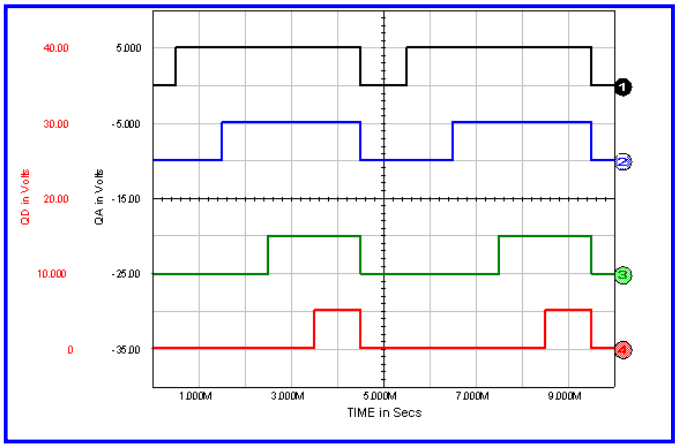


Figure 32-3: IsSpice output results (Q outputs)

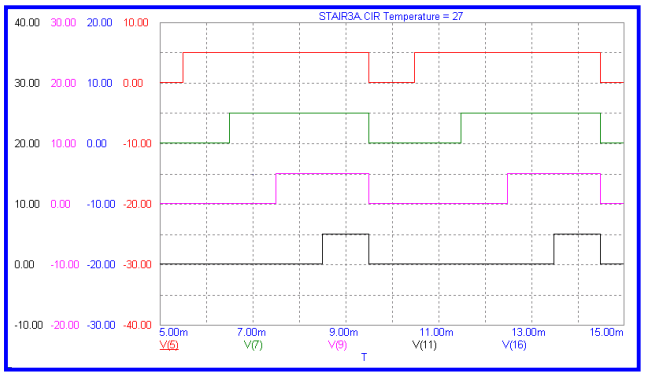


Figure 32-4: Microcap output results (Q outputs)

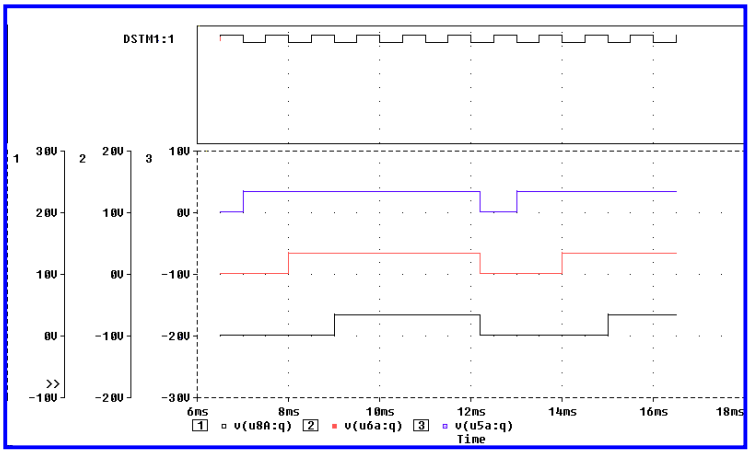


Figure 32-5: Pspice output results (Q outputs)

Note: the Pspice results are shown in a slightly different configuration due to the PROBE output program. Three of the four Q output waveforms are shown in the lower section of the plot, while the clock is shown at the top.

The outputs shown in Figures 32-2 through 32-5 were summed using the Operational Amplifier adder circuit featured in circuit # 37. The results of the breadboard are shown in Figure 32-6, with the clock at the top, and the staircase waveform at the bottom. The IsSpice, Microcap, and Pspice results are shown in Figures 32-7, 32-8, and 32-9 respectively.

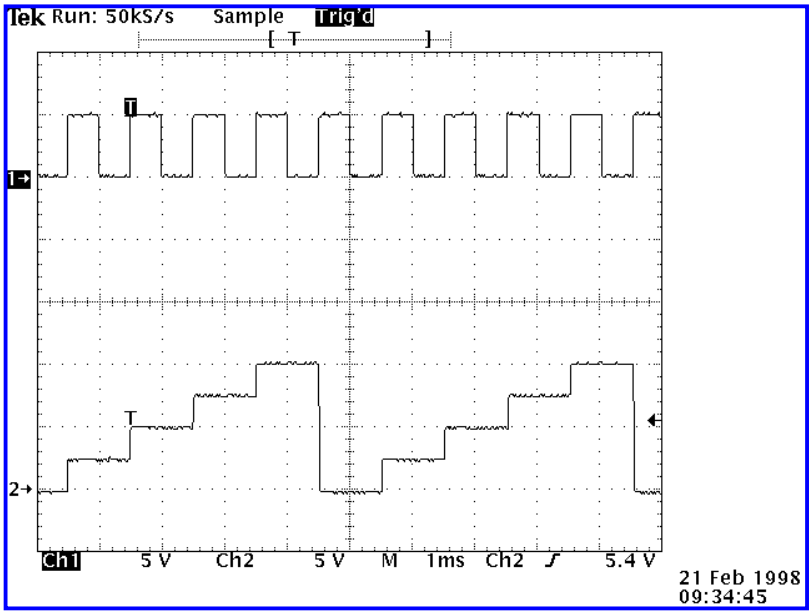


Figure 32-6: Staircase Waveform breadboard results

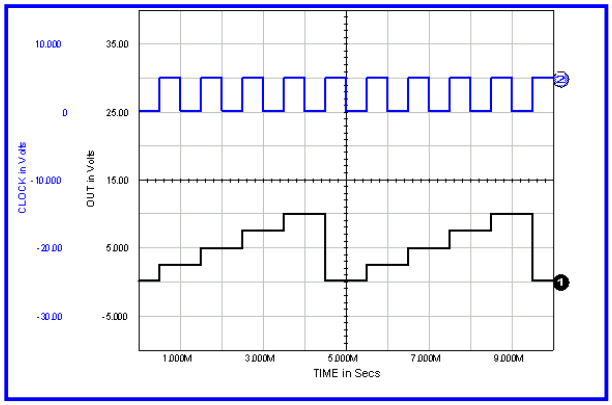


Figure 32-7: Staircase waveform IsSpice results

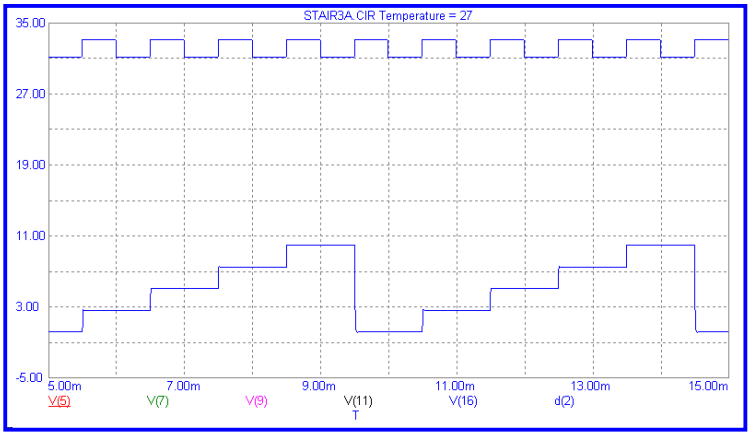


Figure 32-8: Microcap results

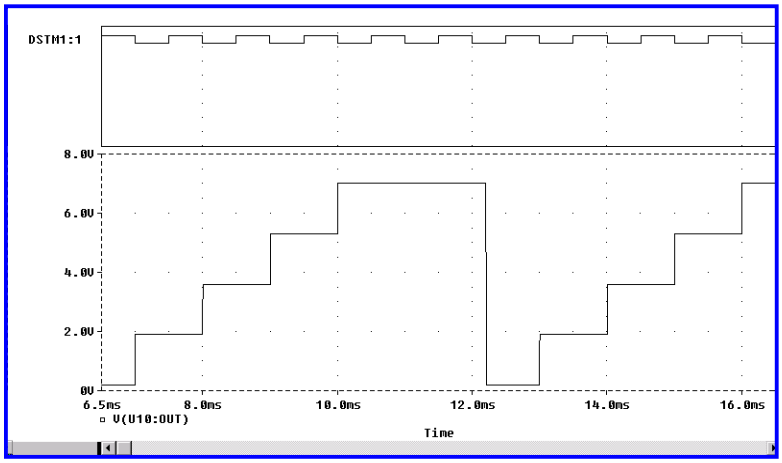


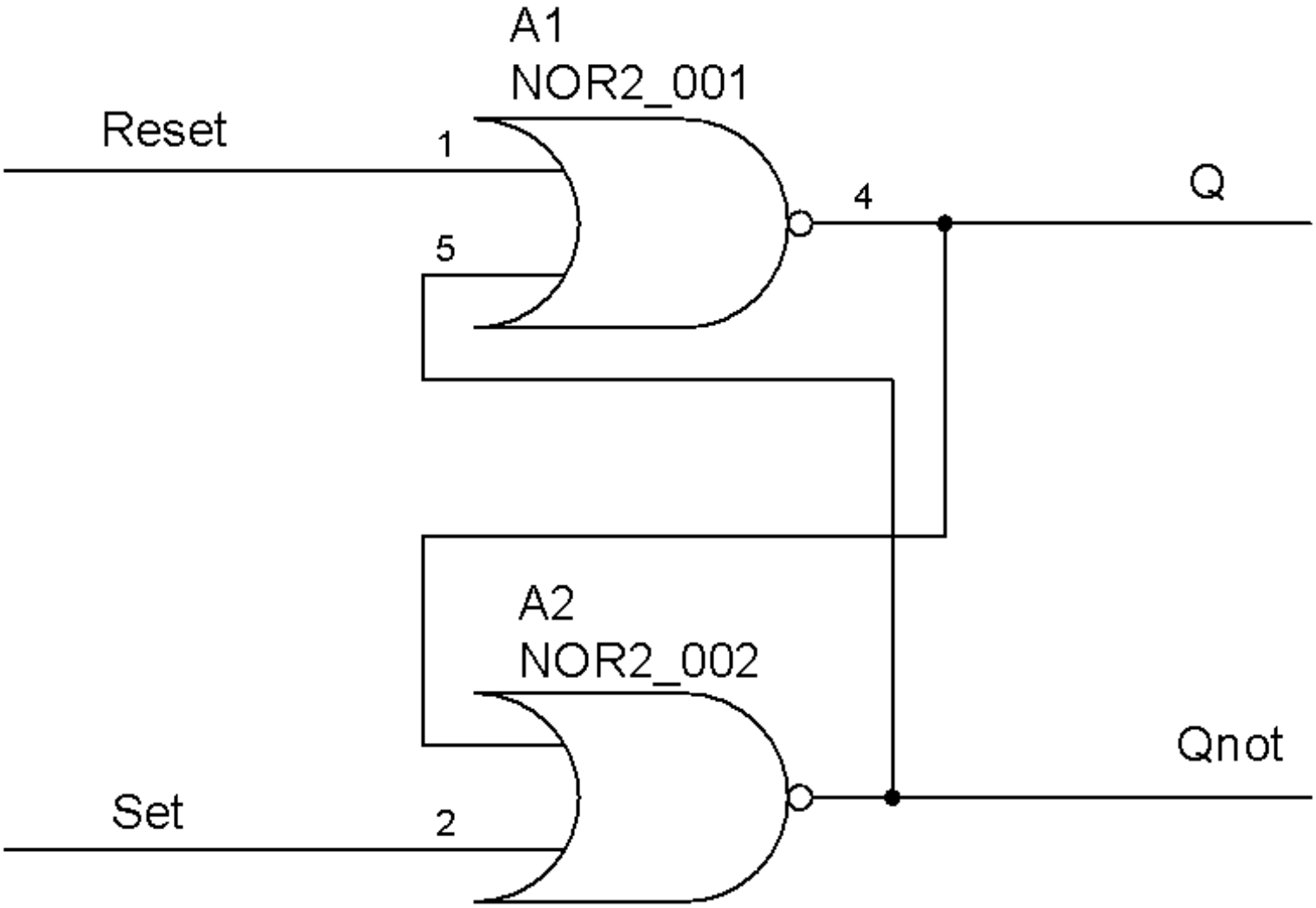
Figure 32-9: Pspice results

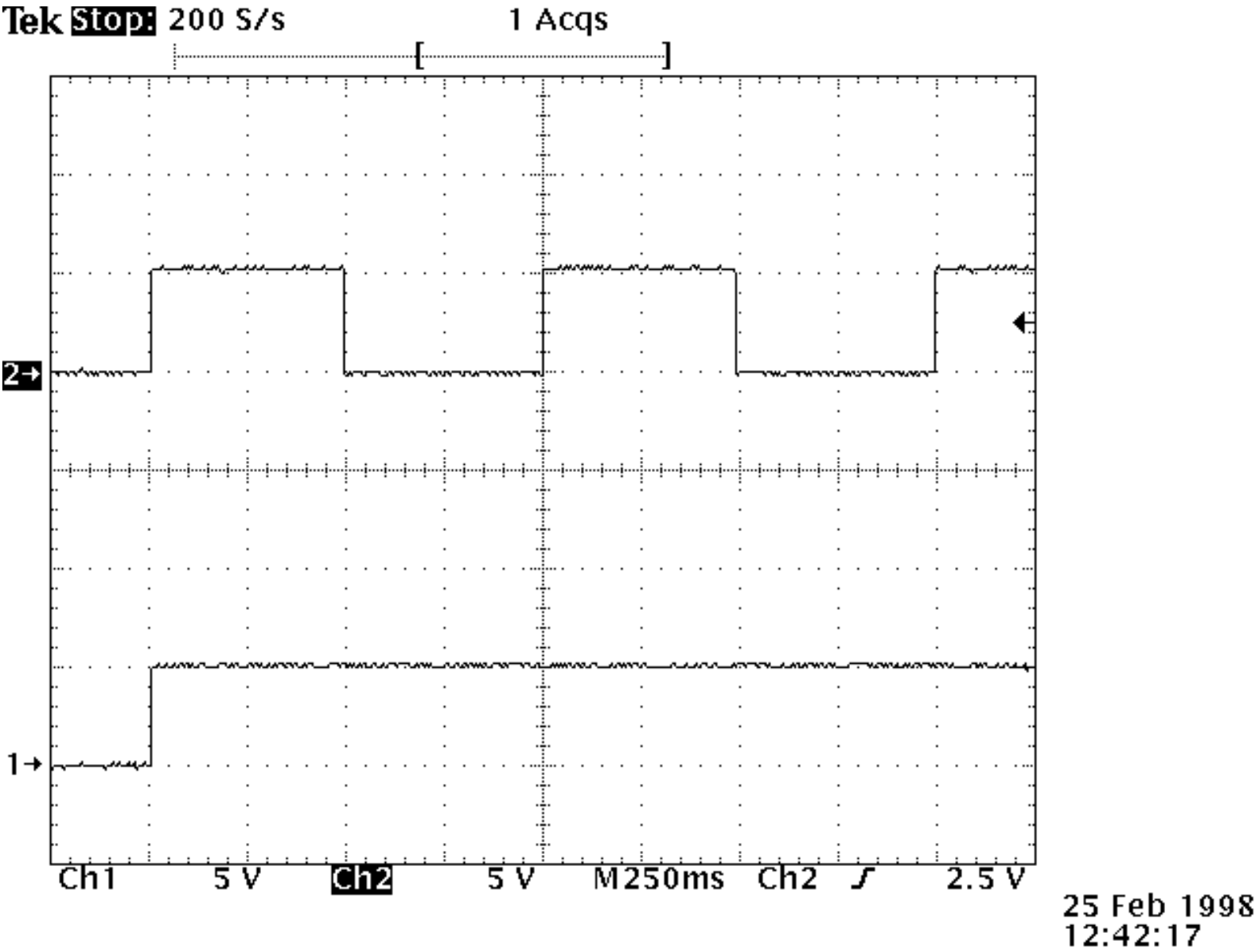
In order to run this simulation using the evaluation version of Pspice, it was necessary to remove the AND gate and one of the J-K flip flops from the circuit. With these components included, the number of digital parts was exceeded for the evaluation version and the schematic would not simulate. These two parts were replaced by a stimulus source with performed the same function as these two components.

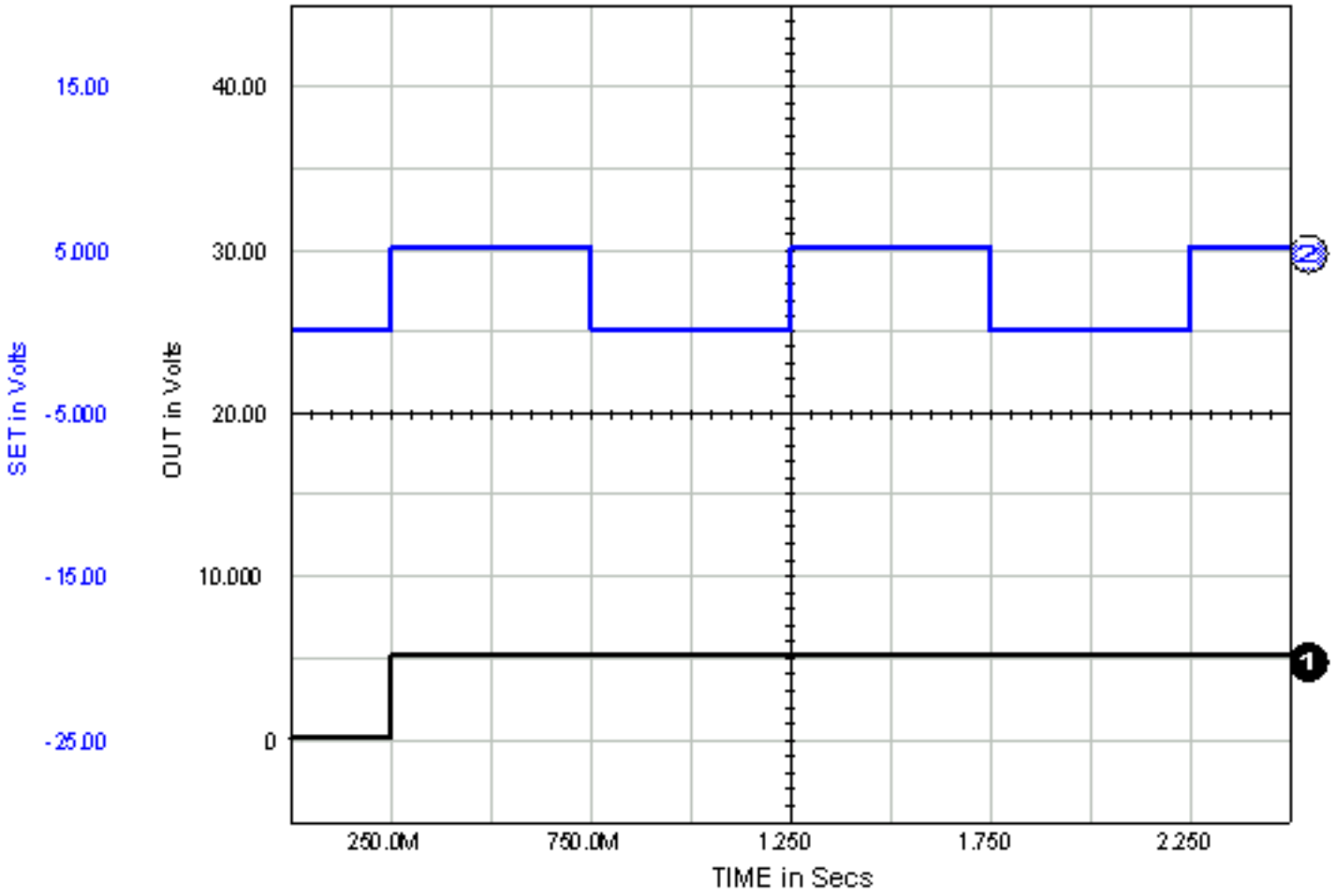
One interesting result of these simulations is the need for the digital circuits to be initialized. Each of the three simulators were run at different time lengths in order to accommodate this requirement of the simulators. If the initialization is not performed, some of the simulators will not be able to determine the output state.

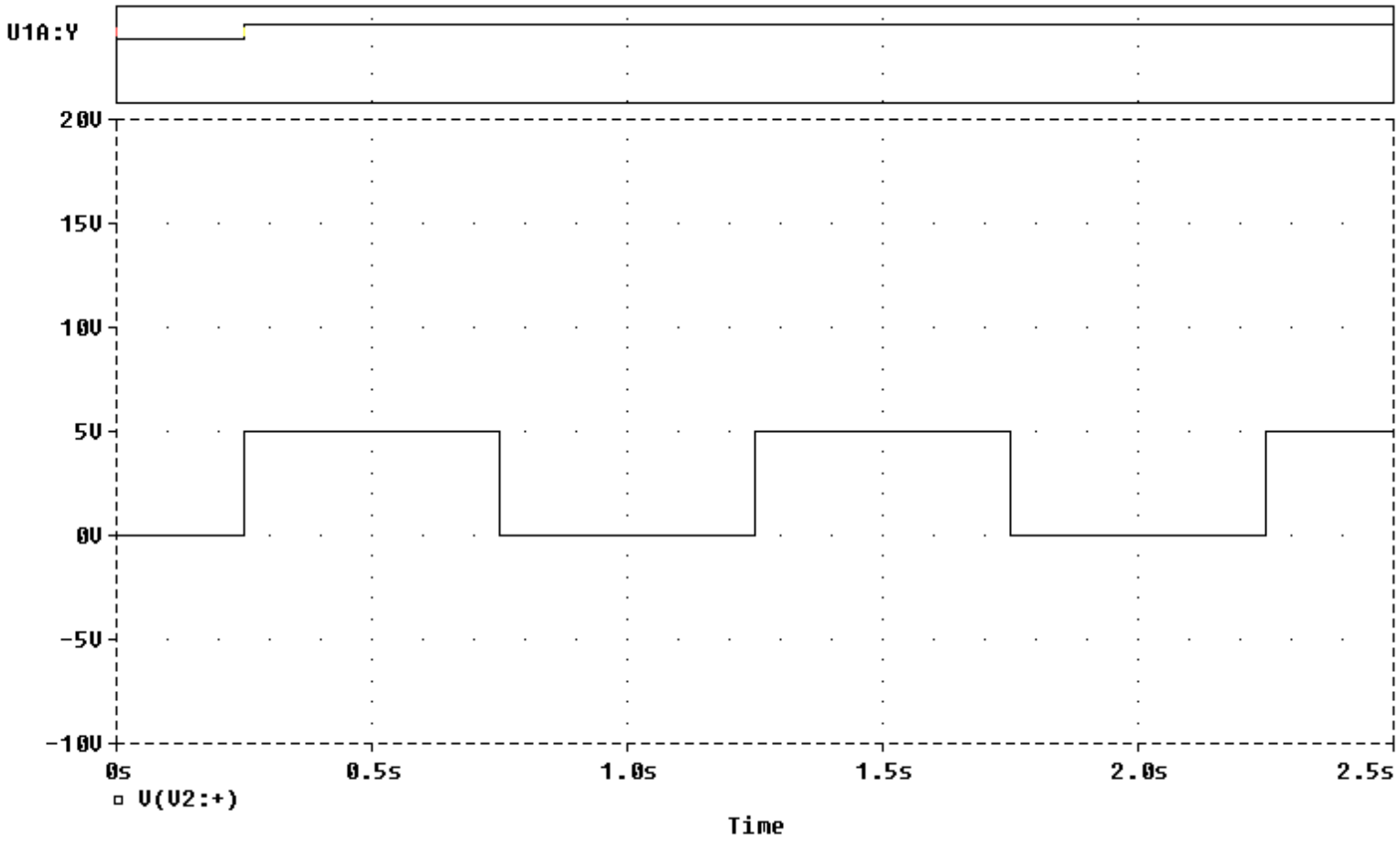
Run Time Summary		
IsSpice v 7.6	Pspice v 6.3	Micro-Cap V v2
3.833 Sec	13.15 Sec	31.23 Sec
Advantages: Applicable for multiple frequency input signals		
Disadvantages: Can be realized with fewer parts		

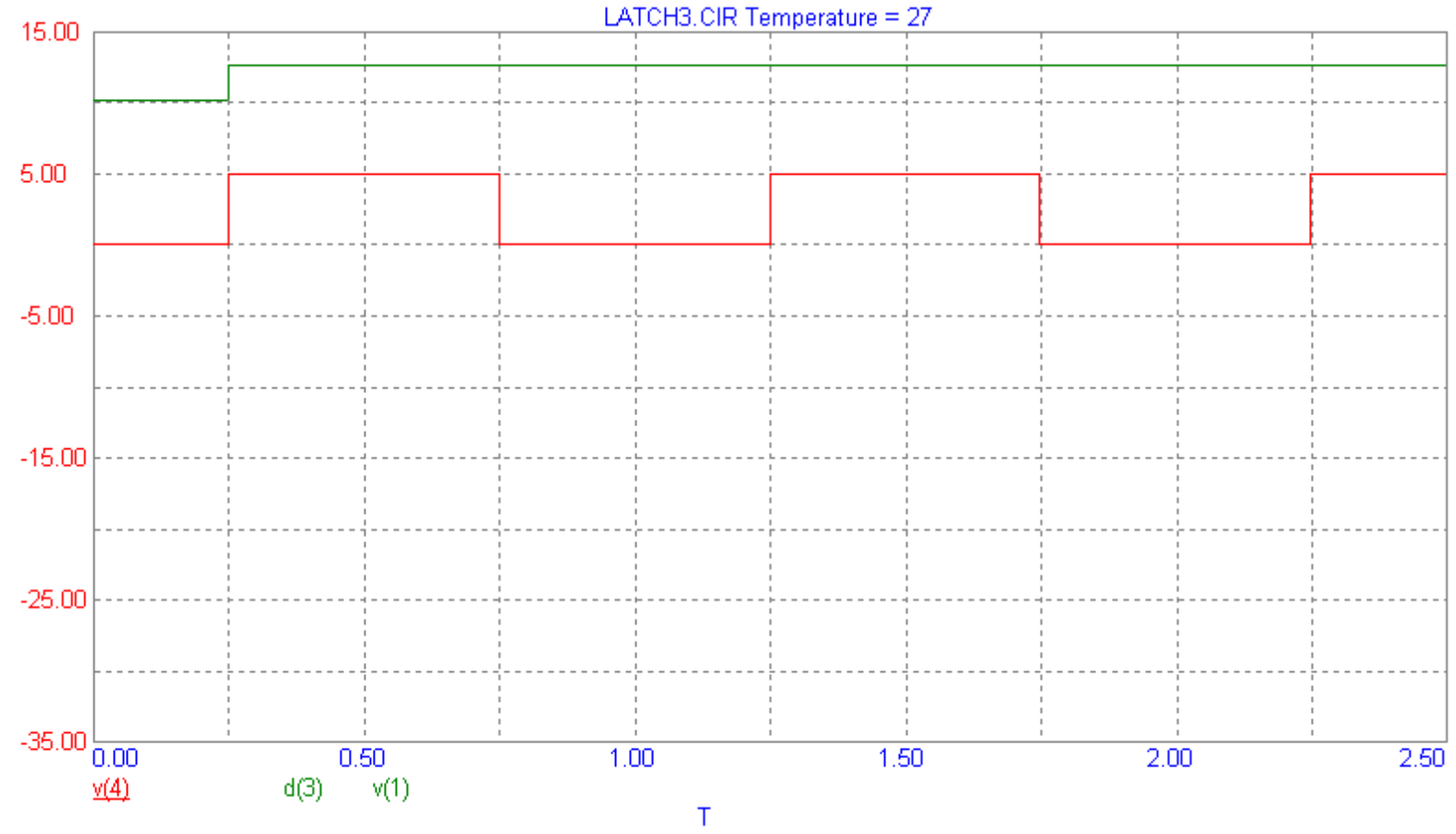
Filenames: stair (IsSpice) stair2 (Microcap) stair3a (Pspice)


A1
NOR2_001
Reset
1
5
4
Q
A2
NOR2_002
Qnot
Set
2


Tek Stop: 200 S/s
1 Acqs
2→
1→
Ch1 5 V Ch2 5 V M250ms Ch2 ƒ 2.5 V
25 Feb 1998
12:42:17


15.00
5.000
-5.000
-15.00
-25.00
SET in Volts
40.00
30.00
20.00
10.000
0
OUT in Volts
250.0M
750.0M
1.250
1.750
2.250
TIME in Secs
2
1

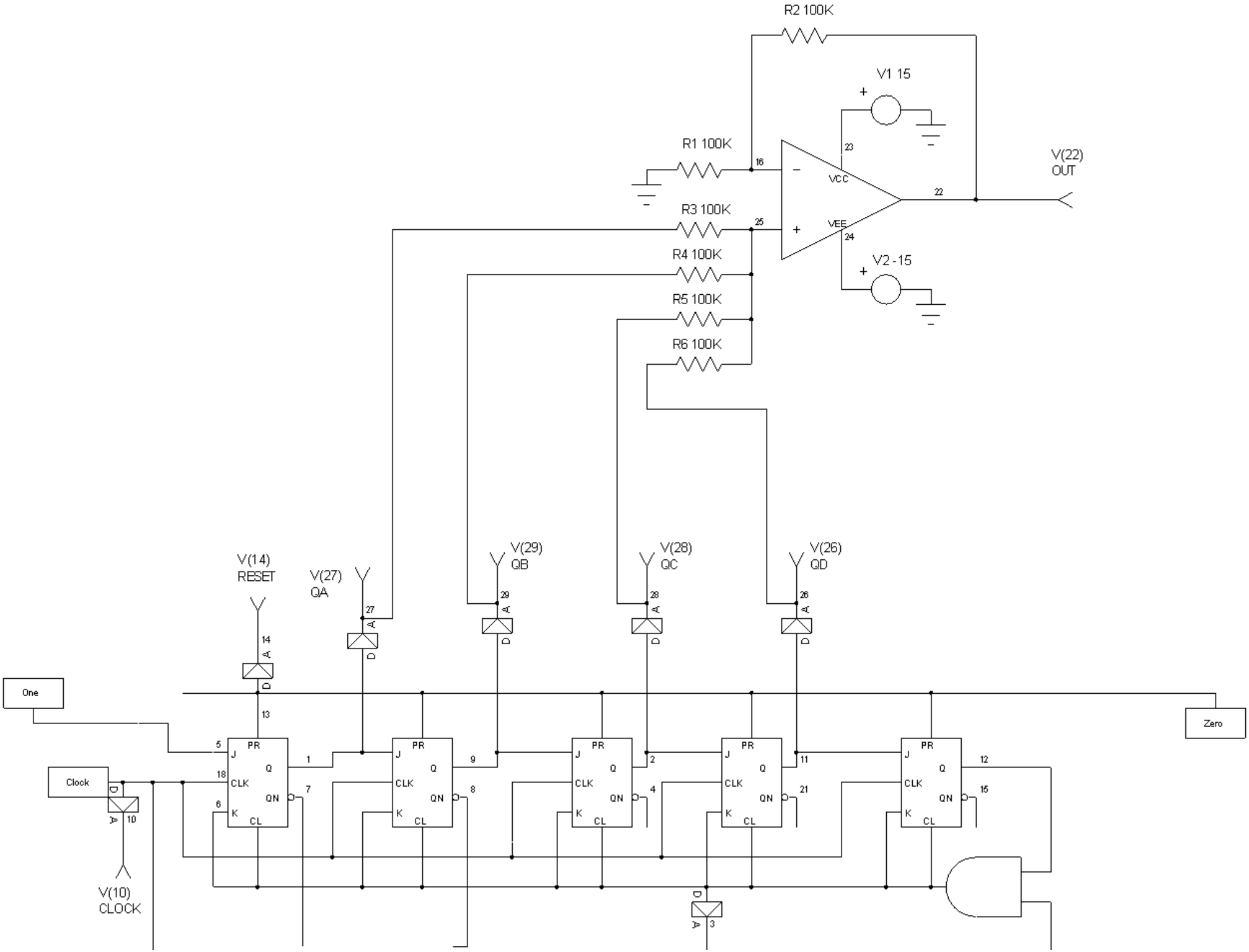

U1A:Y
20V
15V
10V
5V
0V
-5V
-10V
0s
0.5s
1.0s
1.5s
2.0s
2.5s
V(V2:+)
Time

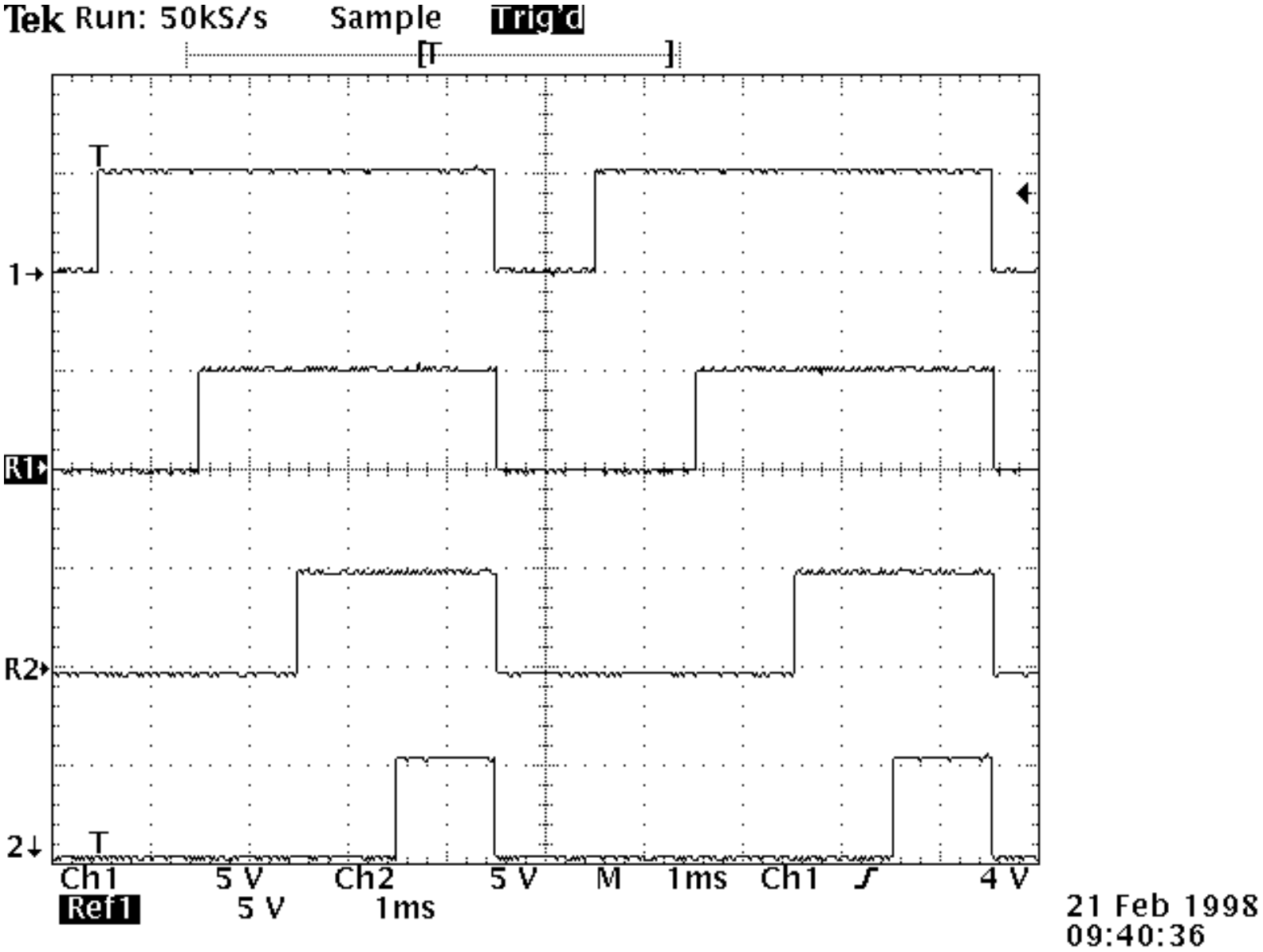

LATCH3.CIR Temperature = 27
15.00
5.00
-5.00
-15.00
-25.00
-35.00
0.00
0.50
1.00
1.50
2.00
2.50
v(4)
d(3)
v(1)
T

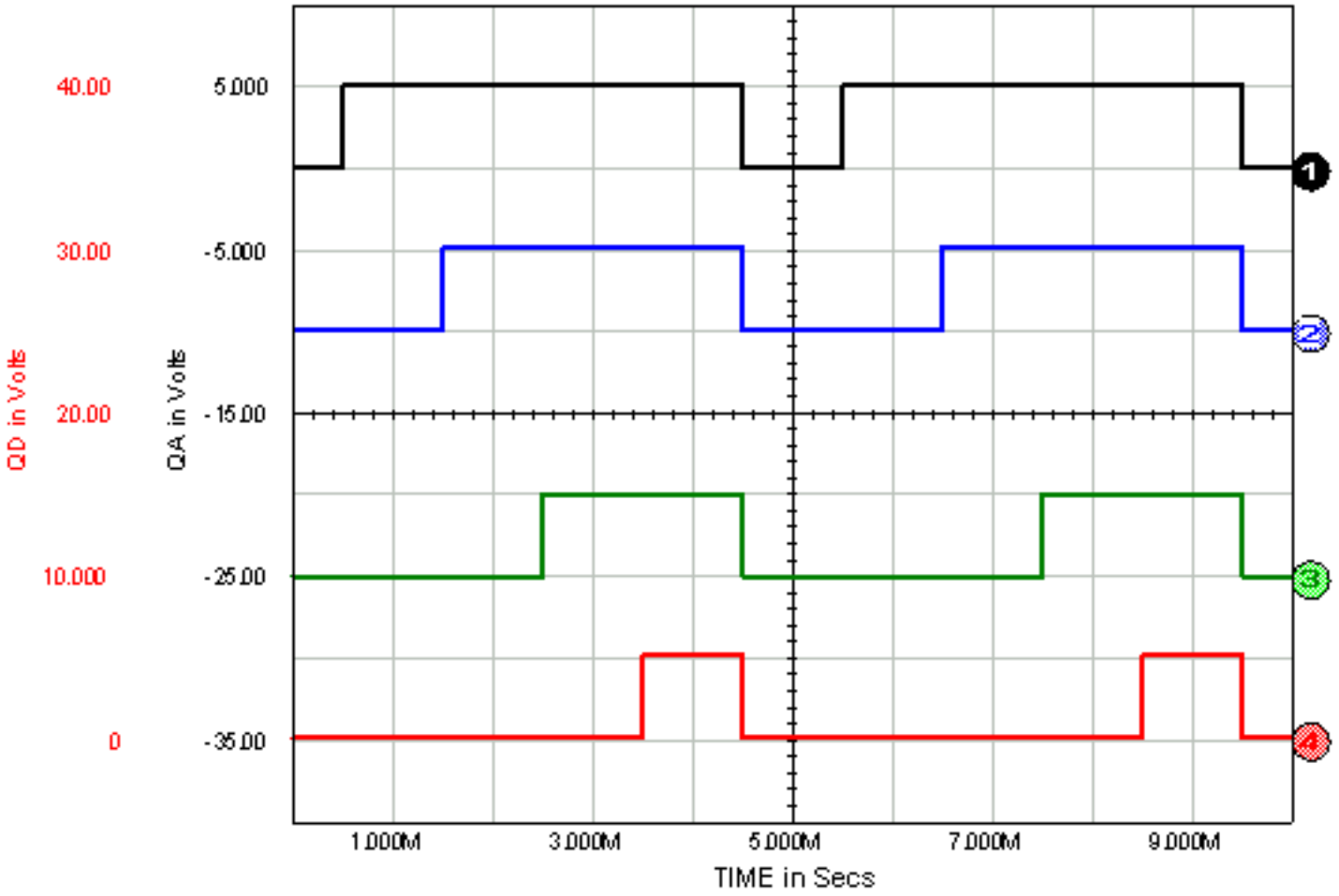
8
Resonator/Oscillator Circuits

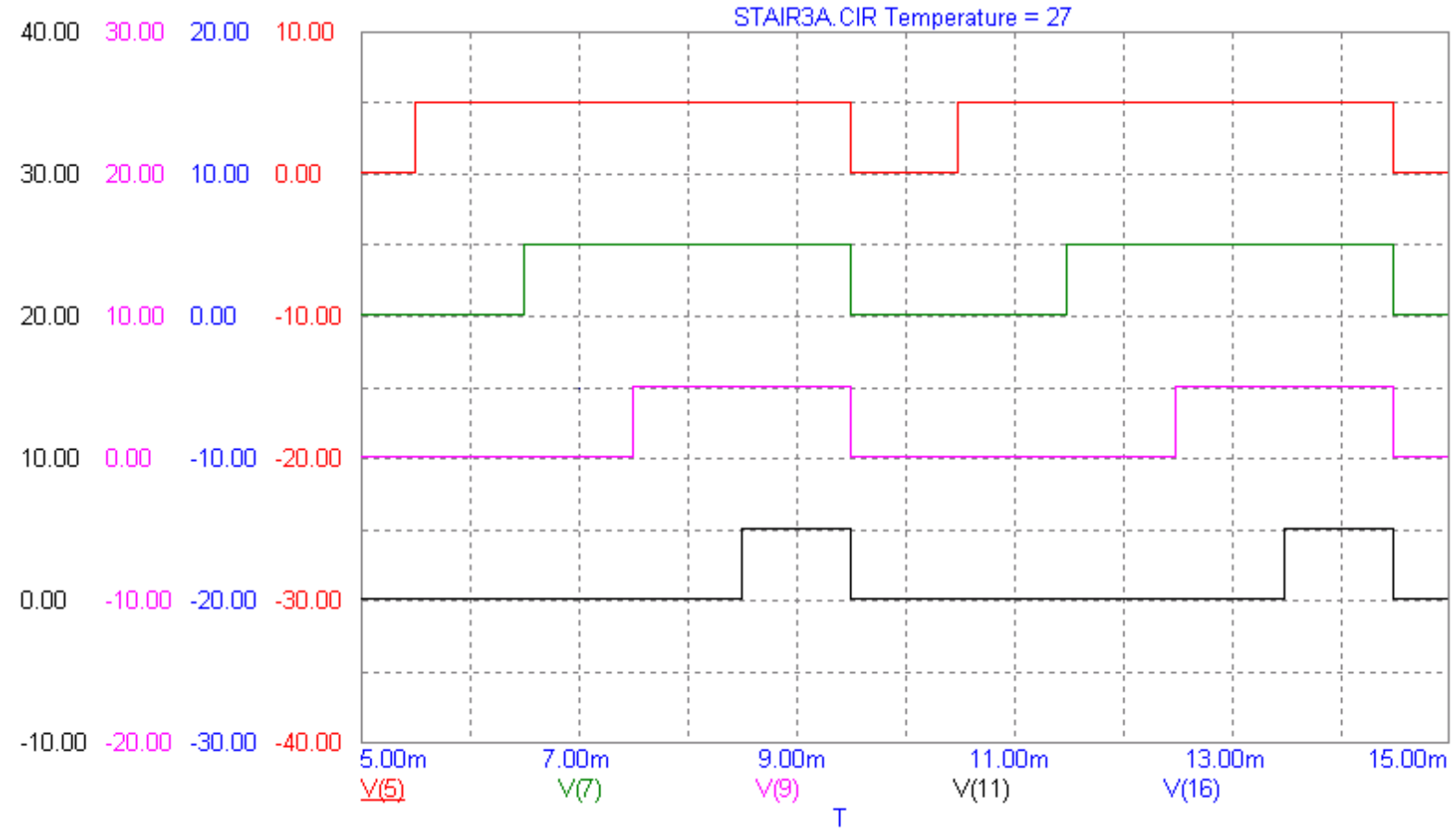
A Resonator is defined as a condition in a circuit that converts energy from a potential form to a kinetic form. One example of a resonance in electronics is that of the L-C filter. As the capacitor discharges, the inductor stores the energy, and as the inductor converts the magnetic energy into electrical energy, the capacitor charges up again. This action can be observed by an oscilloscope, with the resulting waveform having a distinct period. This repeating phenomenon is called a resonance. An Oscillator circuit is defined as "an electronic circuit that converts energy from a direct-current source into a periodically varying electrical output." [Parker, 1984] Therefore, an oscillator takes a steady state signal, and using electrical behaviors of circuit elements, converts the signal into a periodic, time variant signal. This oscillation can be sinusoidal in appearance (sine wave oscillation), square waved, triangular waved, or any variety of repeatable signals.

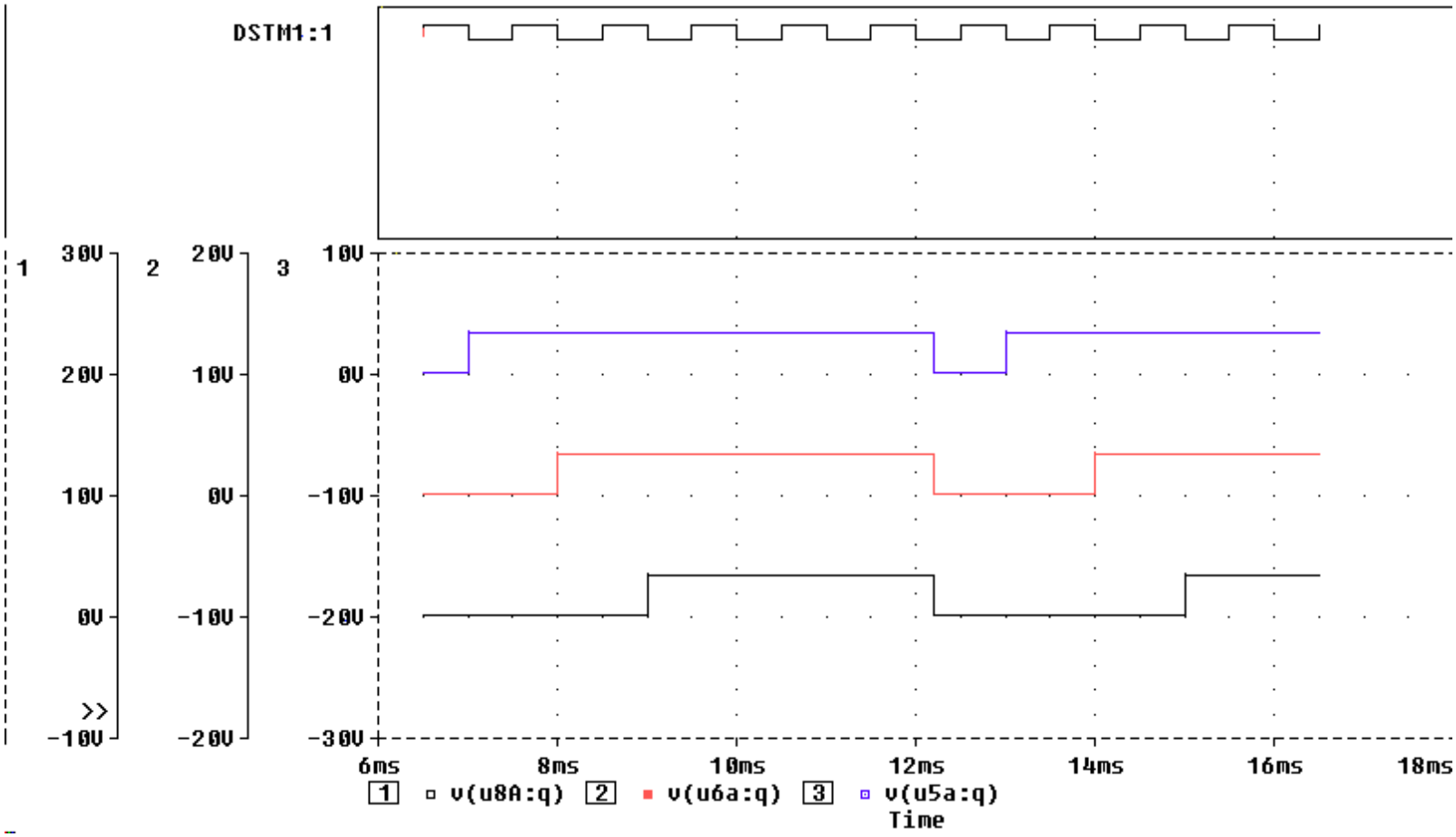
This time variant signal (usually referred to as an AC signal) is found in a multitude of electronic circuits. Power delivered to homes and businesses are nearly universally transmitted using an AC signal. Communications circuits require exact sine waves in order to transmit information over large distances with low loss of signal integrity. Just as numerous as the amount of potential uses for oscillator circuits is the amount of circuits that can create these oscillators. In this chapter we will examine the oscillator circuits in detail.

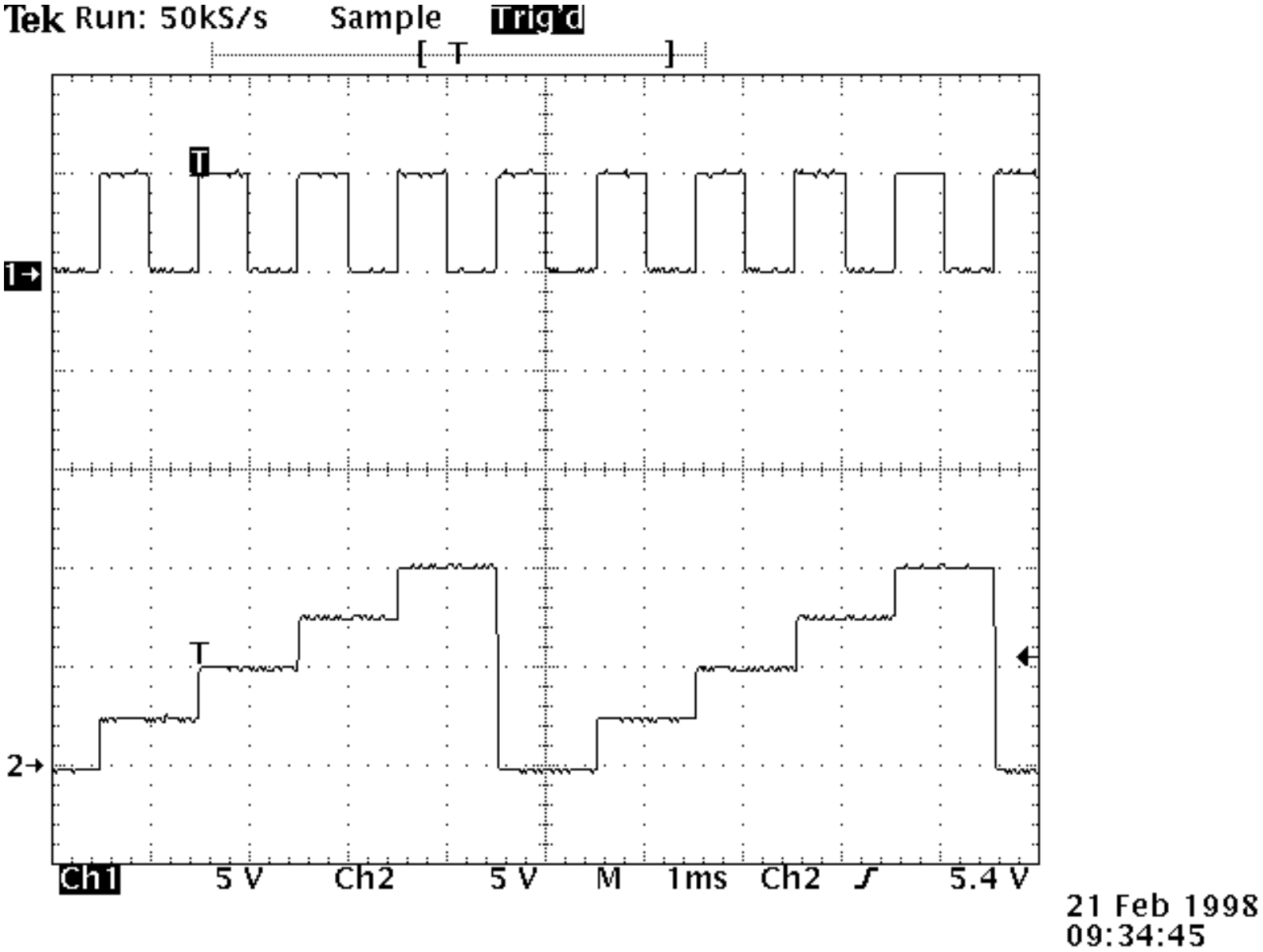

R2 100K
V1 15
R1 100K
V(22)
OUT
R3 100K
R4 100K
V2 -15
R5 100K
R6 100K
V(14)
RESET
V(27)
QA
V(29)
QB
V(28)
QC
V(26)
QD
One
Zero
Clock
V(10)
CLOCK
PR
CLK
CL
VCC
VEE

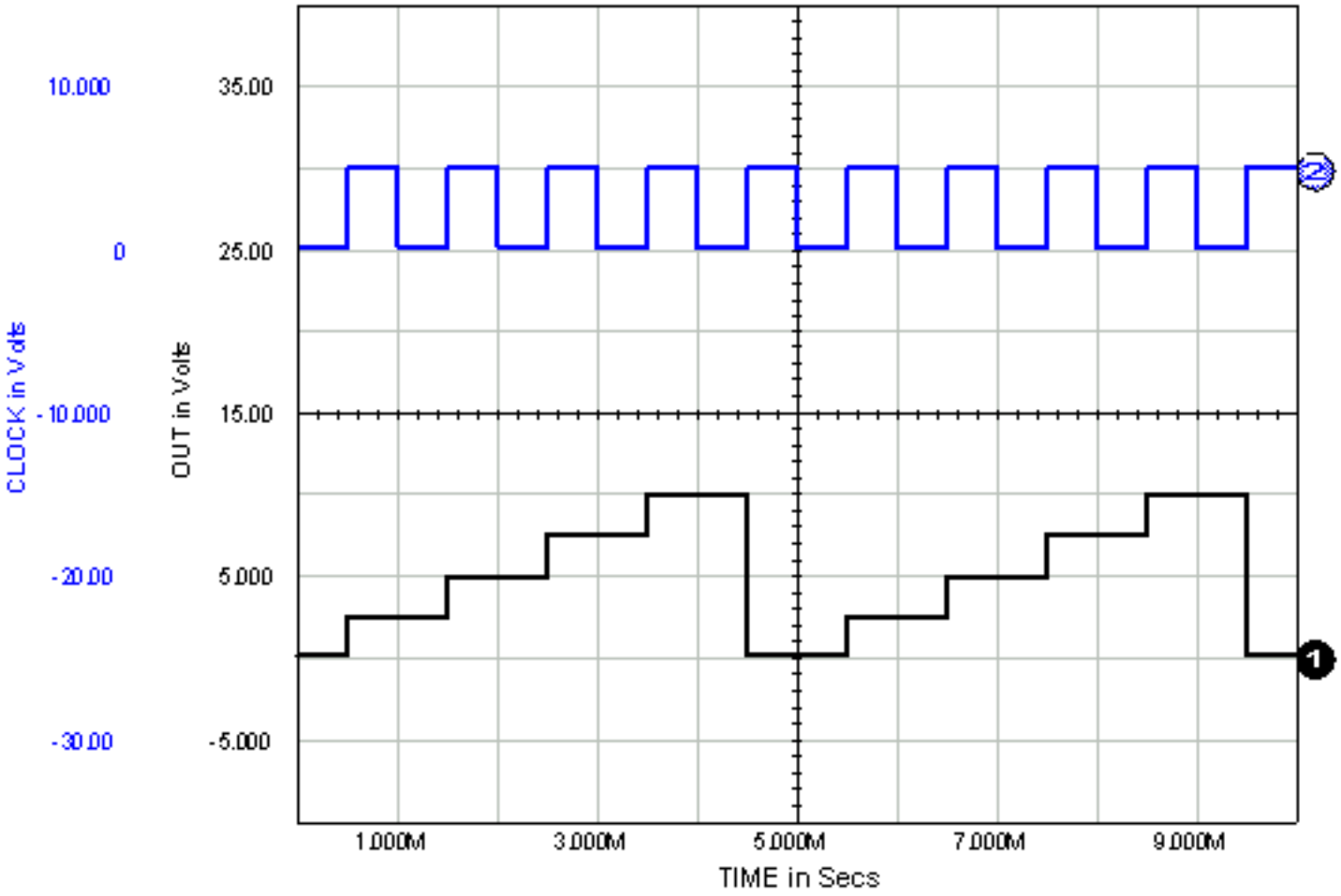

Tek Run: 50kS/s Sample Trig'd
T
1
R1
R2
2
Ch1 5 V Ch2 5 V M 1ms Ch1 ∫ 4 V
Ref1 5 V 1ms
21 Feb 1998
09:40:36

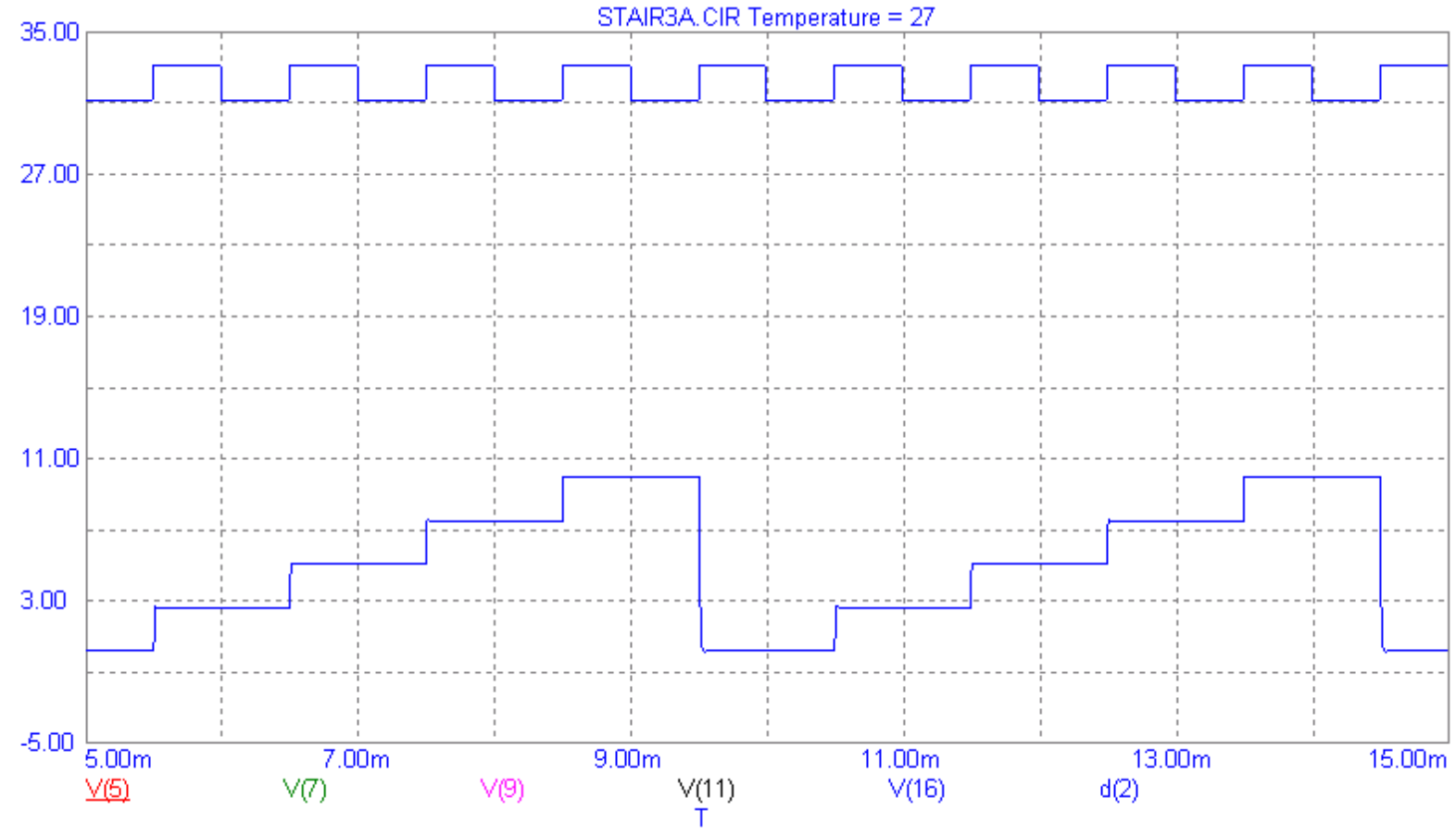

40.00
30.00
20.00
10.000
0
QD in Volts
5.000
-5.000
-15.00
-25.00
-35.00
QA in Volts
1.000M
3.000M
5.000M
7.000M
9.000M
TIME in Secs
1
2
3
4

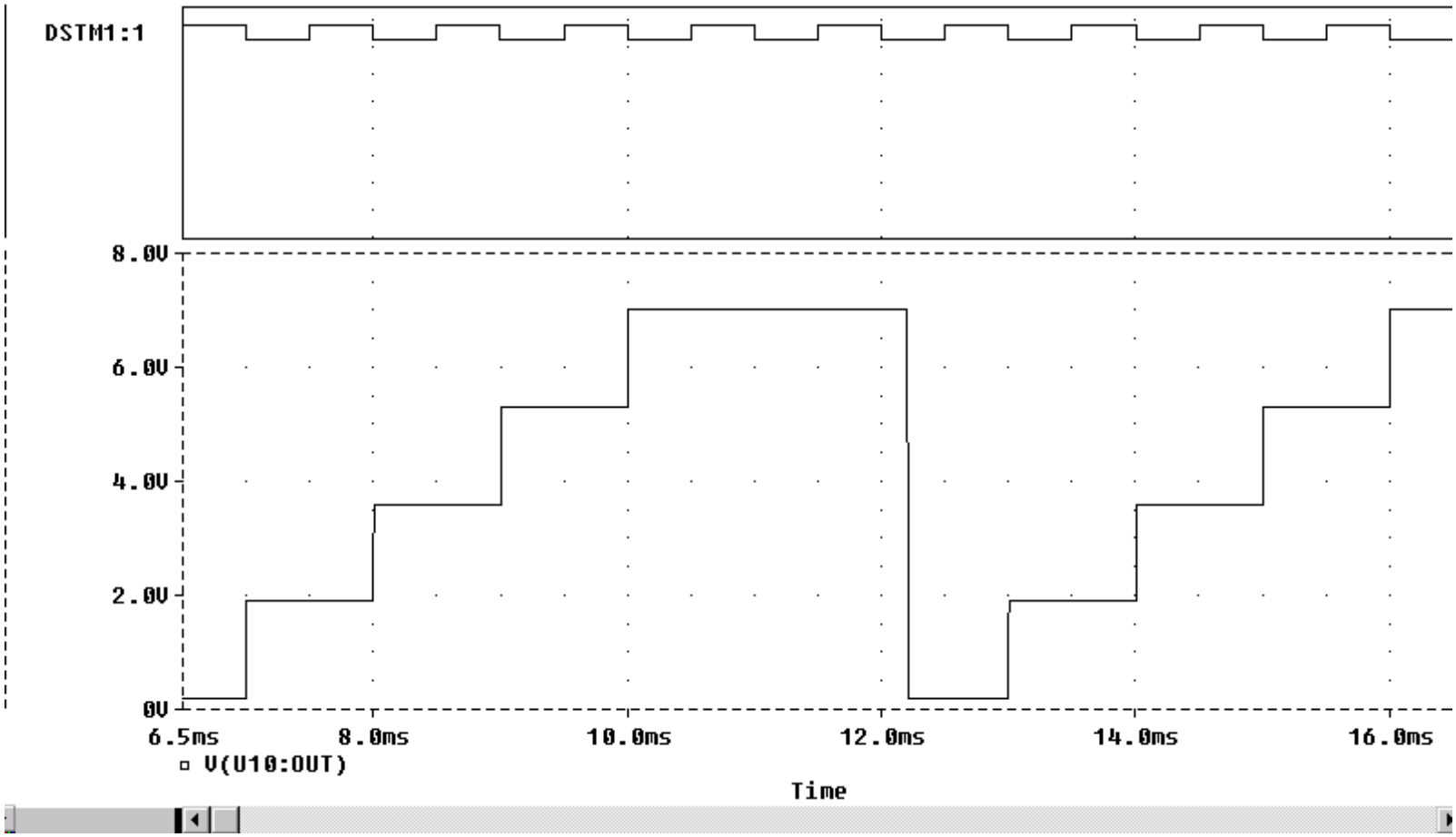

STAIR3A.CIR Temperature = 27
40.00 30.00 20.00 10.00
30.00 20.00 10.00 0.00
20.00 10.00 0.00 -10.00
10.00 0.00 -10.00 -20.00
0.00 -10.00 -20.00 -30.00
-10.00 -20.00 -30.00 -40.00
5.00m
7.00m
9.00m
11.00m
13.00m
15.00m
V(5)
V(7)
V(9)
V(11)
V(16)
T


DSTM1:1
1
30V
20V
10V
0V
>>
-10V
2
20V
10V
0V
-10V
-20V
3
10V
0V
-10V
-20V
-30V
6ms
8ms
10ms
12ms
14ms
16ms
18ms
1 v(u8A:q) 2 v(u6a:q) 3 v(u5a:q)
Time


Tek Run: 50kS/s Sample Trig'd
T
1→
T
2→
Ch1 5 V Ch2 5 V M 1ms Ch2 ∫ 5.4 V
21 Feb 1998
09:34:45


10.000
0
-10.000
-20.00
-30.00
CLOCK in Volts
35.00
25.00
15.00
5.000
-5.000
OUT in Volts
1.000M
3.000M
5.000M
7.000M
9.000M
TIME in Secs
2
1


STAIR3A.CIR Temperature = 27
35.00
27.00
19.00
11.00
3.00
-5.00
5.00m
7.00m
9.00m
11.00m
13.00m
15.00m
V(5)
V(7)
V(9)
V(11)
V(16)
d(2)
T


DSTM1:1
8.0V
6.0V
4.0V
2.0V
0V
6.5ms
8.0ms
10.0ms
12.0ms
14.0ms
16.0ms
V(U10:OUT)
Time

#34: 555 Timer Oscillator

The astable operation of the UA555 as an oscillator has a duty cycle and free running frequency which are both precisely controlled with two external capacitors and two resistors. The circuit shown in Figure 34-1.

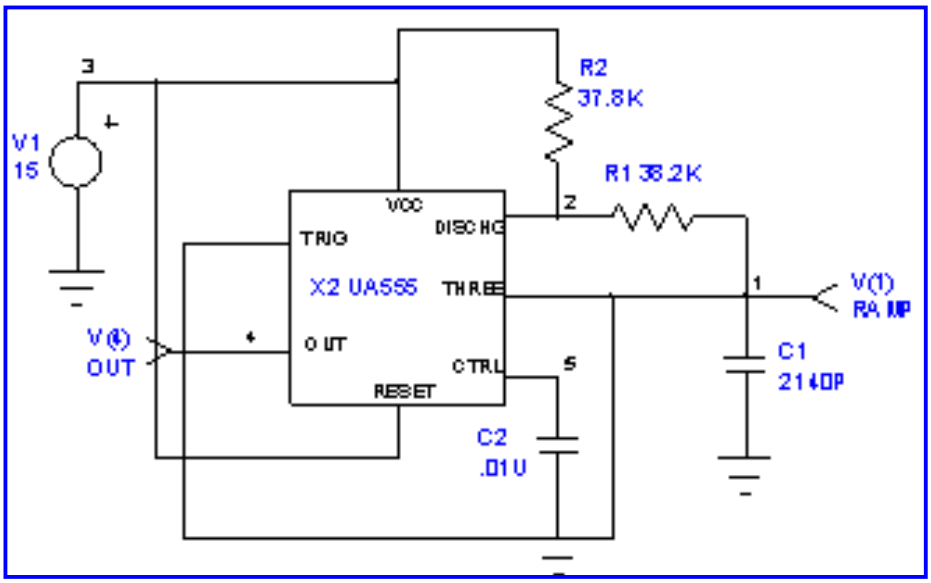


Figure 34-1: 555 Oscillator Schematic

The circuit was constructed in the laboratory. The values of RA, RB, C1, and C2 are the actual measured values of the components used in the circuit. A Tektronix TDS 340A digital real-time oscilloscope was used to record the output data as shown in Figure 34-2. The duty cycle is calculated to be 66.7% and the output voltages oscillate from 5V to 10V. The simulated data, from Ispice, Micro-Cap V, and Pspice, is shown in figure 34-3 through figure 34-5. Table 34-1 illustrates the variances in simulated output data.

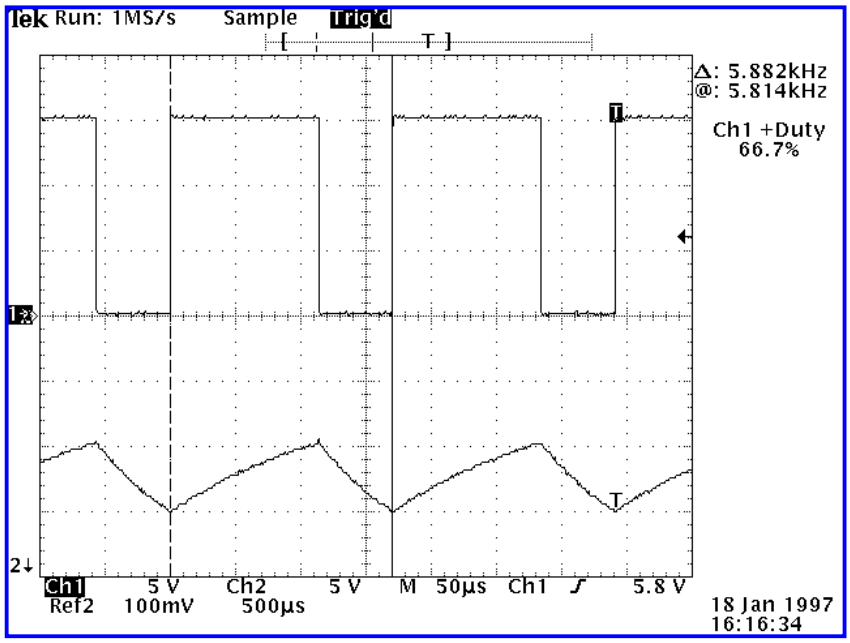


Figure 34-2: 555 Oscillator Measured Data

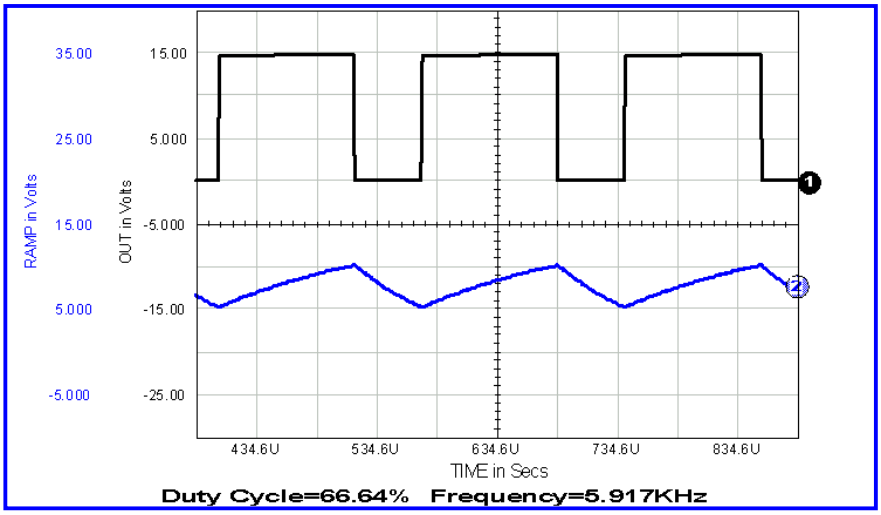


Figure 34-3: Ispice Simulated Data

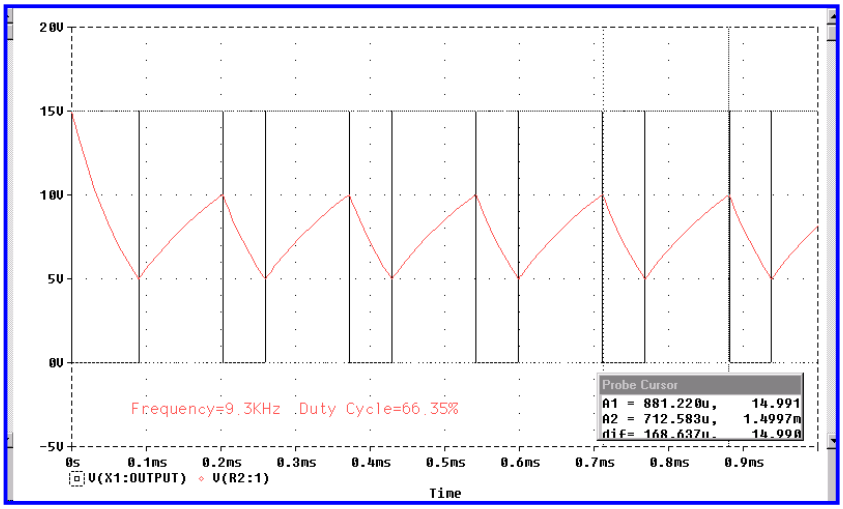


Figure 34-4: Pspice Simulated Data

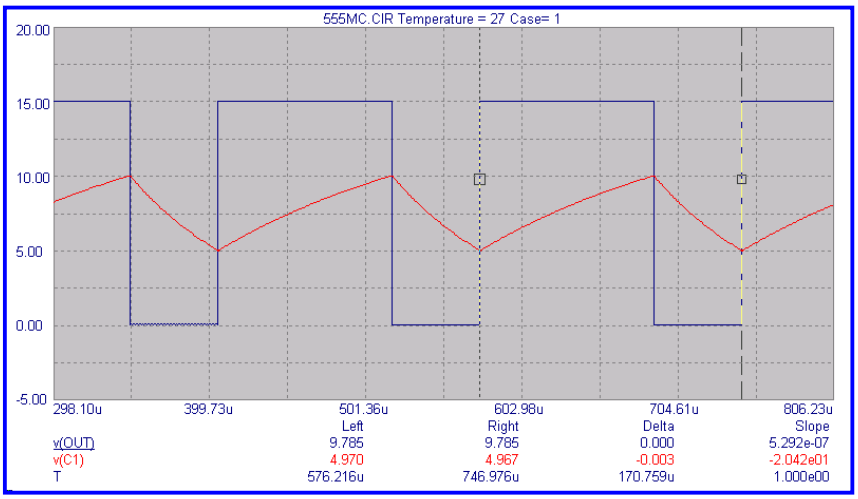


Figure 34-5: Micro-Cap V Simulated Data

Simulator	Spice File	Duty Cycle (%)	Frequency (KHz)	Run Time (sec)
Ispice	555osc	66.64	5.917	16.77
Micro-Cap V	555mc	66.39	5.856	28.94
Pspice	ps 555	66.35	5.93	4.69

Table 34-1: Summary of Results

Note: The Pspice 555D component is digital and therefore greatly reduced the run time of the simulation.

Simulation Tips:

- The Ispice simulator required a UIC statement in the edit controls box, even though no initial conditions were used in the transient simulation.
- The Micro-Cap V global setting for DIGIOLVL, the default digital IO level, needed to be specified at two for the simulation to run correctly.

#35: 4th Order Butterworth Low Pass Oscillator

Shown in Figure 35-1 is a fourth order butterworth low pass oscillator. Figure 35-2 is the square wave generated at node 10 and the resultant sine wave after filtering at node 3. The lab results are shown in Figure 35-3.

- Circuit tip: Note that the Q of the op-amp stage in a oscillator circuit is designed to be large in order to create an oscillation, while the Q of the op-amp stage of a filter is designed to be small in order to suppress the possibility of oscillation.

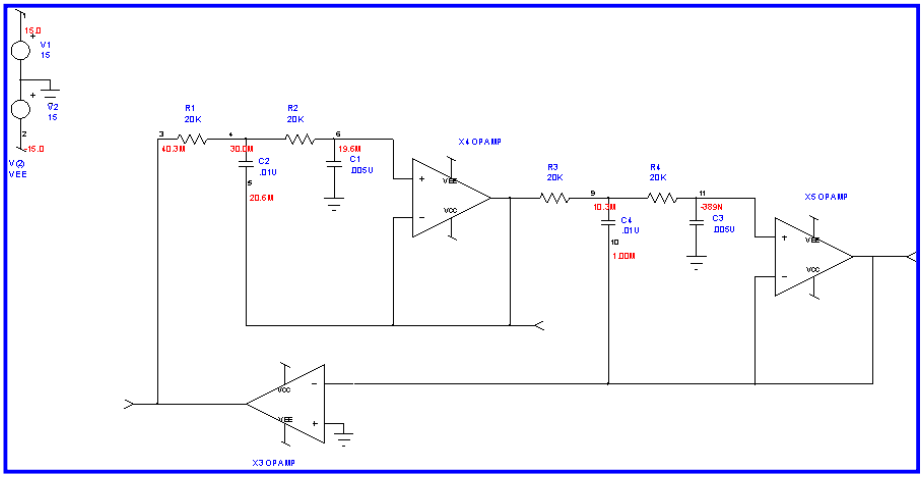


Figure 35-1: Fourth order Butterworth low pass oscillator schematic

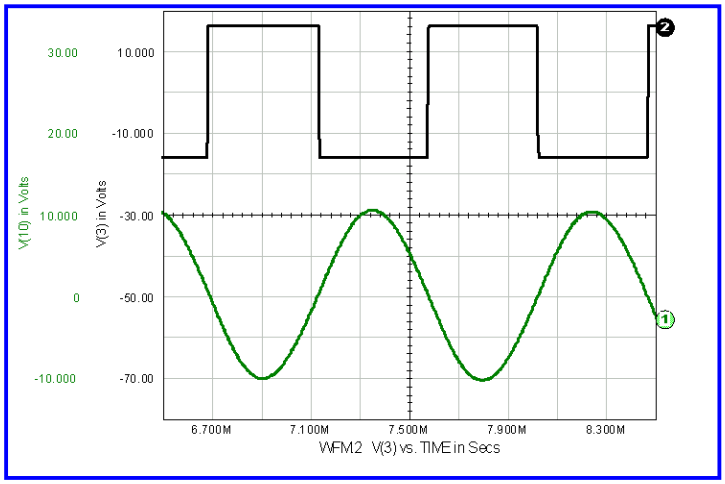


Figure 35-2: IsSpice results of square wave generated at node 10 and resultant sine wave at node 3

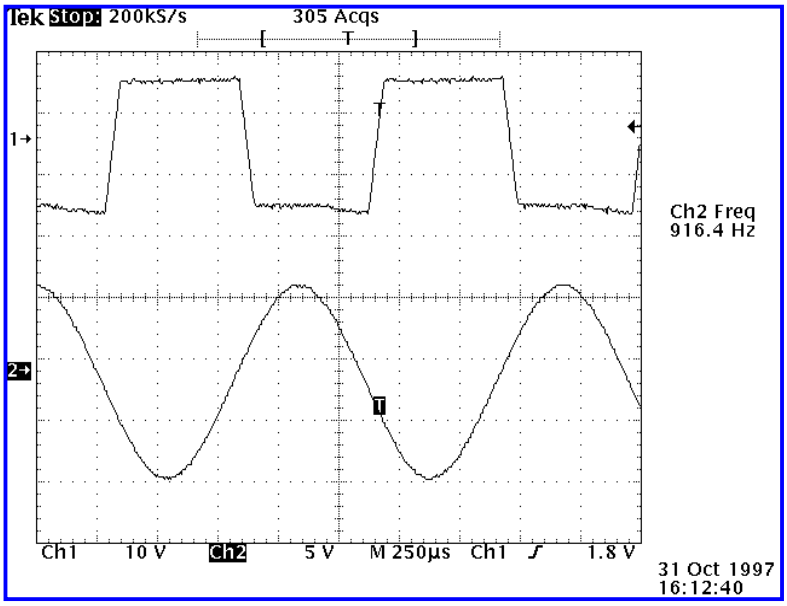


Figure 35-3: Hardware results of Butterworth Low Pass Oscillator.

The schematic for Microcap is shown in Figure 35-4. The resulting waveforms are shown in Figure 35-5. The Pspice result is shown in Figure 35-6.

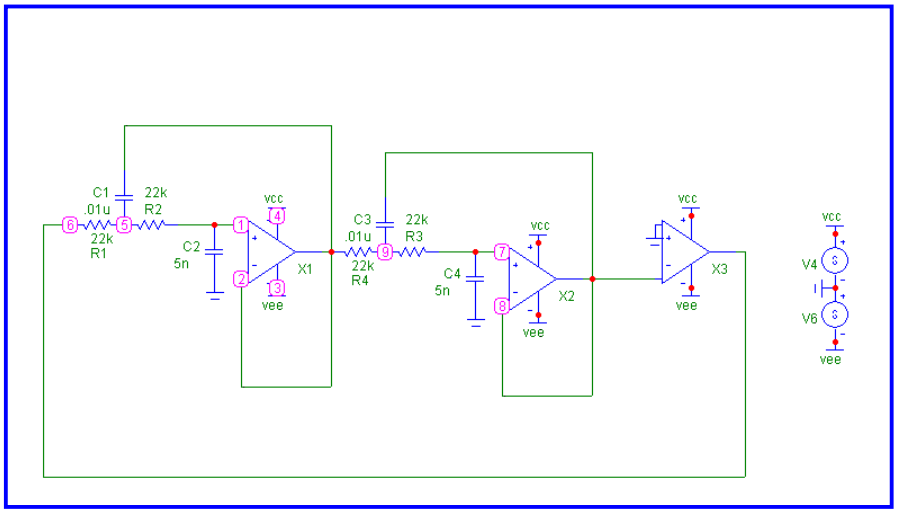
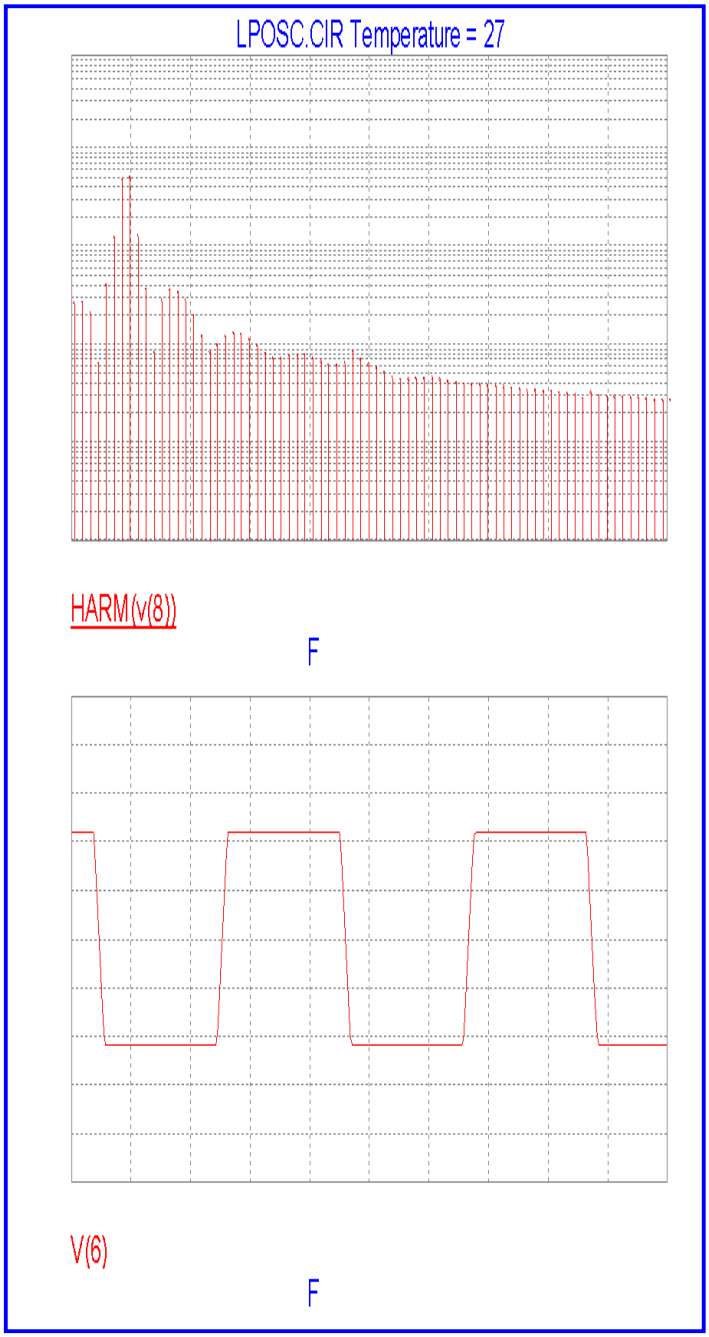


Figure 35-4: Microcap schematic of Butterworth Low Pass Oscillator


LPOSC.CIR Temperature = 27
HARM(v(8))
F
V(6)
F

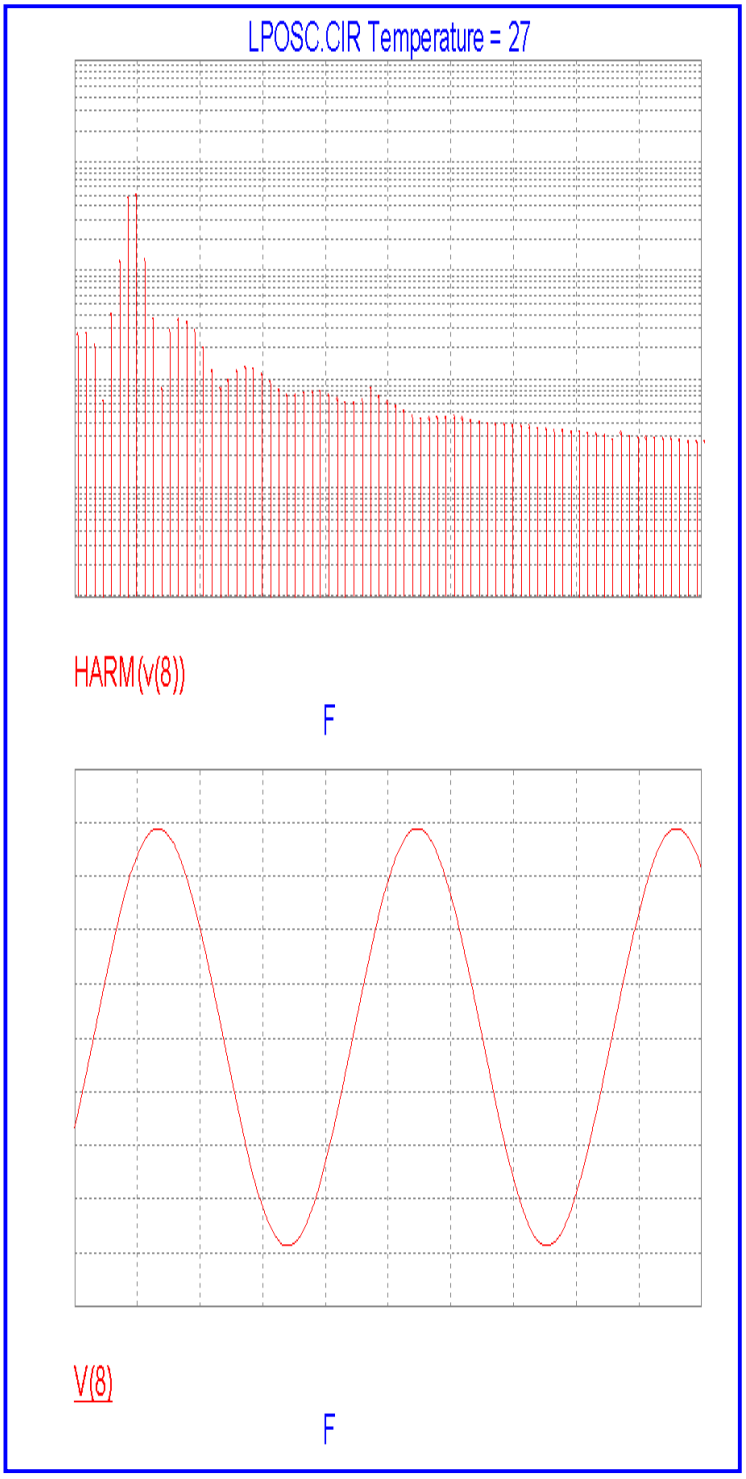


Figure 35-5: Microcap results of Butterworth Low Pass Oscillator

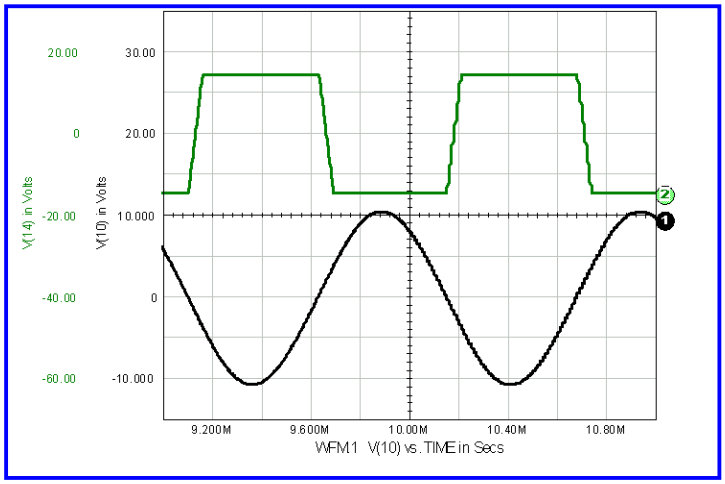


Figure 35-6: Pspice results of Butterworth Low Pass Oscillator

- Simulation tip: Although all three simulators correctly predicted the frequency and amplitude of the Sine wave, only the IsSpice simulation predicted the DC offset in the output waveform. The reason for this is the simulations for each used the LM124 libraries that came with the simulation package. These libraries can be provided by manufacturers or the software company. It is very important to remember that these models may not be accurate for the parameter that you are interested in. Even in IsSpice, there were 4 different models for the LM124 and only one correctly predicted the DC offset. If the model does not accurately reflect the component being modeled, this does not necessarily mean the model is useless or wrong (although this is a possibility). People make models to model different aspects of the part. For example, some models may have noise rejection modeled accurately, or AC characteristics, or input current draw, or some may not model any of these. Models may be transistor level or Macro models. Models are made for different reasons. If all you are interested in are large signal characteristics, it would make no difference if noise rejection was modeled accurately. In addition, if you were only interested in large signal characteristics, you probably would not want a model with noise rejection because it is probably transistor level and will take orders of magnitude longer to simulate and make the simulation much more difficult to converge. The bottom line is, in any simulator, all models are not created equal. You must understand the trade off between speed, accuracy, and the ability to converge [Kielkowski, 1994].

The Fourier analysis was also computed using each of the simulators and compared to the hardware data. The Fourier results of the hardware is shown in Figure 35-7. The Fourier results of each of IsSpice, Microcap, and Pspice are shown in Figure 35-8 through 35-10.

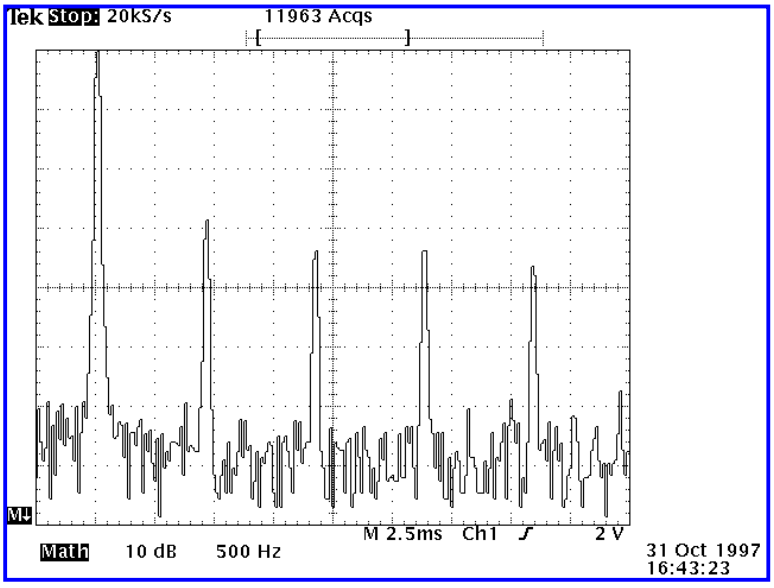


Figure 35-7: Fourier analysis results of output of Butterworth Low Pass Oscillator.

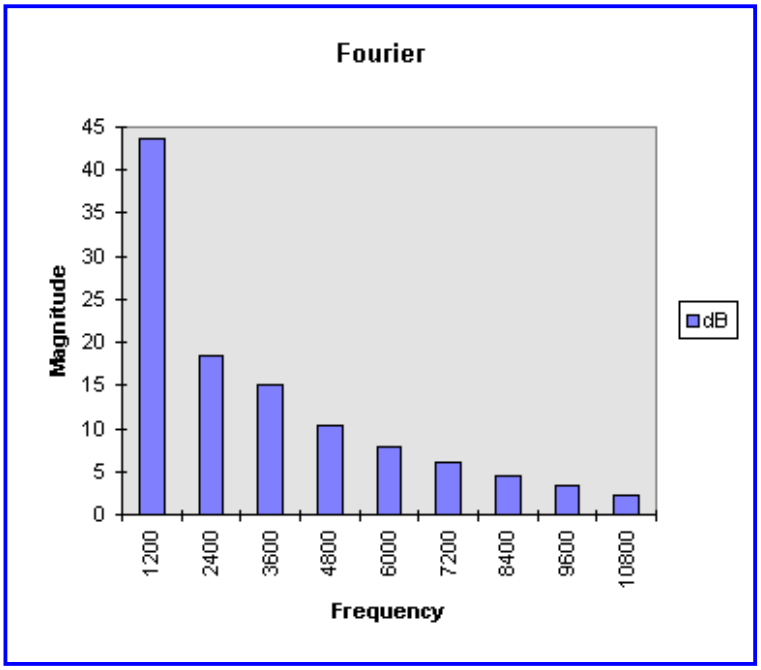


Figure 35-8: IsSpice Fourier results

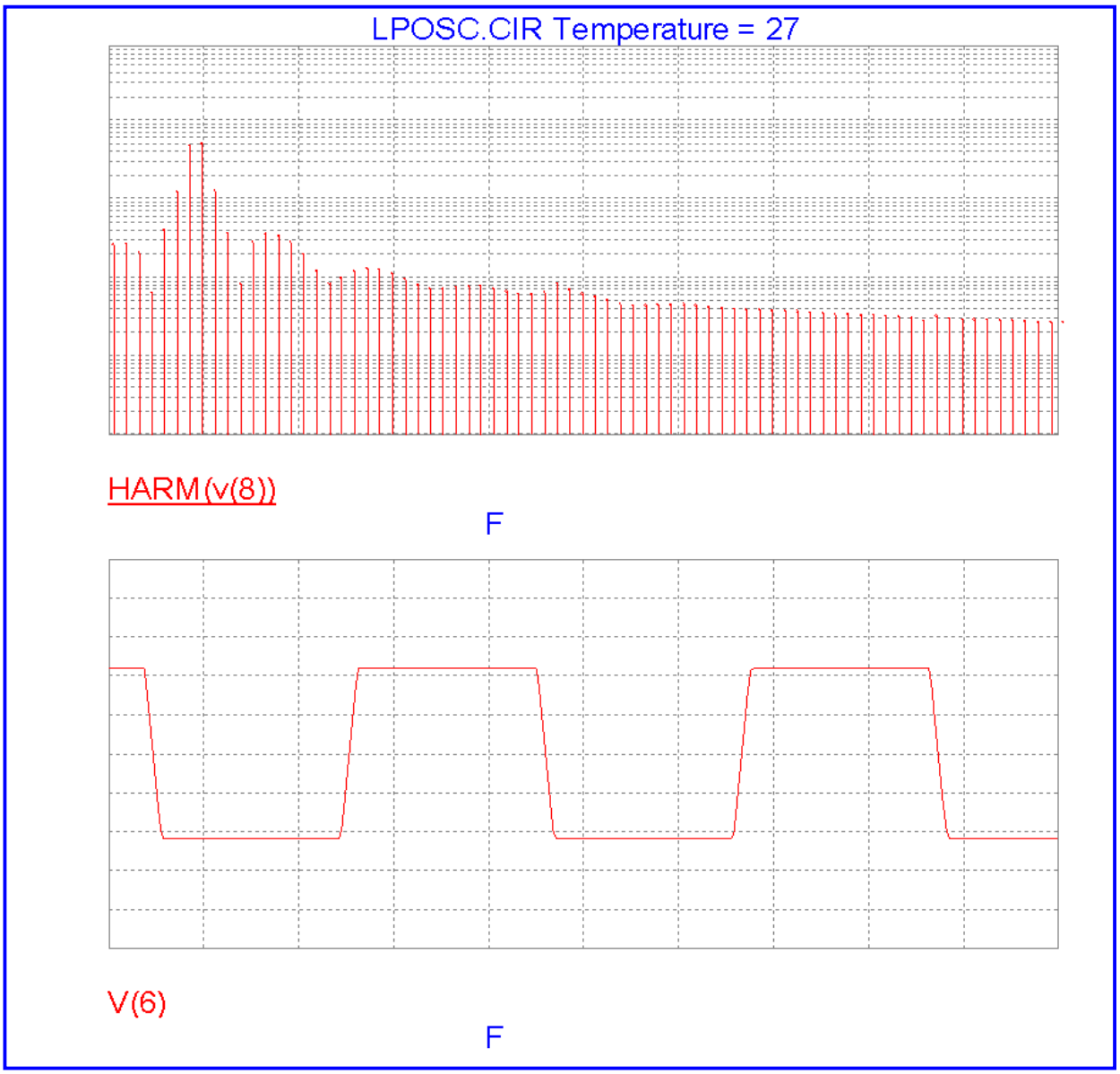


Figure 35-9: Microcap Fourier results

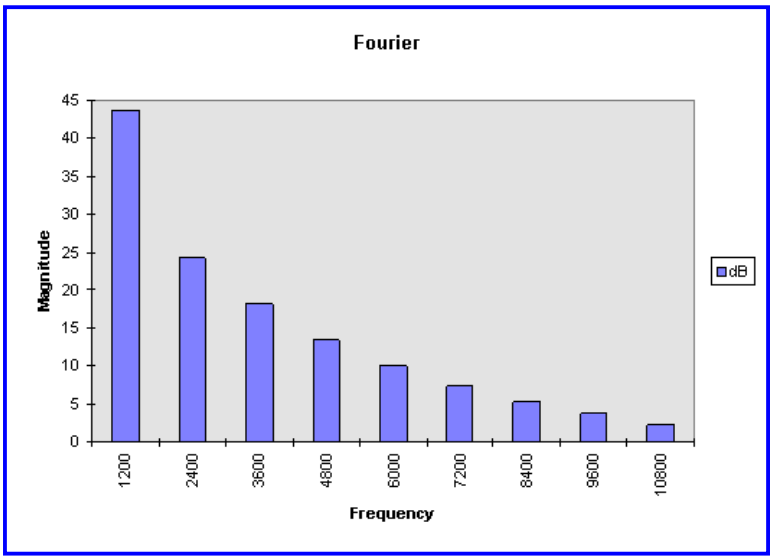


Figure 35-10: Pspice Fourier results

Notice the simulators returned three different results for the Fourier results of this circuit.

Separated waveforms of the hardware in figure 35-3 are shown in Figure 35-11 and Figure 35-12 with measurements.

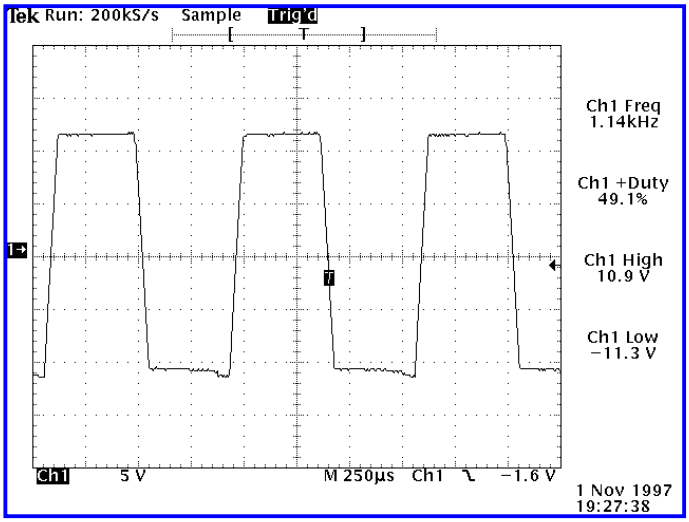


Figure 35-11: Node 10 voltage waveform with high voltage, low voltage, duty cycle, and frequency measurements

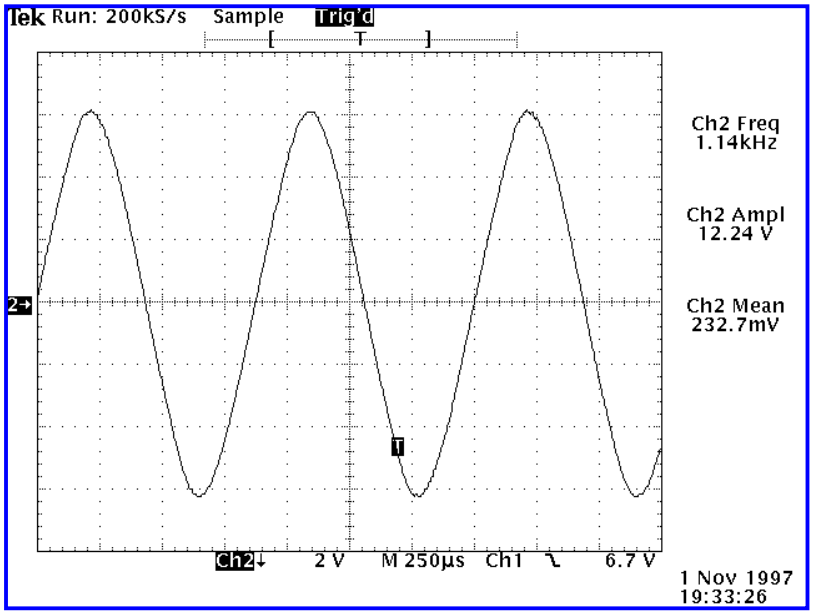
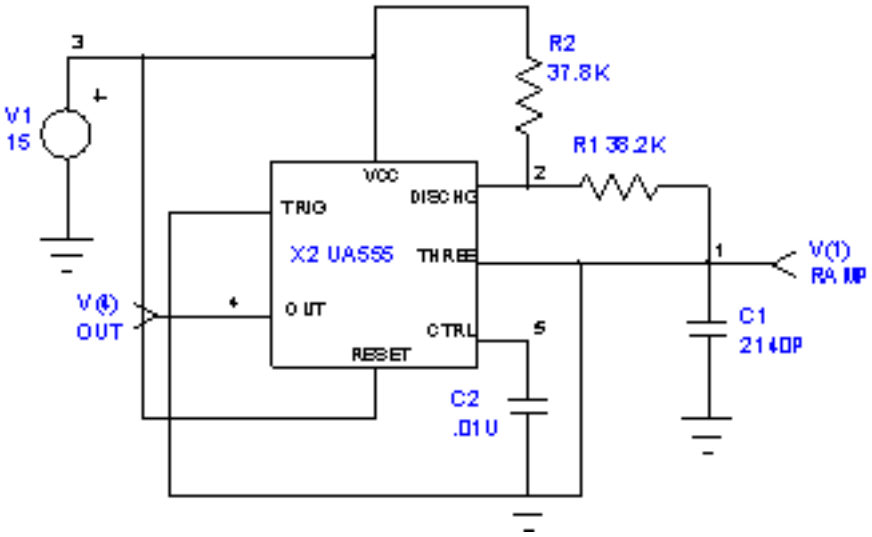
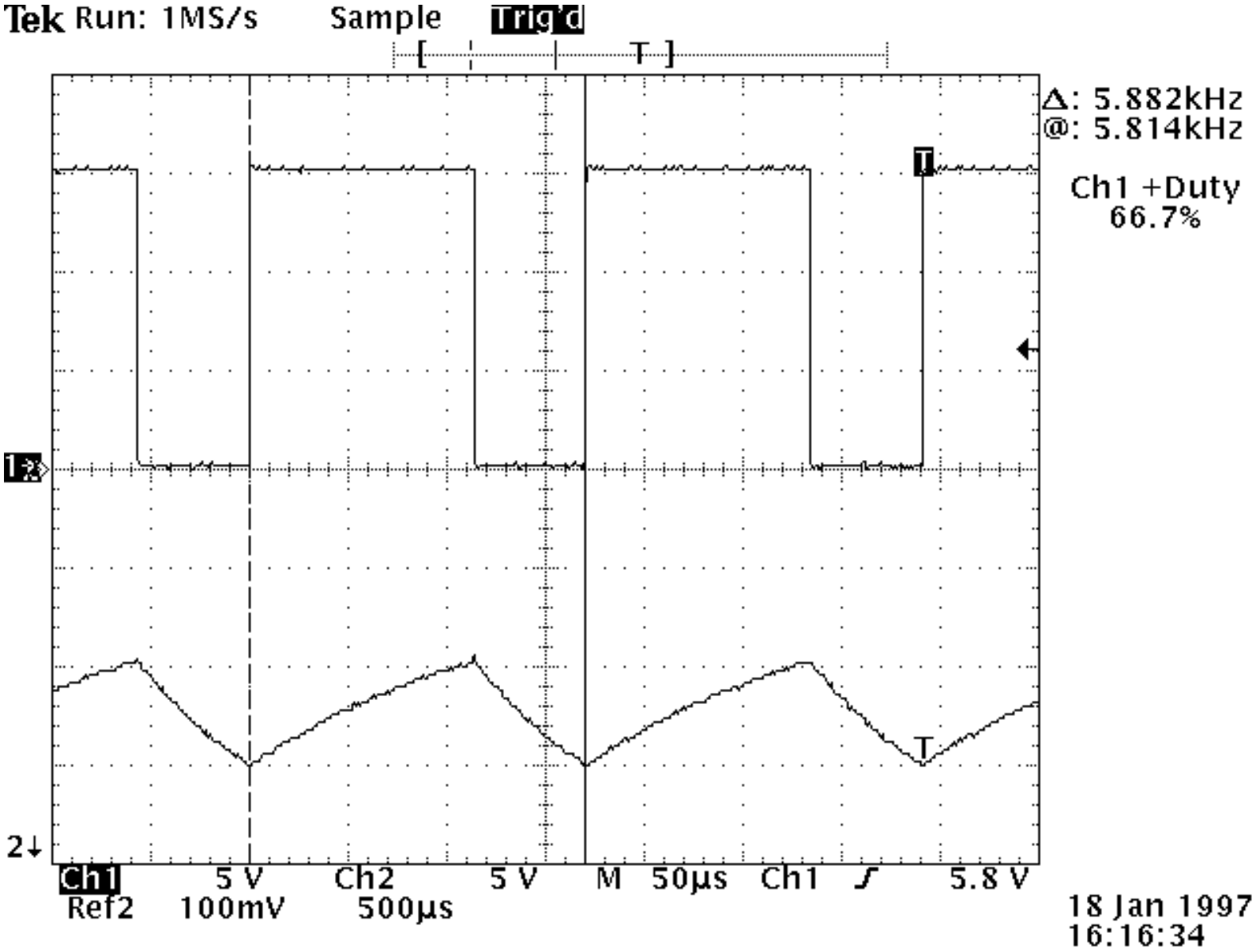


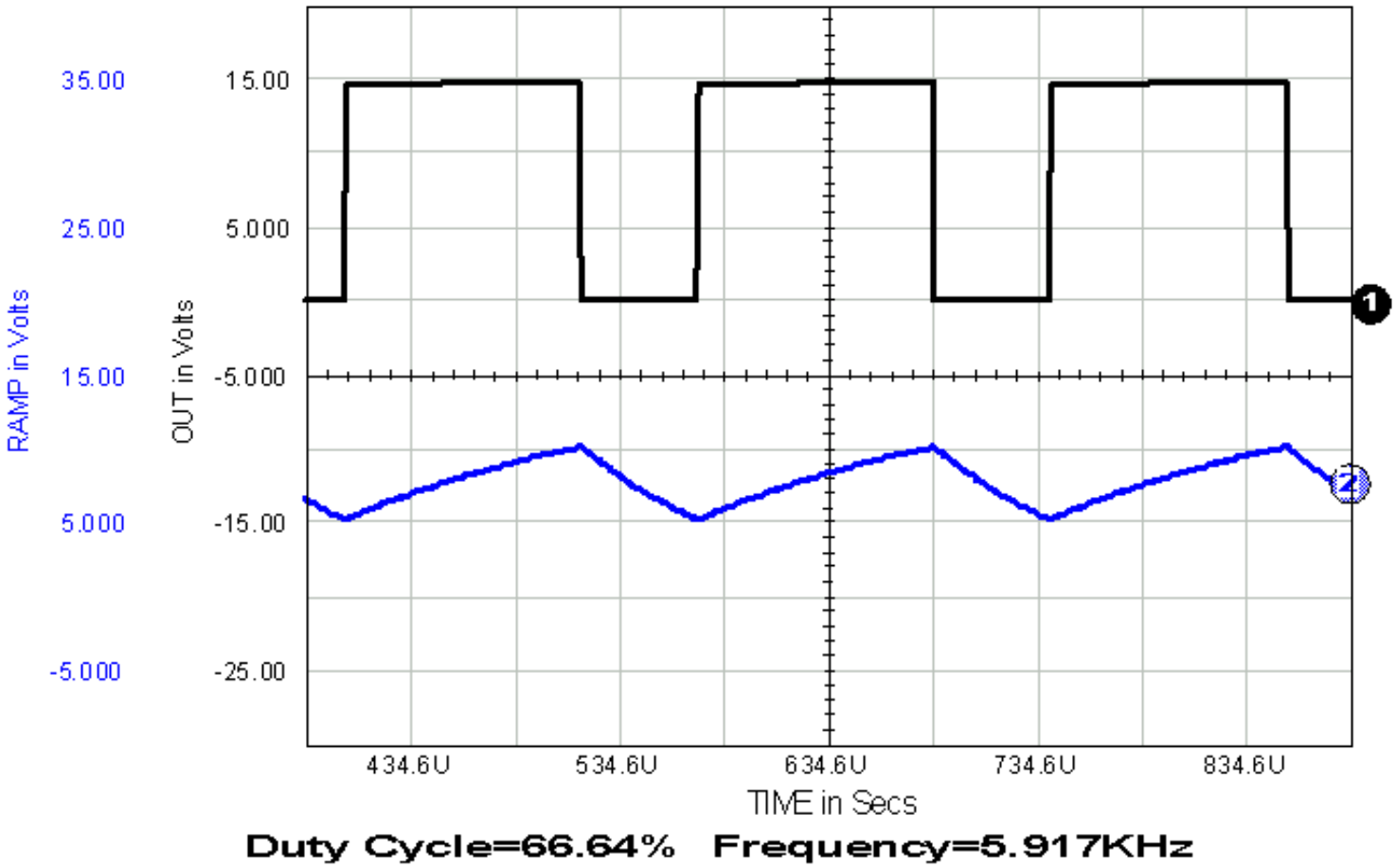
Figure 35-12: Output sine wave with frequency, amplitude, and mean measurements.

Run Time Summary		
IsSpice v 7.6	PsPice v 6.3	Micro-Cap V v2
16.45 Sec	27.68 Sec	32.22 Sec
Advantages: Good long term frequency stability, moderate distortion, easily adjusted, moderate drive capability		
Disadvantages: High parts count, DC offset		

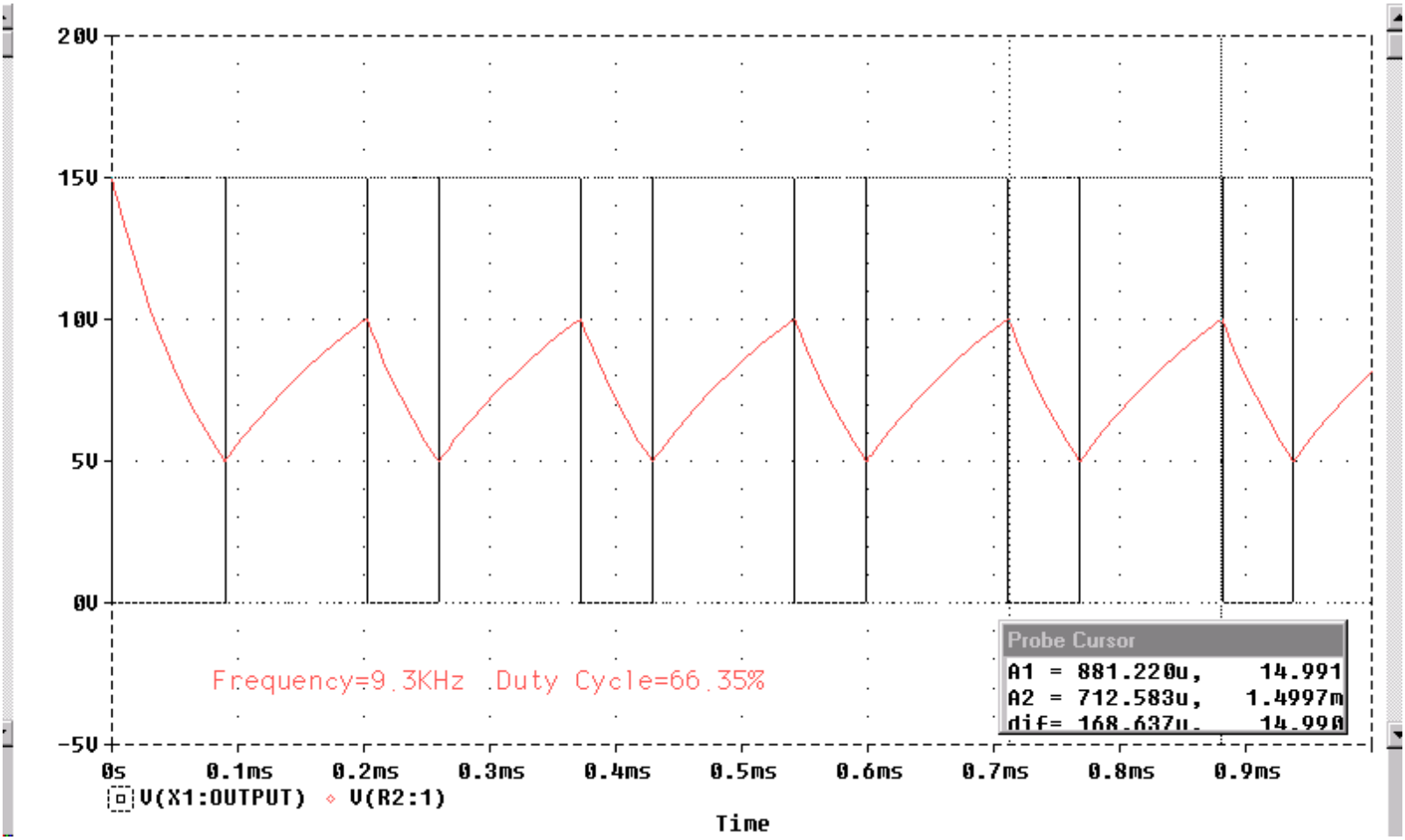
Filenames: lp_osc (IsSpice) pbp_osc (Pspice) Lposc (Micro-cap) Four.xls (Excel)

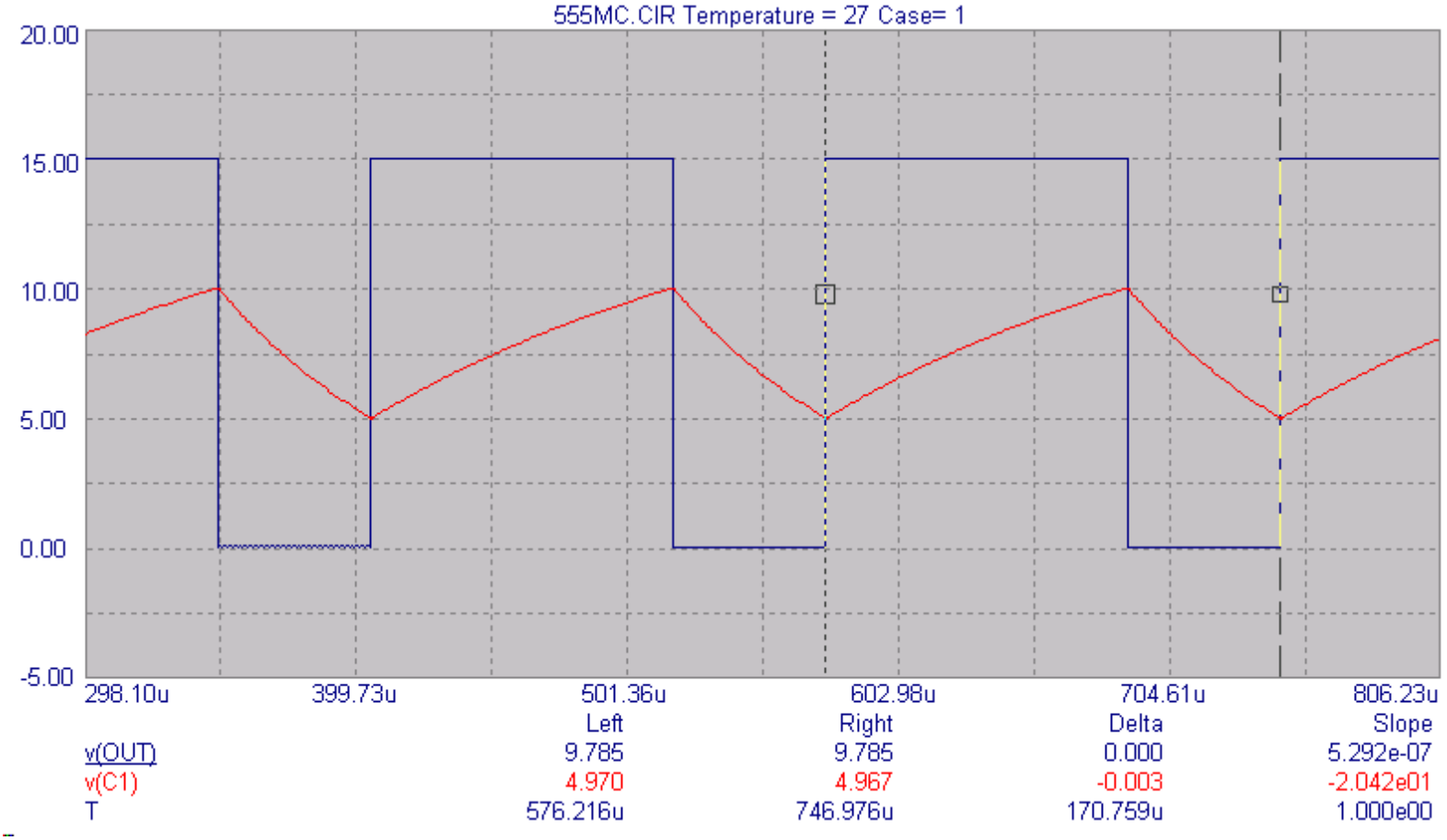

3
V1
15
R2
37.8K
R1 38.2K
2
VCC
DISCHG
TRIG
X2 UA555
THREE
1
V(1)
RAMP
V(4)
OUT
4
OUT
CTRL
5
RESET
C1
2140P
C2
.01U


Tek Run: 1MS/s Sample Trig'd
Δ: 5.882kHz
@: 5.814kHz
Ch1 +Duty
66.7%
Ch1 5 V Ch2 5 V M 50µs Ch1 ∫ 5.8 V
Ref2 100mV 500µs
18 Jan 1997
16:16:34



Duty Cycle=66.64% Frequency=5.917KHz


20V
15V
10V
5V
0V
-5V
Frequency=9.3KHz .Duty Cycle=66.35%
Probe Cursor
A1 = 881.220u, 14.991
A2 = 712.583u, 1.4997m
dif= 168.637u, 14.990
0s
0.1ms
0.2ms
0.3ms
0.4ms
0.5ms
0.6ms
0.7ms
0.8ms
0.9ms
V(X1:OUTPUT)
V(R2:1)
Time



	Left	Right	Delta	Slope
v(OUT)	9.785	9.785	0.000	5.292e-07
v(C1)	4.970	4.967	-0.003	-2.042e01
T	576.216u	746.976u	170.759u	1.000e00

Simulator	Spice File	Duty Cycle (%)	Frequency (KHz)	Run Time (sec)
Ispice	555osc	66.64	5.917	16.77
Micro-Cap V	555mc	66.39	5.856	28.94
Pspice	ps 555	66.35	5.93	4.69

#36: Hex Inverter Oscillator

The delay is created by the alternate charging of capacitor C1 (through R1) and discharge of C1 (through R2). The output is a square wave of fixed frequency. Many different inverter IC's are capable of this operation (SN54LS05, SN74LS04, CD4049). Make sure the propagation delay is small compared to the period of the oscillator frequency desired.

- Circuit tip: If you are attempting to breadboard this circuit, you may need bypass capacitors (0.1 uF capacitors from Vdd to the local IC ground) in order to minimize jitter and noise effects. These IC's switch at a very fast rate, and can easily cause switching noise to appear on the outputs.

- Circuit tip: A minimum propagation delay is required for the start up of this circuit. Make sure the data sheet or SCD of this part has a minimum listed propagation delay.

The circuit schematic is shown in Figure 36-1

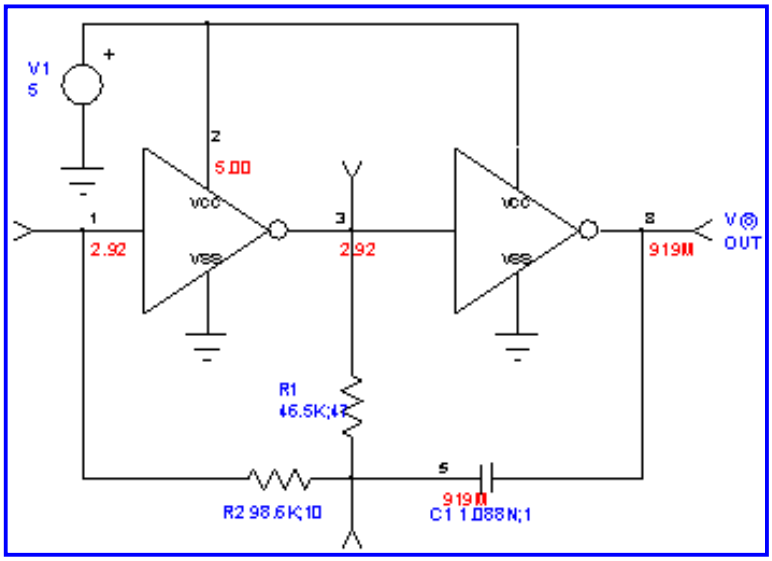


Figure 36-1: Inverter oscillator schematic

The IsSpice simulation results are shown in Figure 36-2. These results compare very well with the measured performance (Figure 36-3).

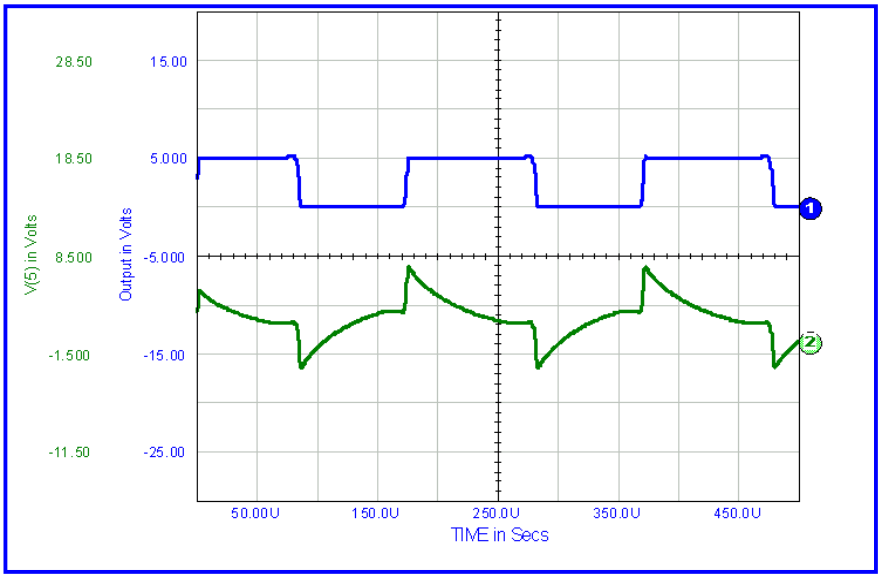


Figure 36-2: IsSpice simulation results of node 5 and output waveforms

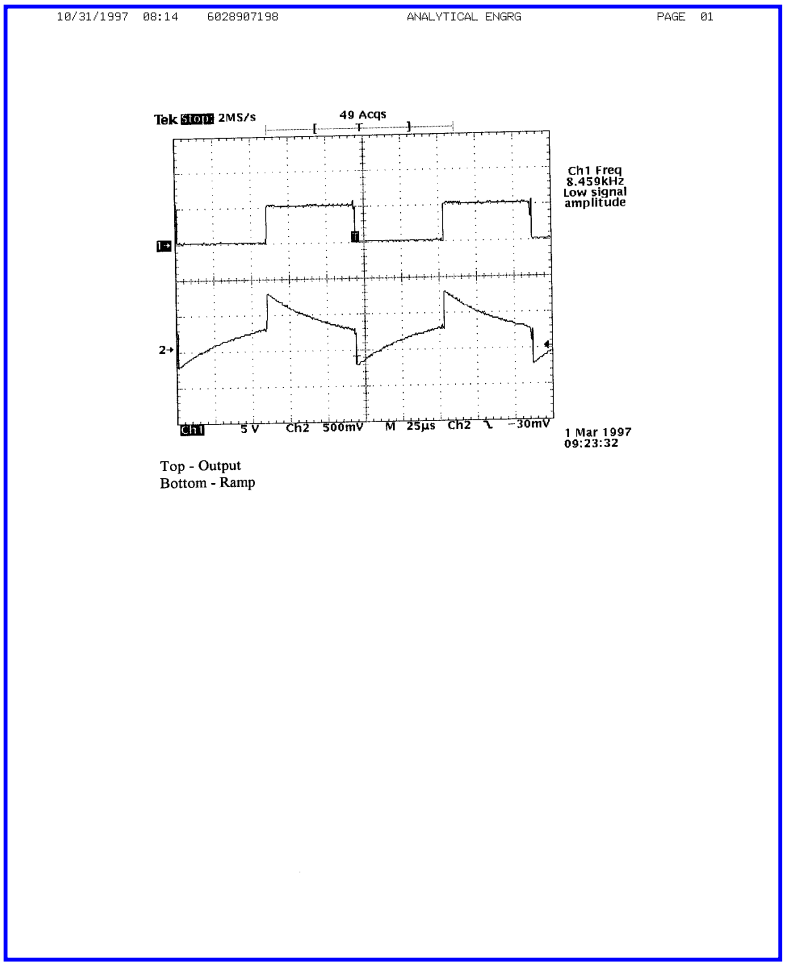


Figure 36-3: Hardware resulting waveforms of Inverter oscillator schematic.

The circuit was also simulated in Pspice and Micro-Cap. The results of those simulations are shown in Figure 36-4 and Figure 36-5. In figure 36-5, interestingly, the Micro-Cap results showed an output frequency of roughly twice that of Pspice or IsSpice. The reason for this is the Micro-Cap model for the 4049 inverter was used. This model had a hysteretic input threshold. In actuality, the part has a linear region and is not hysteretic, however, the Harris data sheet for this part does show the threshold levels of the model are within the data sheet requirements. This illustrates the dependency of the frequency on the input threshold of the 4049 inverter.

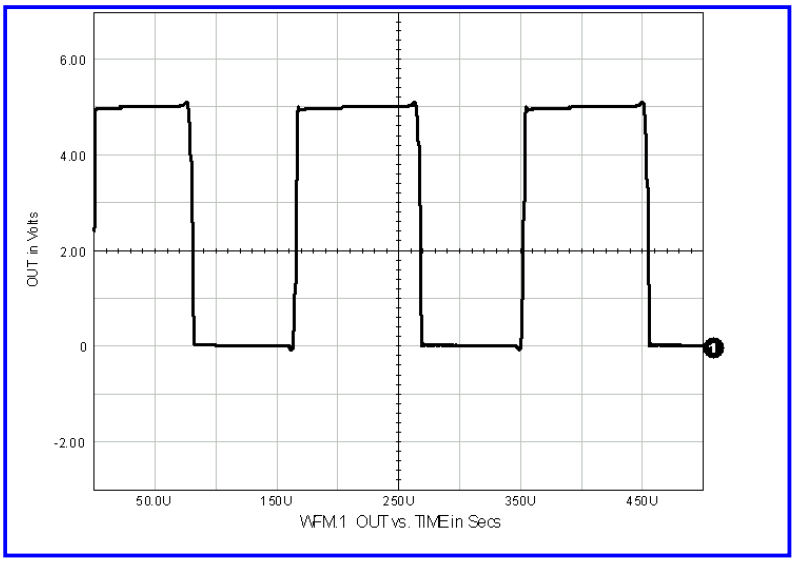


Figure 36-4: Pspice resulting waveforms of Inverter oscillator schematic

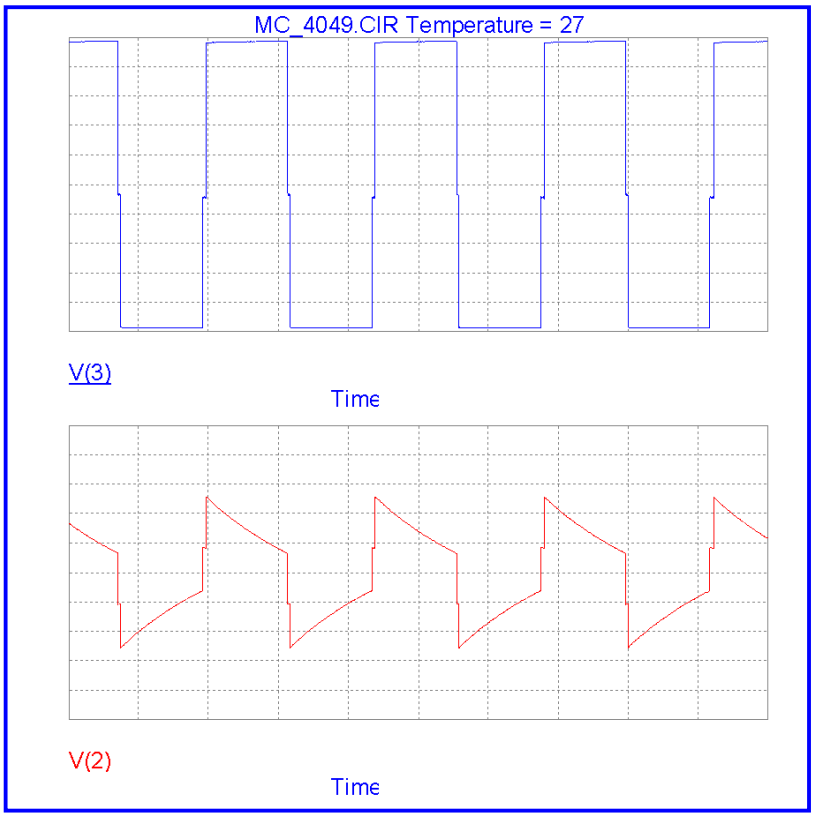
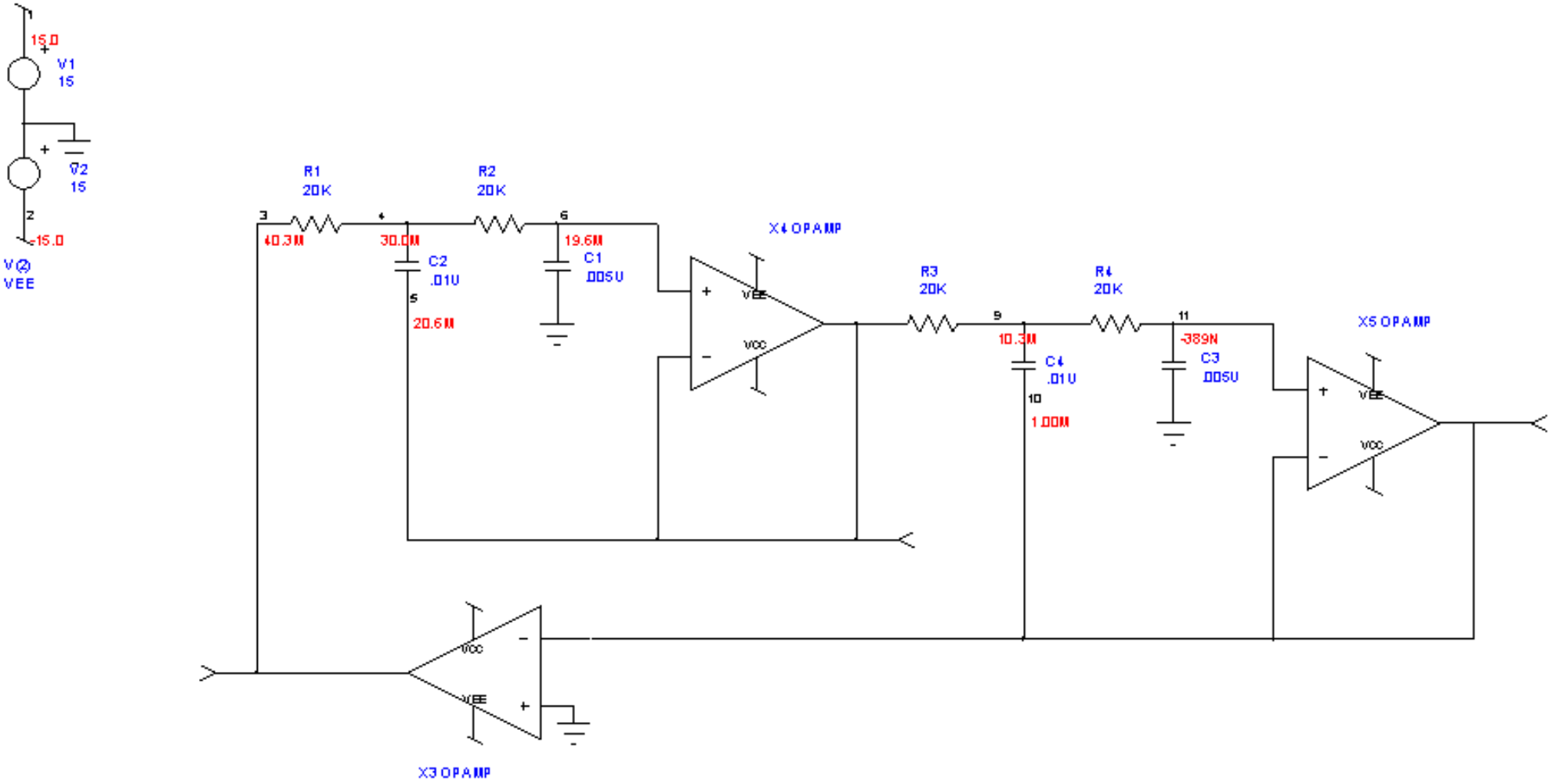


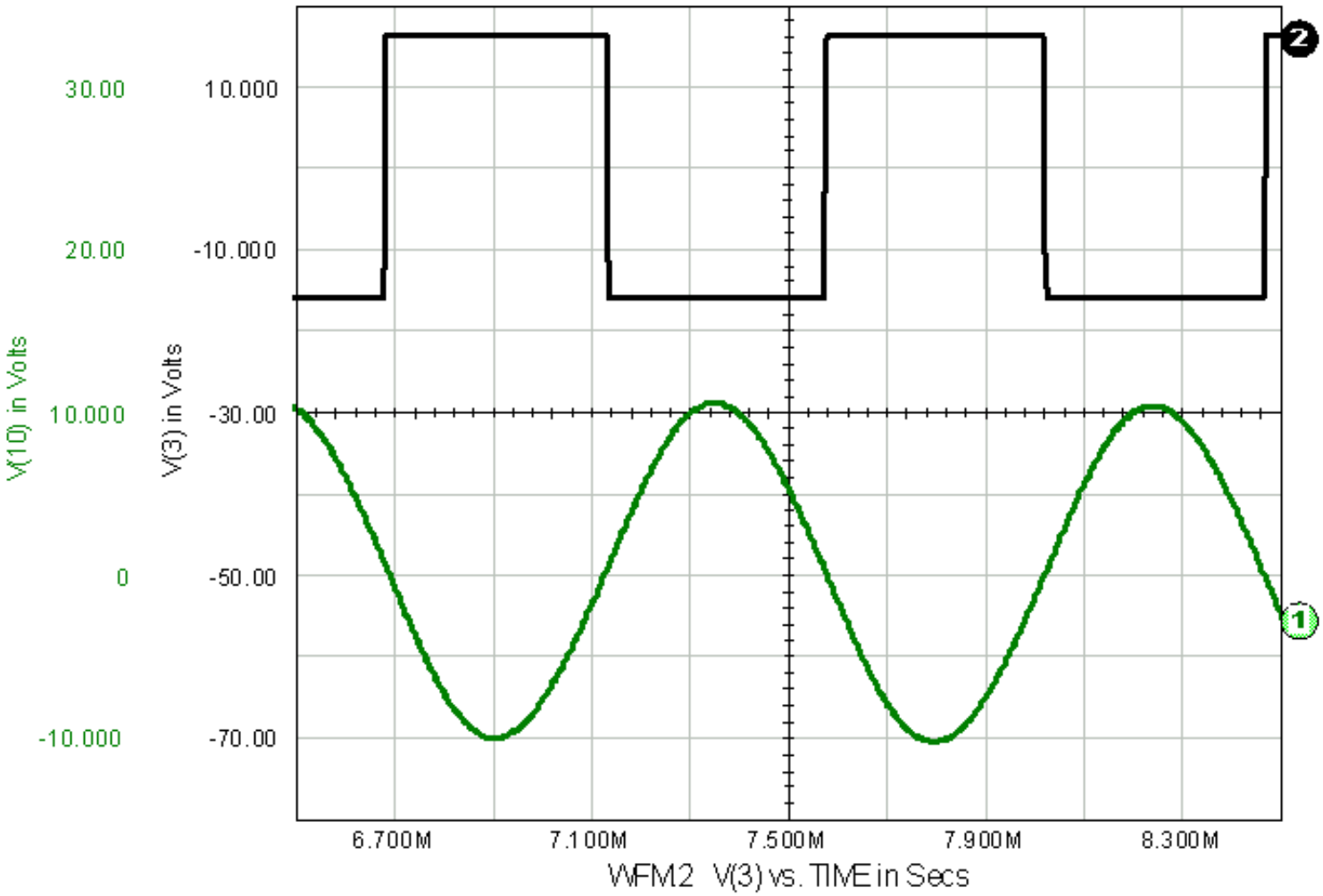
Figure 36-5: Micro-cap resulting waveforms of Inverter oscillator schematic.

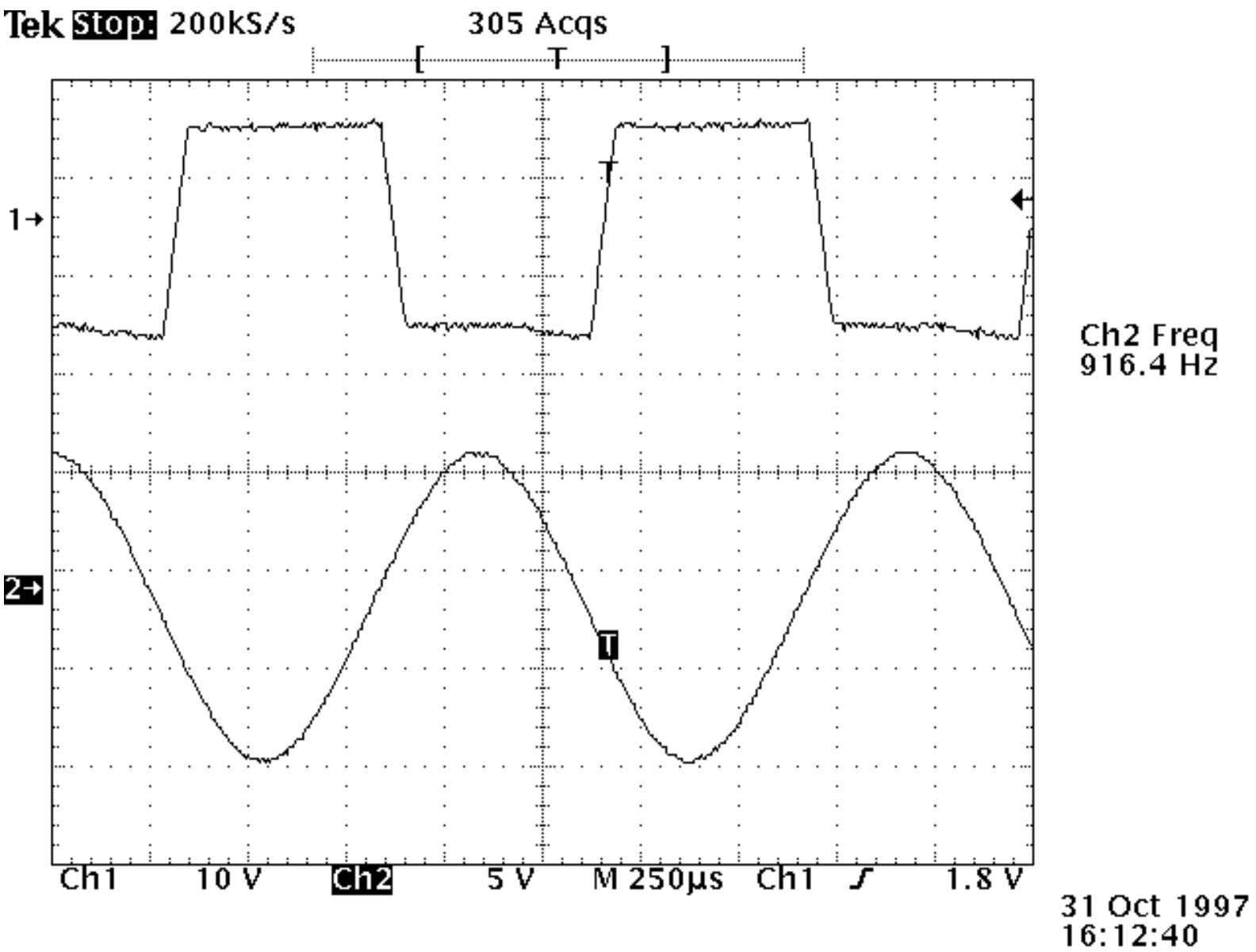
Run Time Summary		
IsSpice v 7.6	PsPice v 6.3	Micro-Cap V v2
4.066 Sec	2.94 Sec	8.85 Sec
Advantages: Low parts count, good drive capability		

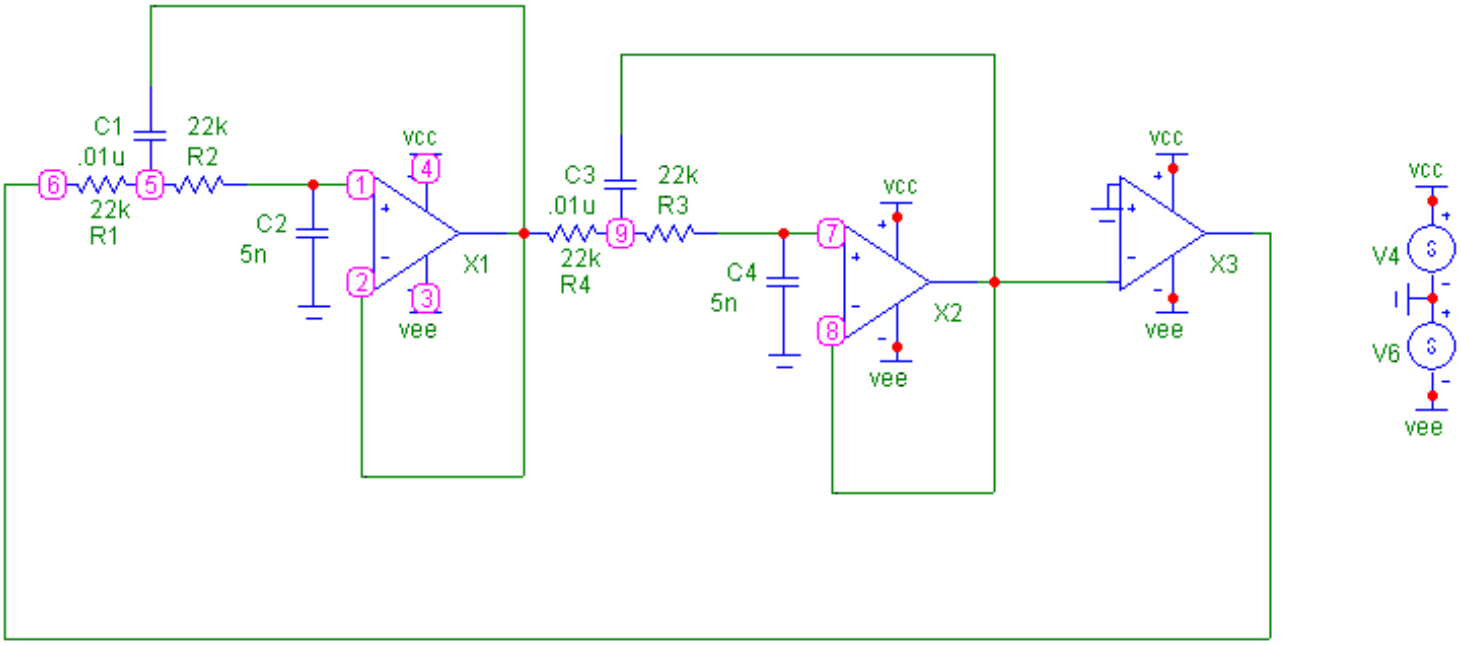
Disadvantages: The accuracy over life, temperature may be unpredictable

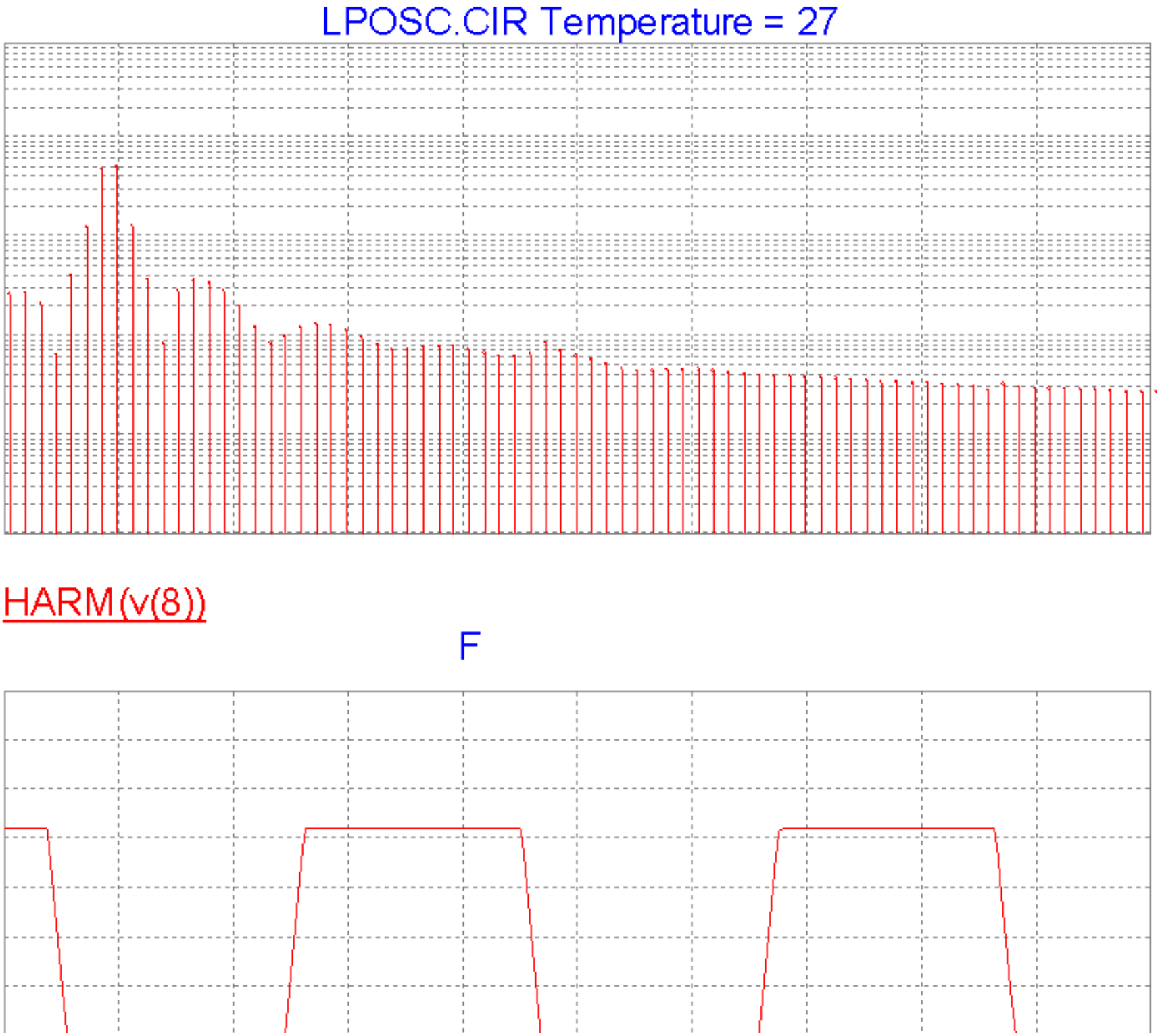
Filenames: 4049osc (IsSpice) ps_4049 (Pspice) mc_4049 (Micro-Cap)

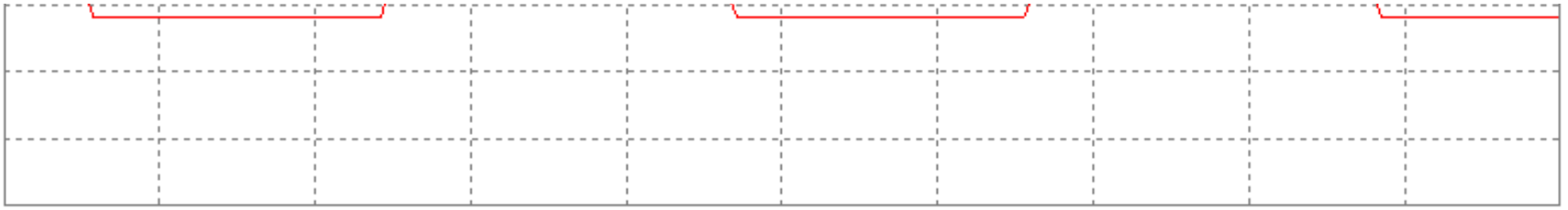

1
15.0
V1
15
2
V2
15
-15.0
V(2)
VEE
R1
20K
R2
20K
3
4
6
40.3M
30.0M
19.6M
C2
.01U
C1
.005U
5
20.6M
X4 OPAMP
VEE
VCC
R3
20K
R4
20K
9
11
10.3M
-389N
C4
.01U
C3
.005U
10
1.00M
X5 OPAMP
VEE
VCC
VCC
VEE
X3 OPAMP


30.00
20.00
10.000
0
-10.000
V(10) in Volts
10.000
-10.000
-30.00
-50.00
-70.00
V(3) in Volts
6.700M
7.100M
7.500M
7.900M
8.300M
WFM2 V(3) vs. TIME in Secs
2
1


Tek Stop: 200kS/s
305 Acqs
1→
2→
Ch2 Freq
916.4 Hz
Ch1 10 V
Ch2 5 V
M 250µs Ch1 ∫ 1.8 V
31 Oct 1997
16:12:40

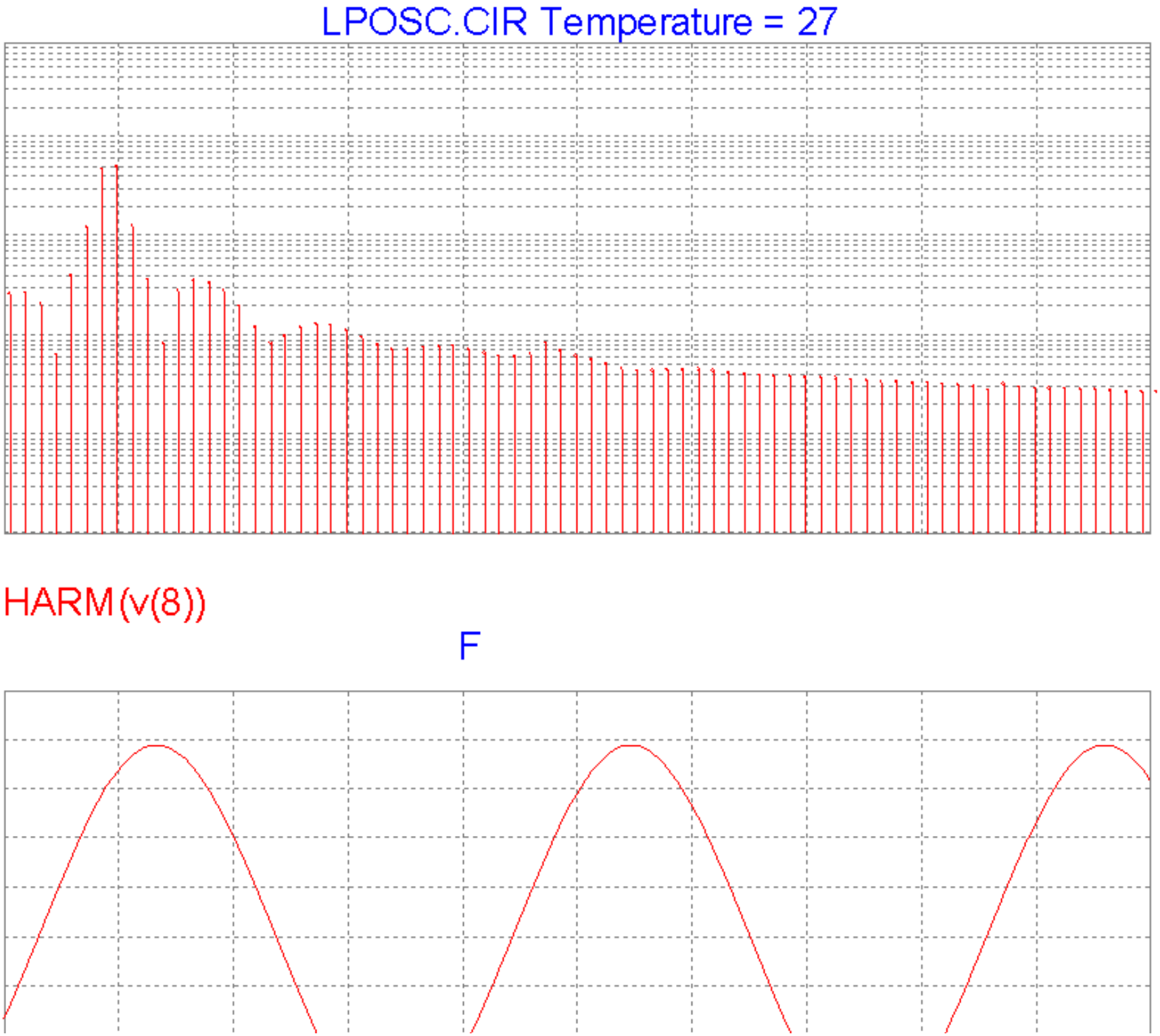

C1
.01u
22k
R2
6
5
22k
R1
C2
5n
vcc
4
1
2
3
vee
X1
C3
.01u
22k
R3
9
22k
R4
C4
5n
vcc
7
8
vee
X2
vcc
vee
X3
vcc
V4
I
V6
vee

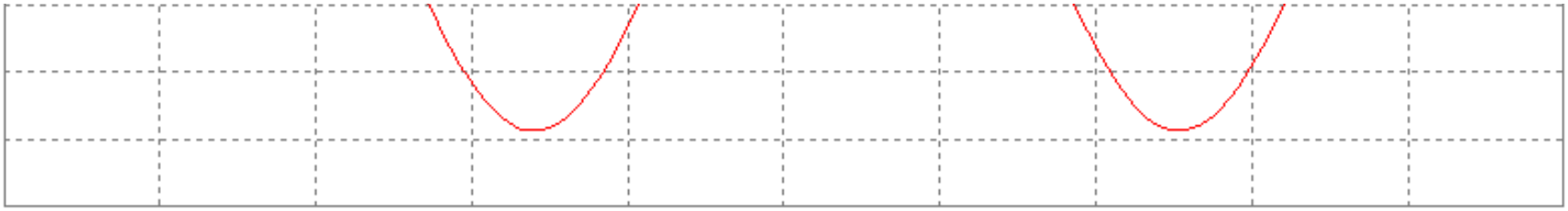

LPOSC.CIR Temperature = 27
HARM(v(8))
F



V(6)

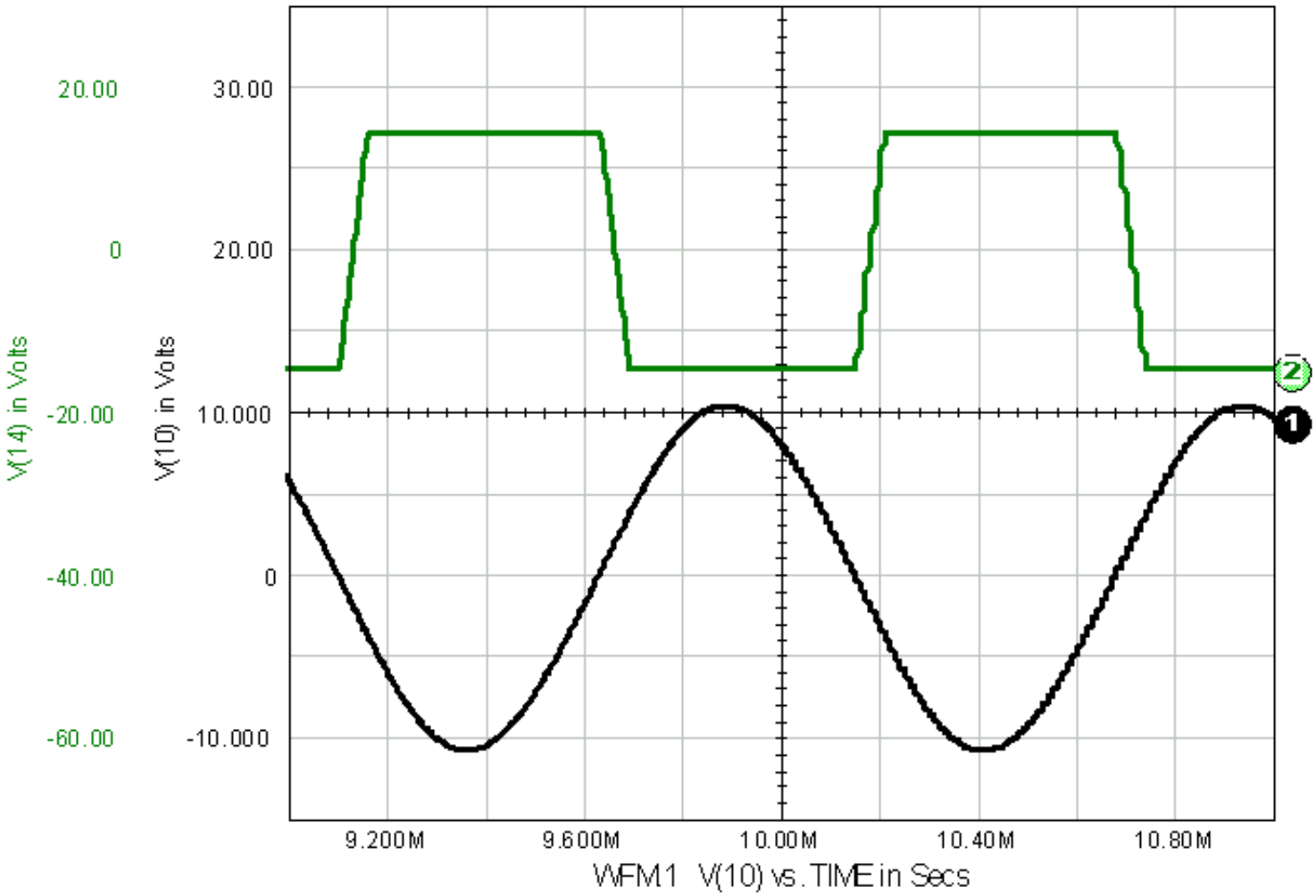
F

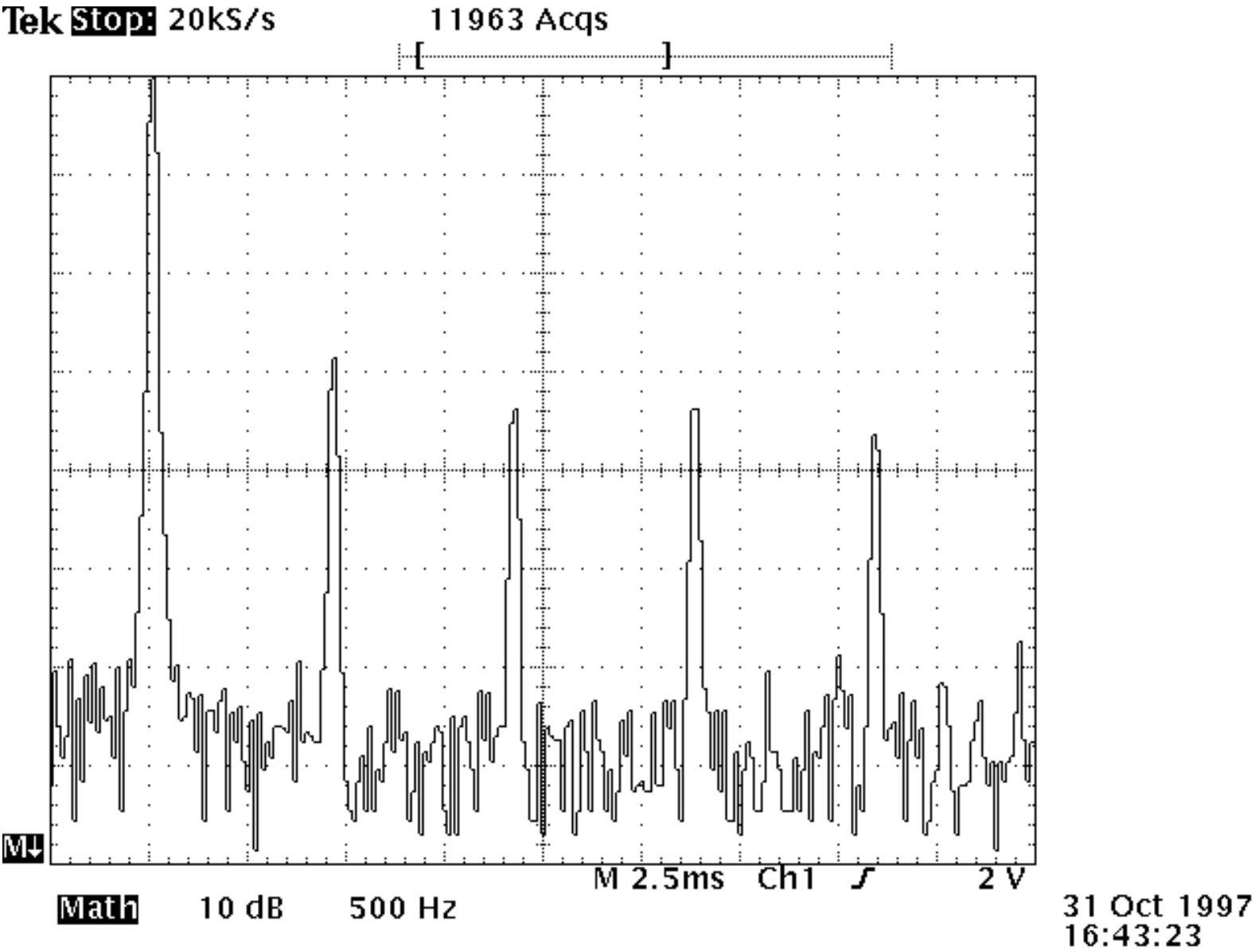

LPOSC.CIR Temperature = 27
HARM(v(8))
F

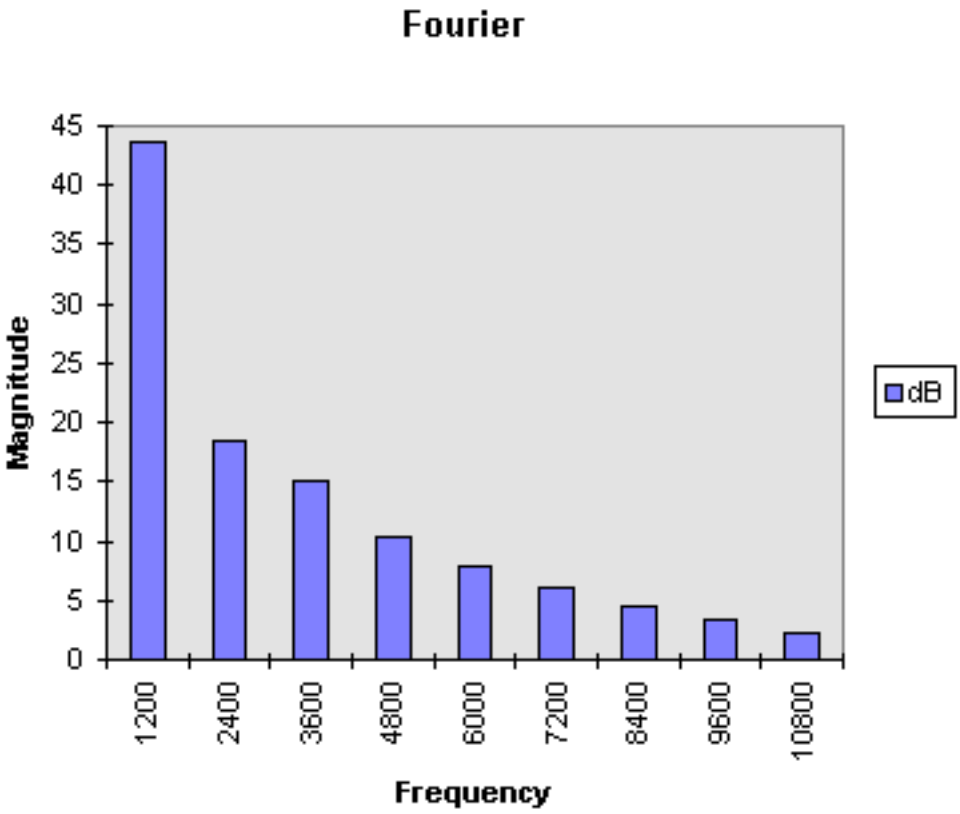


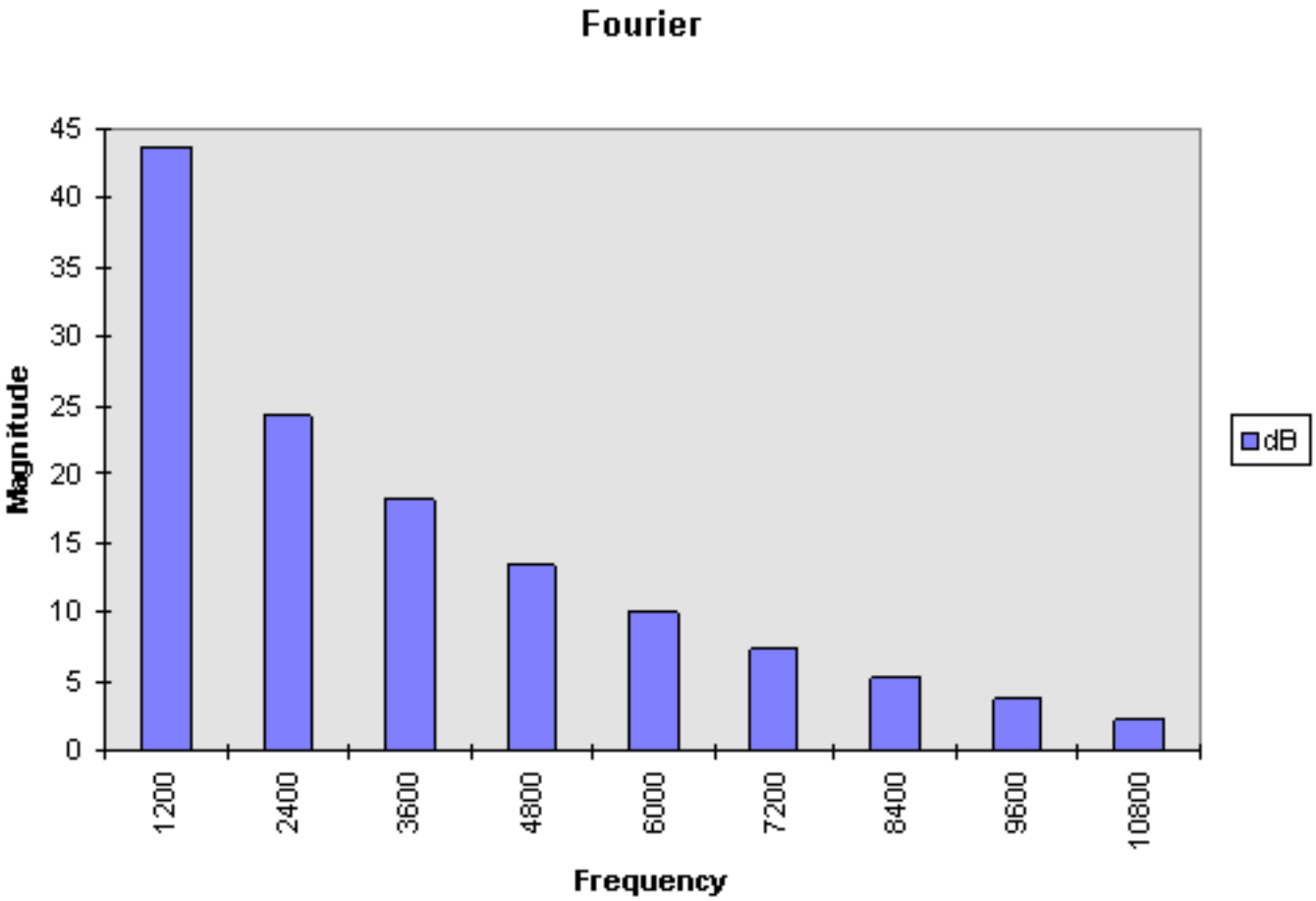
V(8)

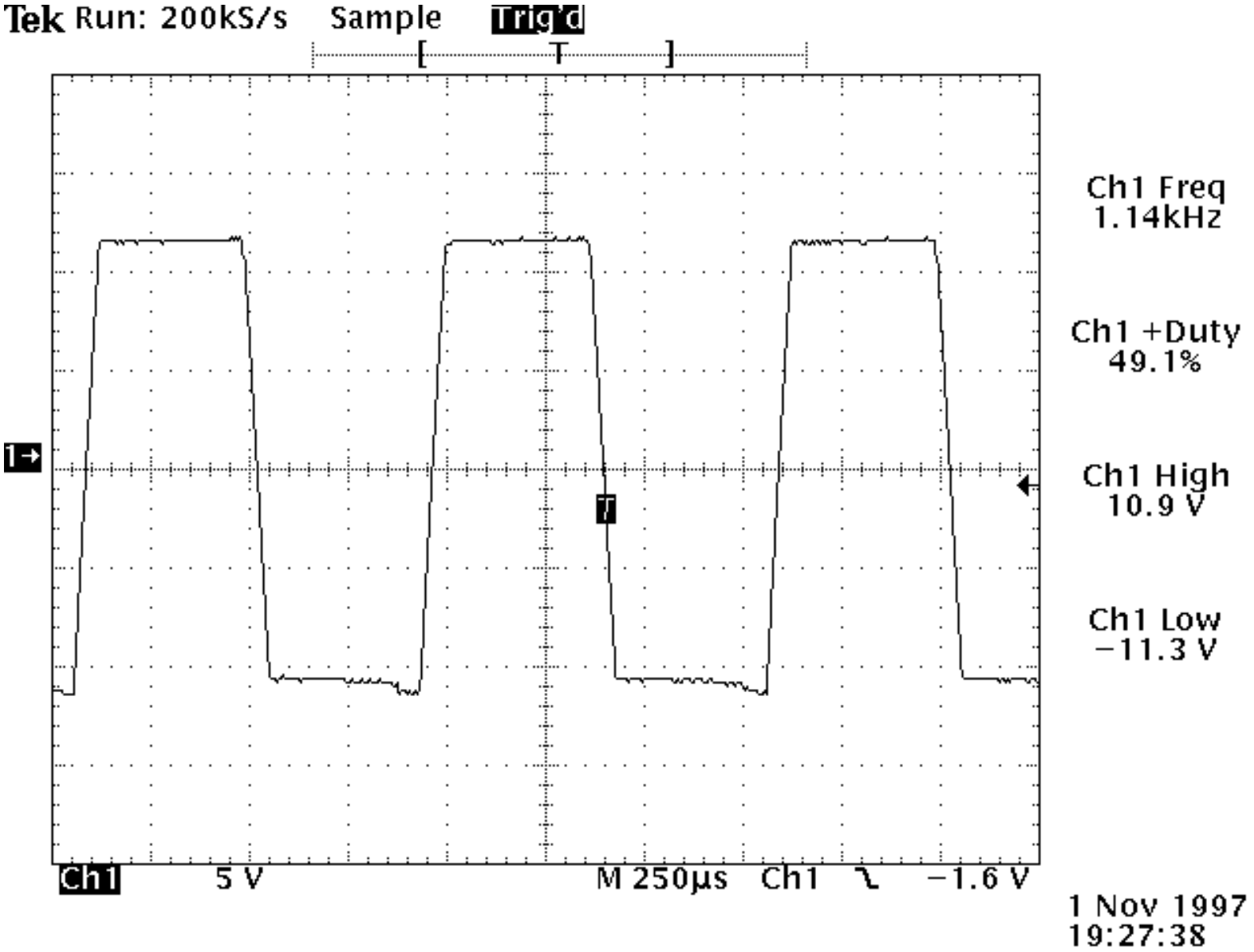
F

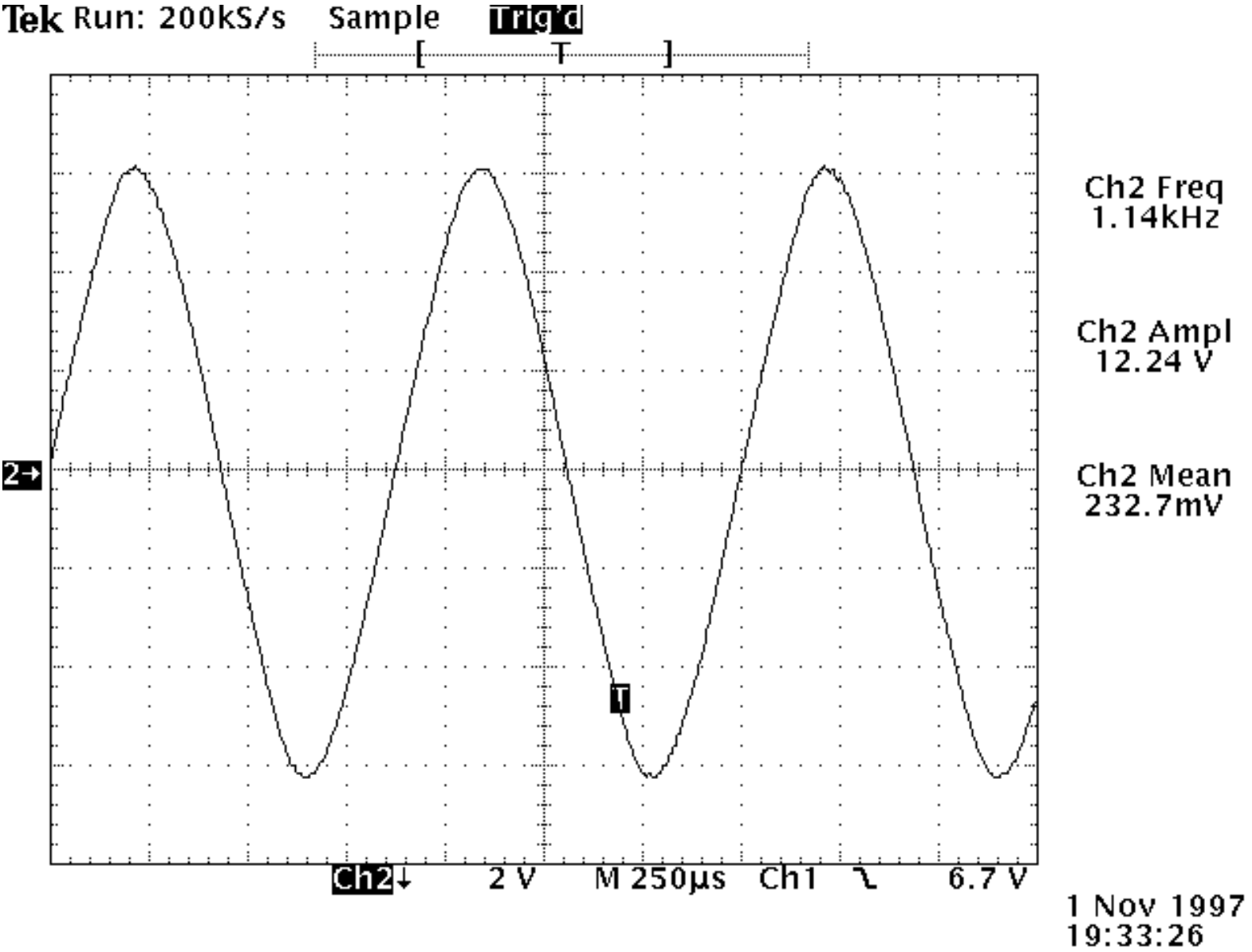

20.00
0
-20.00
-40.00
-60.00
V(14) in Volts
30.00
20.00
10.000
0
-10.000
V(10) in Volts
9.200M
9.600M
10.00M
10.40M
10.80M
WFM1 V(10) vs. TIME in Secs
2
1


Tek Stop: 20kS/s
11963 Acqs
M↓
M 2.5ms Ch1 ∫ 2 V
Math 10 dB 500 Hz
31 Oct 1997
16:43:23


Fourier
Magnitude
45
40
35
30
25
20
15
10
5
0
1200
2400
3600
4800
6000
7200
8400
9600
10800
Frequency
dB


Fourier
Magnitude
45
40
35
30
25
20
15
10
5
0
1200
2400
3600
4800
6000
7200
8400
9600
10800
Frequency
dB


Tek Run: 200kS/s Sample Trig'd
Ch1 Freq
1.14kHz
Ch1 +Duty
49.1%
Ch1 High
10.9 V
Ch1 Low
−11.3 V
Ch1 5 V
M 250µs Ch1 ⌊ −1.6 V
1 Nov 1997
19:27:38


Tek Run: 200kS/s Sample Trig'd
Ch2 Freq
1.14kHz
Ch2 Ampl
12.24 V
Ch2 Mean
232.7mV
2→
T
Ch2↓ 2 V M 250µs Ch1 ⌊ 6.7 V
1 Nov 1997
19:33:26

#37: 4th order Butterworth no offset Low Pass Oscillator

Very similar to the circuit in Figure 35-1, the difference being there is no DC offset in this circuit. The schematic is shown in Figure 37-1. This has the benefit of the harmonics distortion not being sensitive to the Vcc/Vee parameters of the operational amplifier. Two matched zener diodes (1N4735A 6.2 volts were used in the lab circuit) across the operational amplifier clamp the output to roughly equal levels. The resistor R9 limits the current through the clamping diodes. Figure 37-2 is the clamped square wave generated at node '13'. The resultant sine wave after filtering at node '10' is shown in Figure 37-4. The lab results are shown in Figure 37-3 and Figure 37-5.

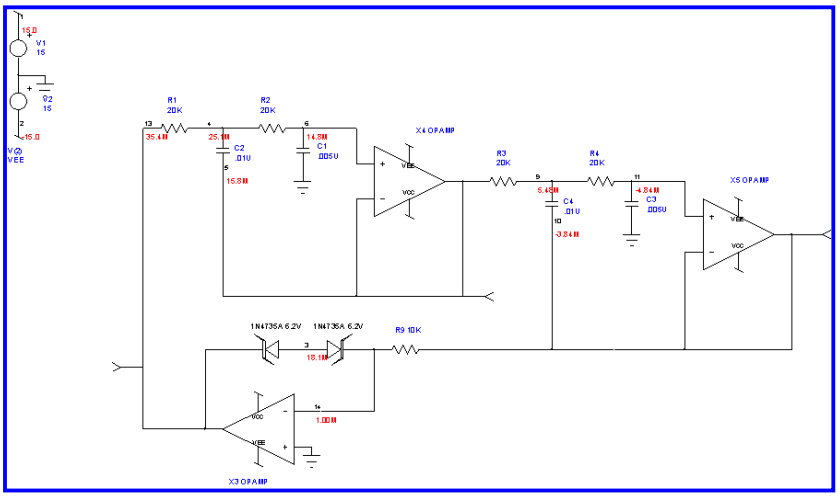


Figure 37-1: 4th order Butterworth no offset Low Pass Oscillator

order Butterworth no offset Low Pass Oscillator

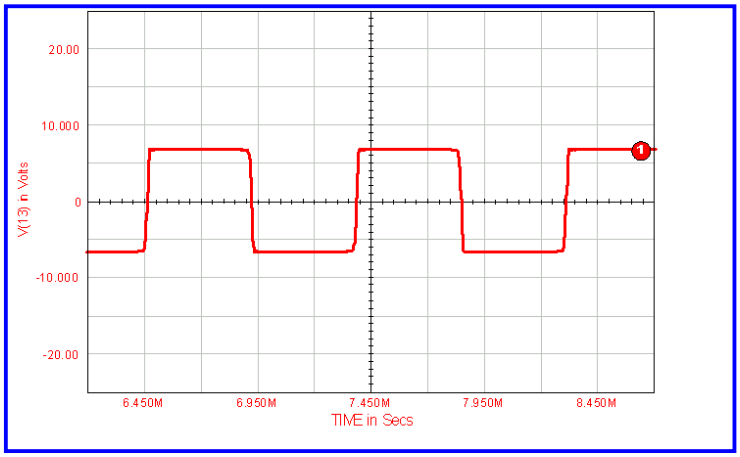


Figure 37-2: Clamped square wave at node 13

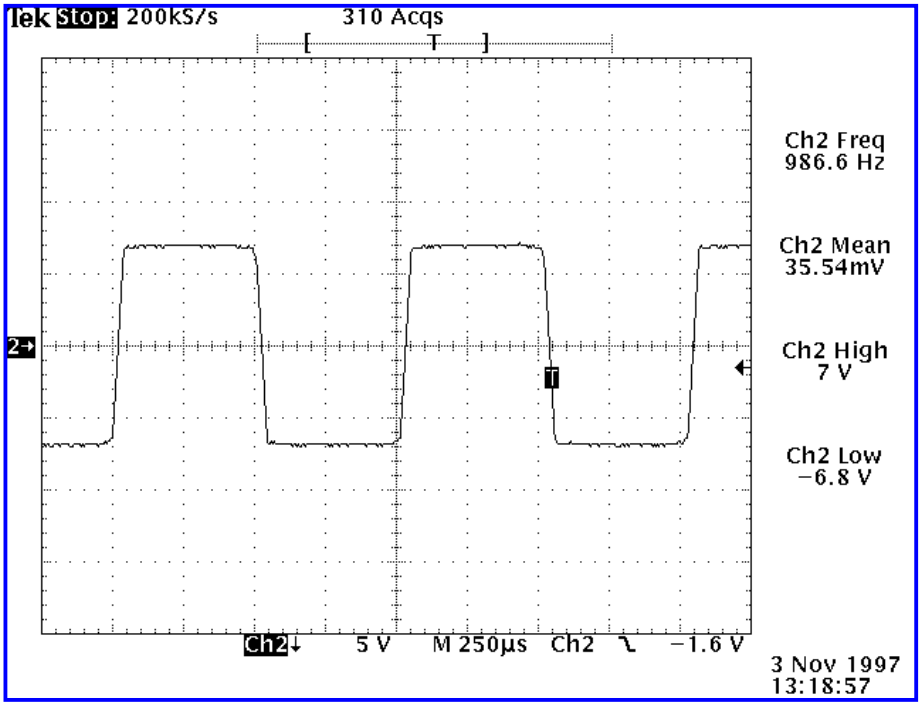


Figure 37-3: Lab results of Butterworth no offset Low Pass Oscillator

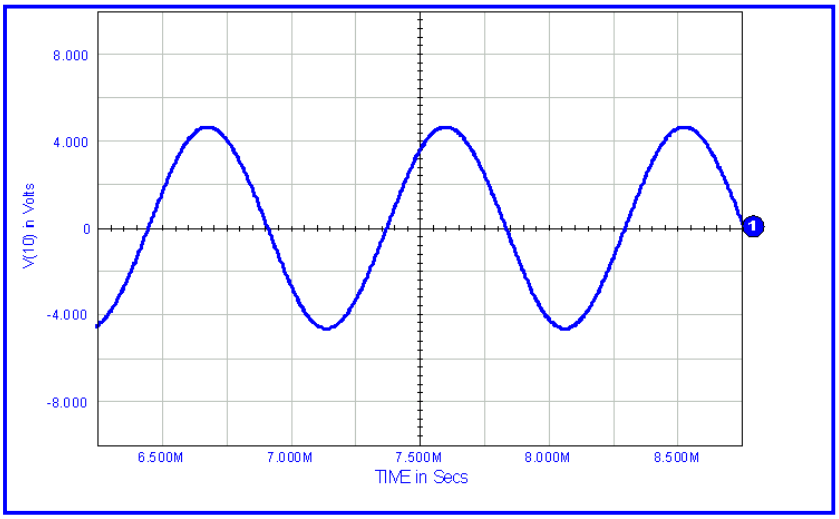


Figure 37-4: Sine wave output at node 10

order Butterworth no offset Low Pass Oscillator

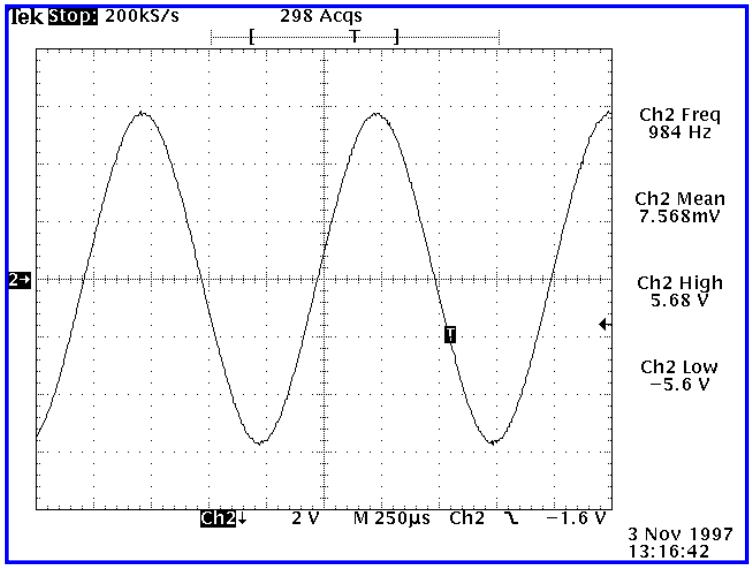


Figure 37-5: Lab results of Butterworth no offset Low Pass Oscillator

- Simulation tip: The amplitude of the spice model result has about a 1 volt offset missing from the result. This is due to the forward drop of the zener diode, which is not typically modeled in zener diode models. It is not difficult to model this parameter, but since the purpose was to show the zero offset result, it is not important here.

The same circuit was simulated in Pspice and Micro-Cap. The results are shown in Figures 37-34 through 37-37.

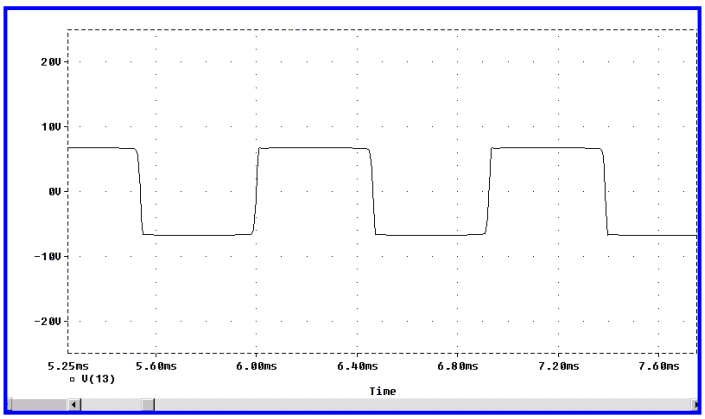


Figure 37-6: Pspice result of Butterworth no offset Low Pass Oscillator

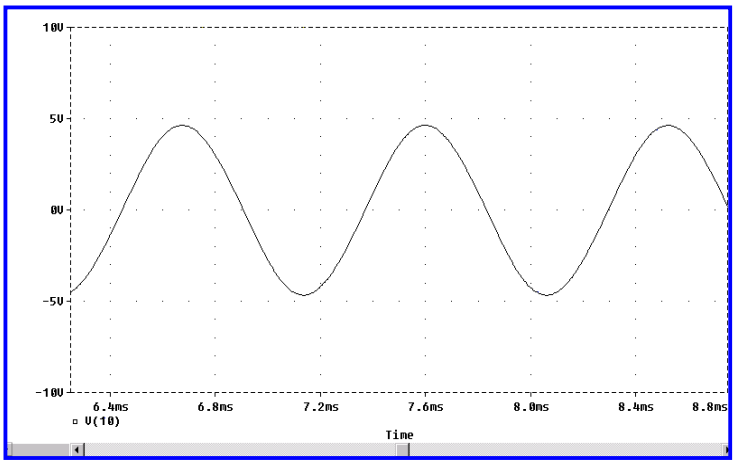


Figure 37-7: Pspice result of Butterworth no offset Low Pass Oscillator

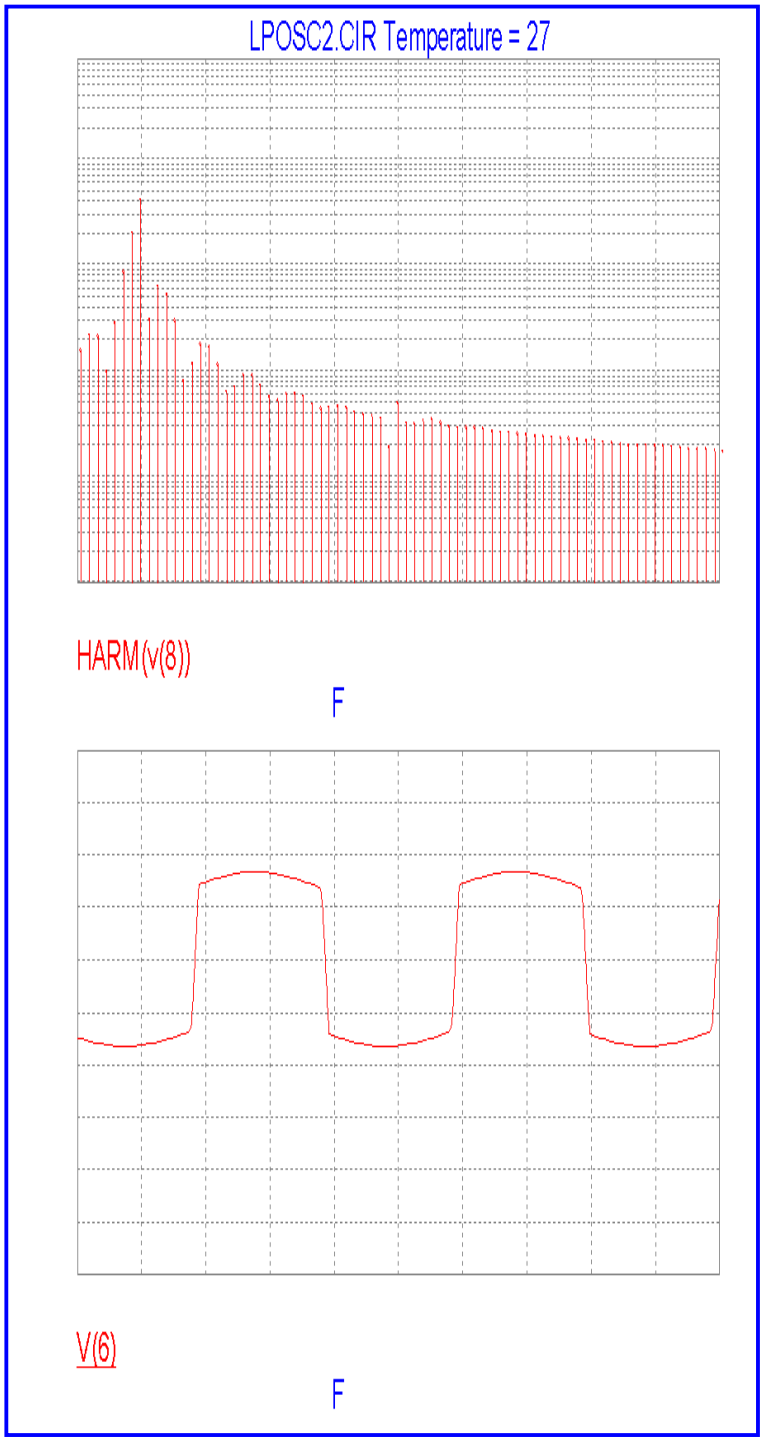


Figure 37-8: Micro-Cap result of Butterworth no offset Low Pass Oscillator

order Butterworth no offset Low Pass Oscillator

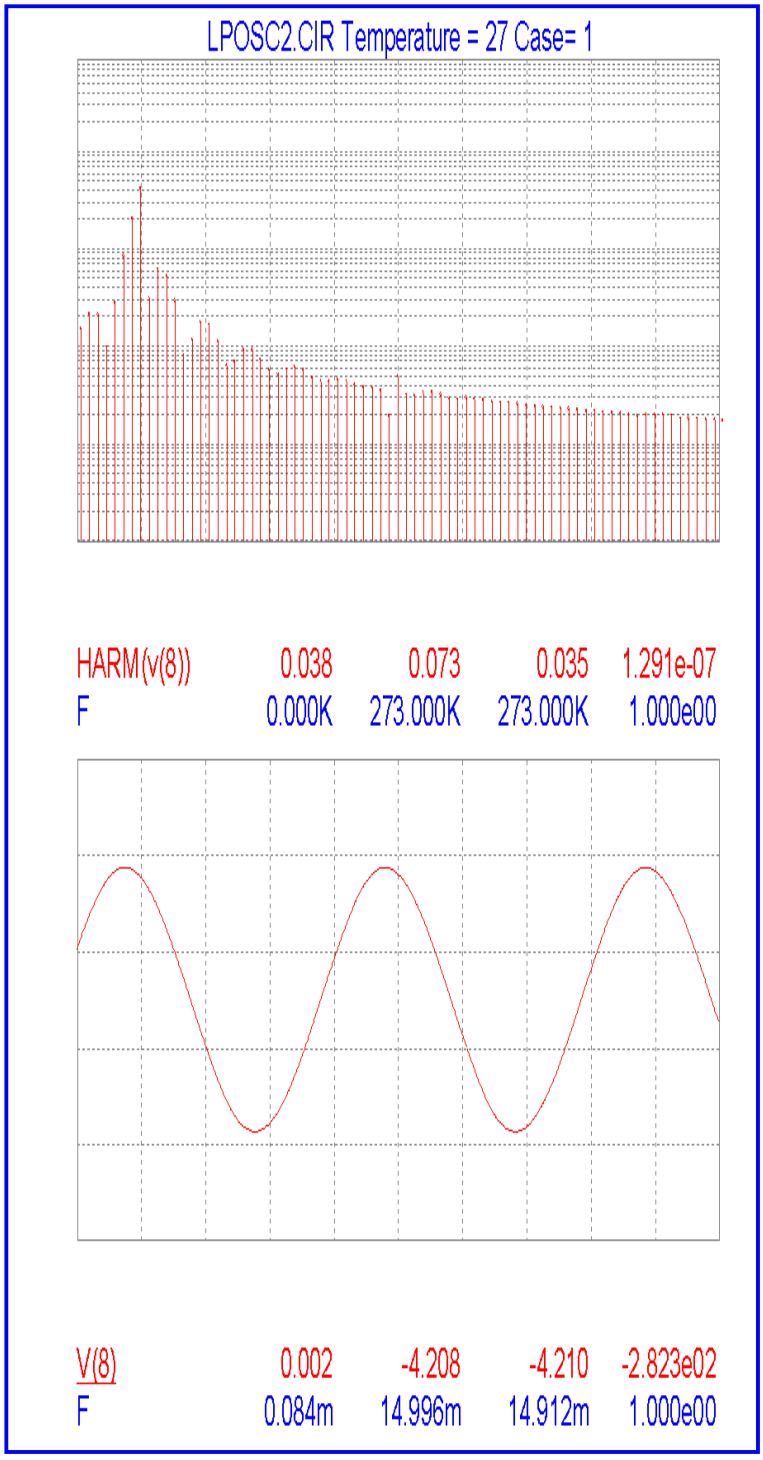


Figure 37-9: Micro-Cap result of Butterworth no offset Low Pass Oscillator

The Fourier result was also calculated. The hardware result is shown in Figure 37-38 and the results from the simulators are shown in Figures 37-39 through 37-41.

order Butterworth no offset Low Pass Oscillator

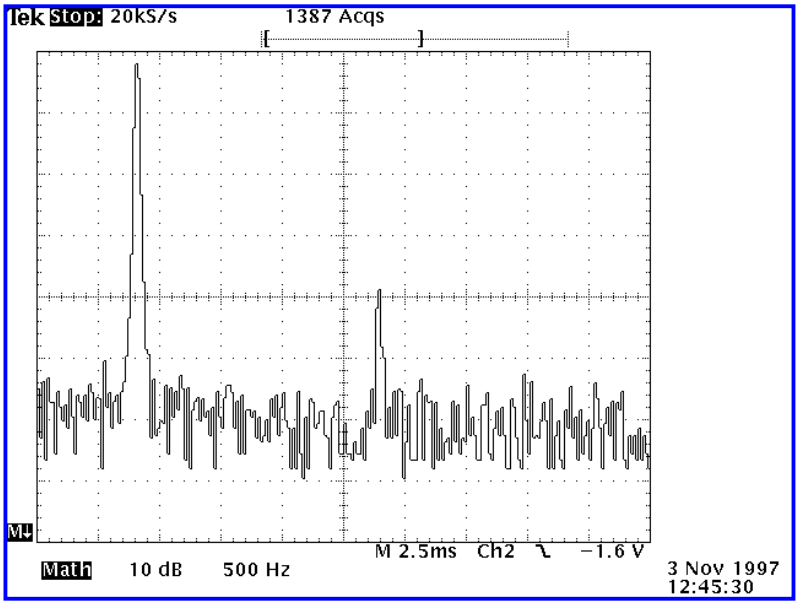


Figure 37-10: Lab data Fourier Analysis result of output sine wave

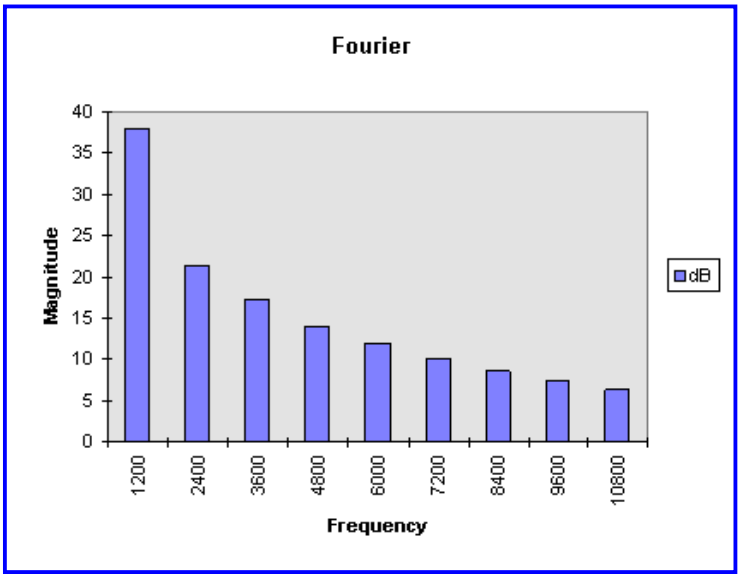
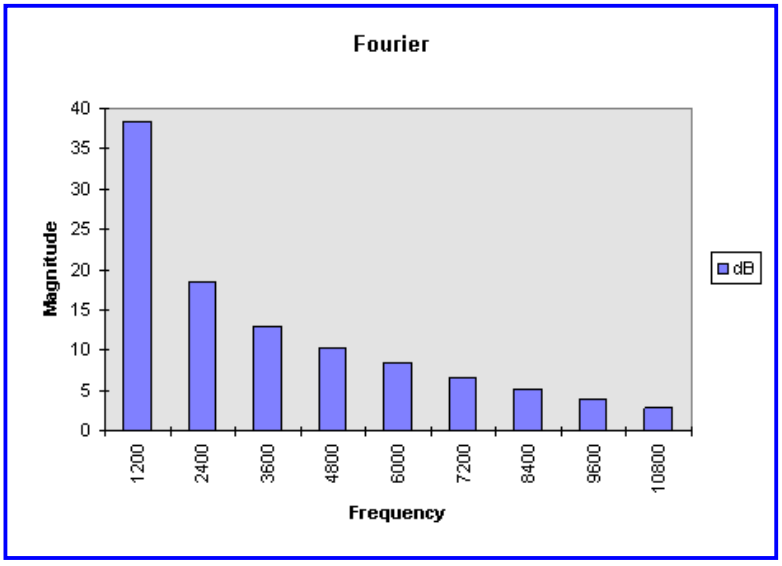


Figure 37-11: IsSpice Fourier Analysis results



order Butterworth no offset Low Pass Oscillator

Figure 37-12: Pspice Fourier Analysis results

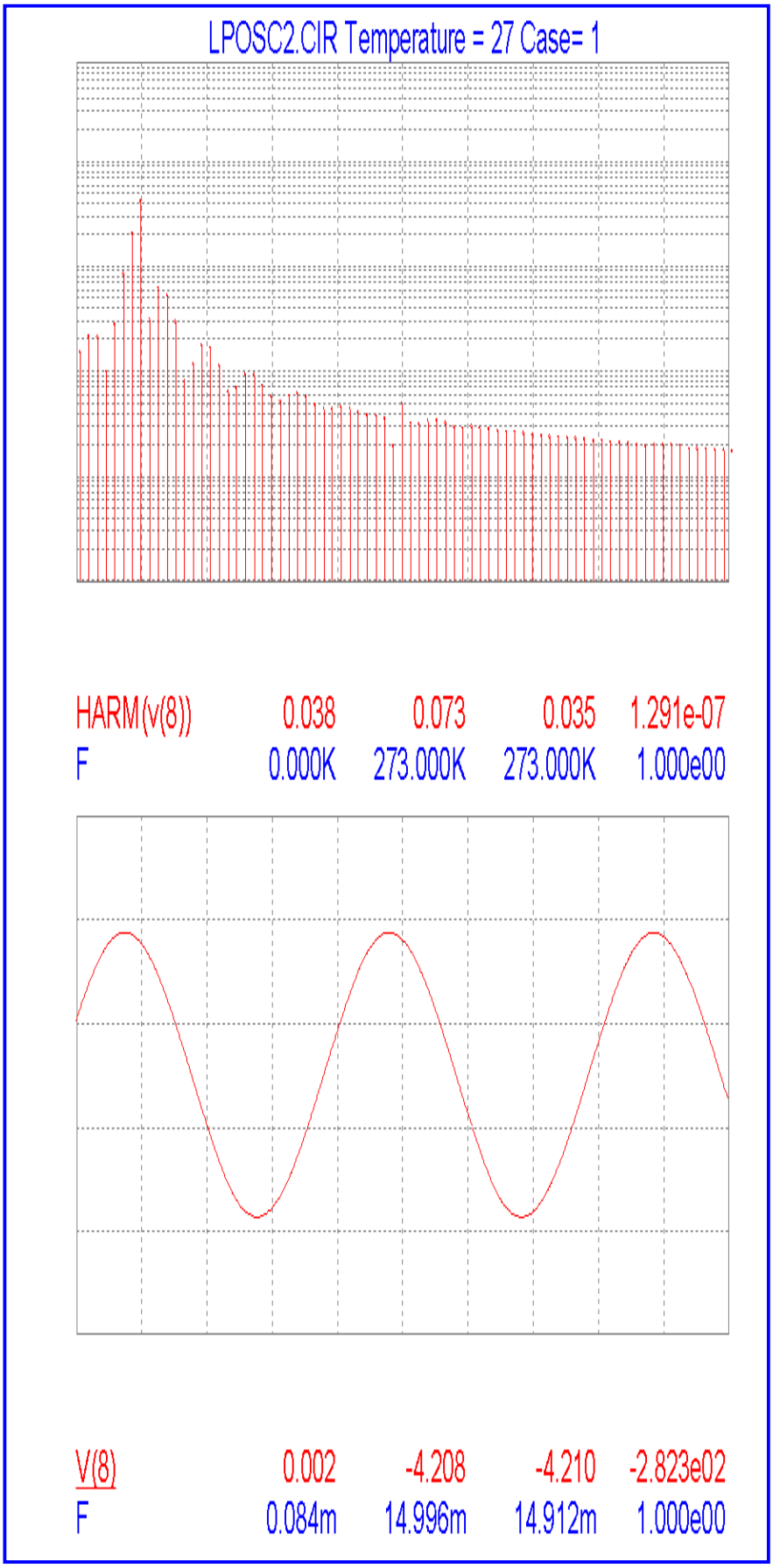


Figure 37-13: Micro-Cap Fourier Analysis results

Notice in the Fourier results, the 2nd harmonic is now greatly attenuated. The

hardware circuit used 5% tolerance resistors, causing the simulation frequency to be slightly off. Another simulation was run with the exact resistor values of the hardware circuit in order to show the accuracy of the model. The schematic is shown in Figure 37-14 and the resulting waveform is shown in Figure 37-15.

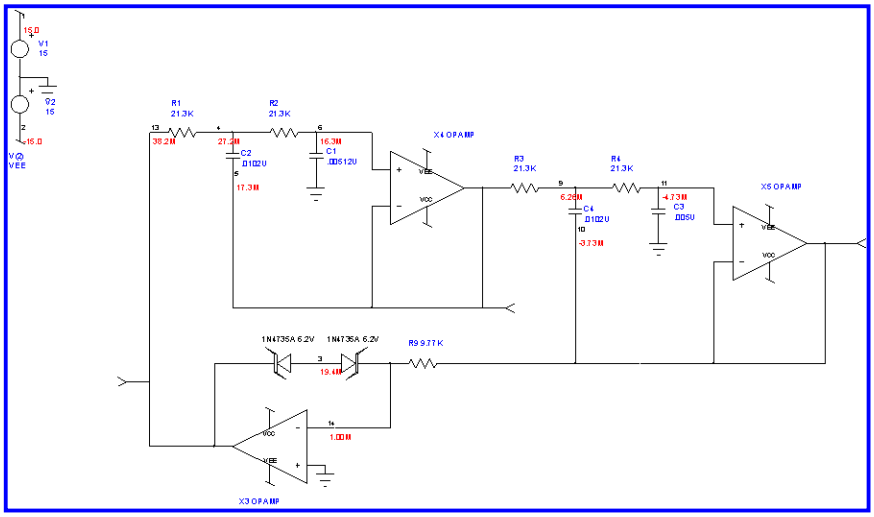


Figure 37-14: More Exact simulation circuit

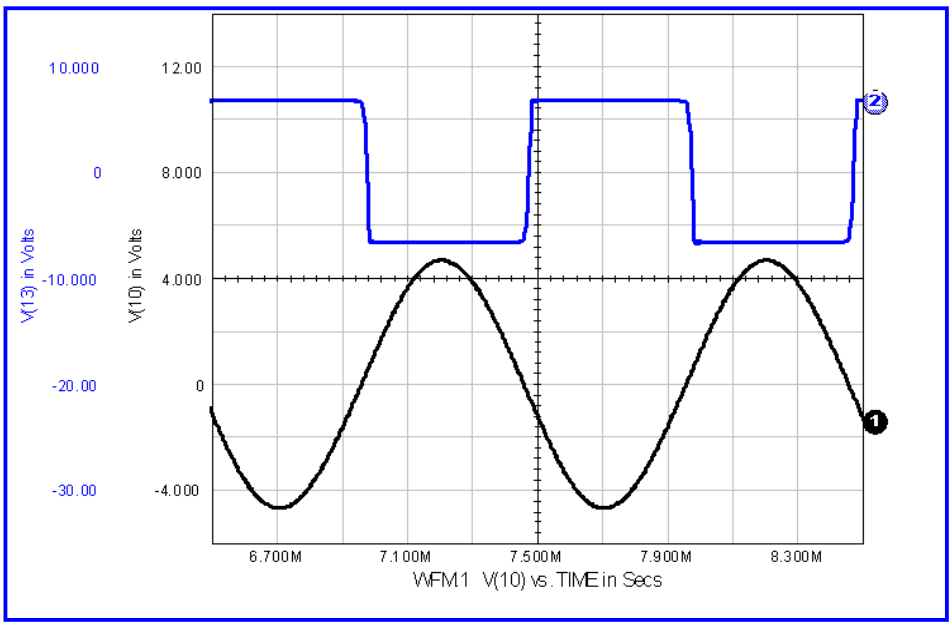


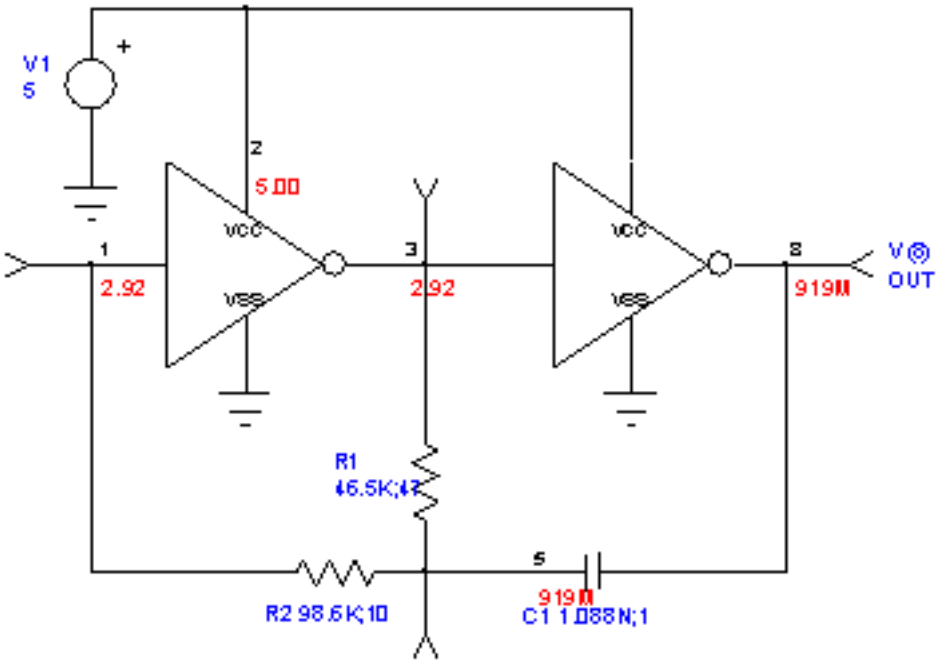
Figure 37-15: More Exact simulation results

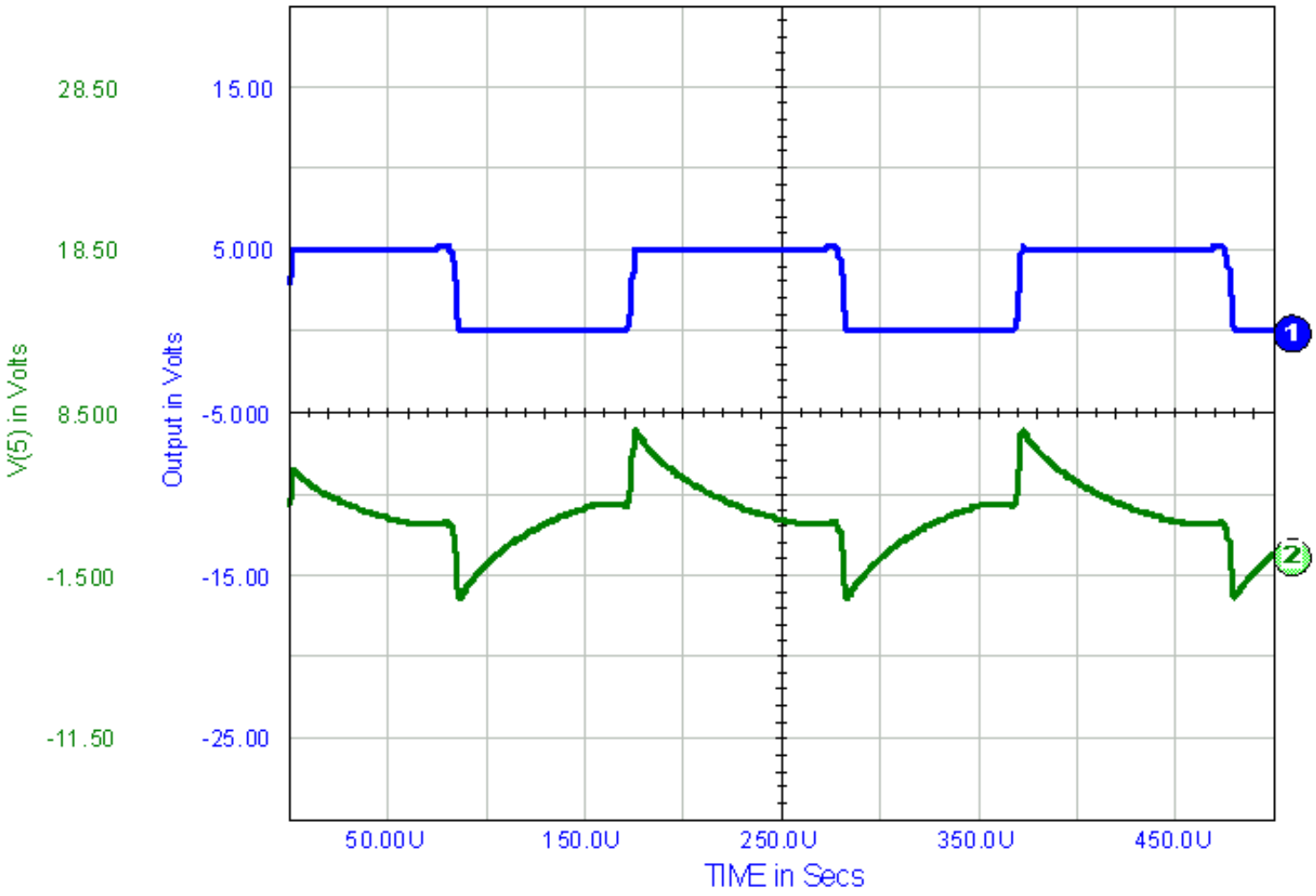
Run Time Summary		
IsSpice v 7.6	PsPice v 6.3	Micro-Cap V v2
8.966 Sec	12.25 Sec	34.52 Sec
Advantages: Good long term frequency stability, moderate distortion, easily adjusted, moderate drive capability		

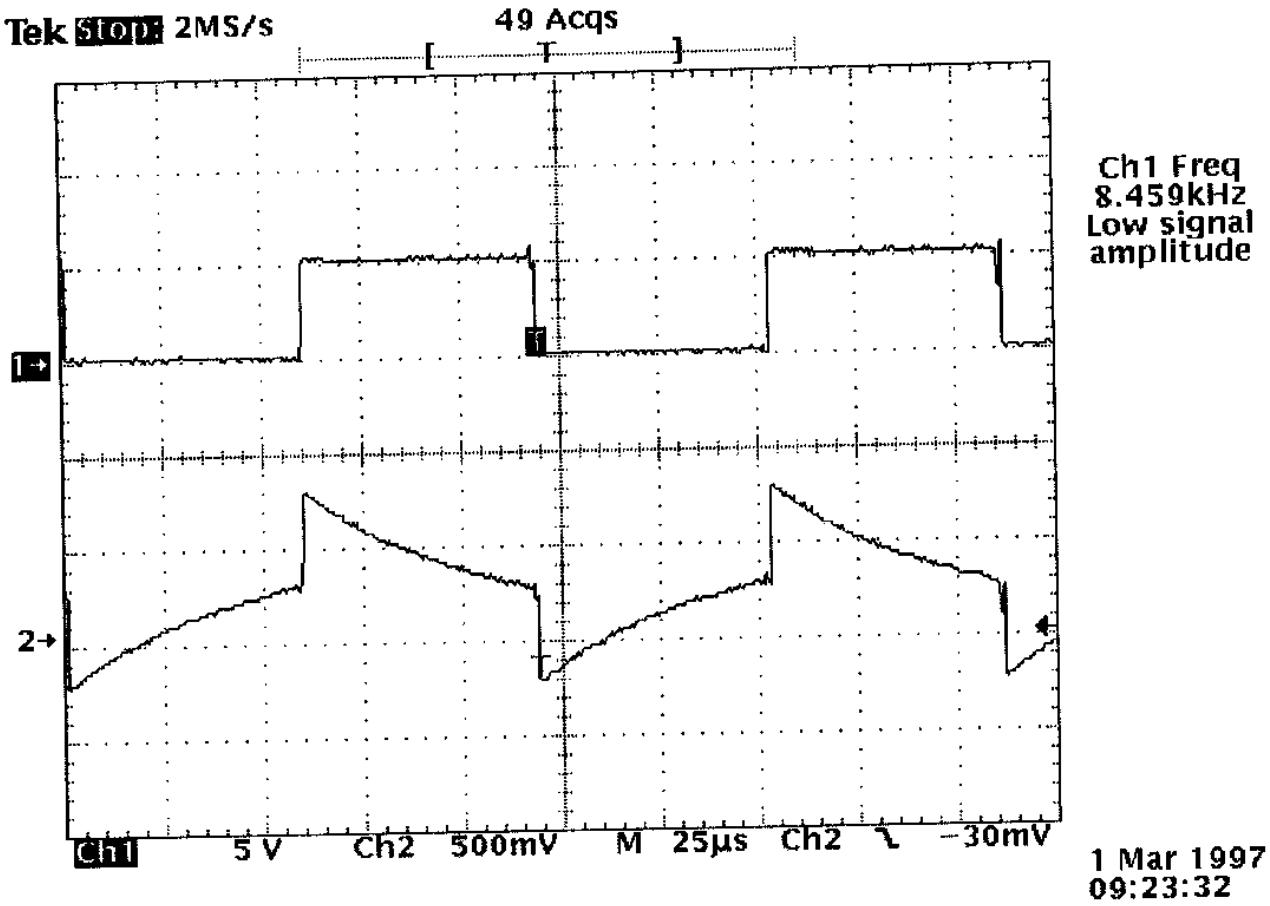
order Butterworth no offset Low Pass Oscillator

Disadvantages: High parts count

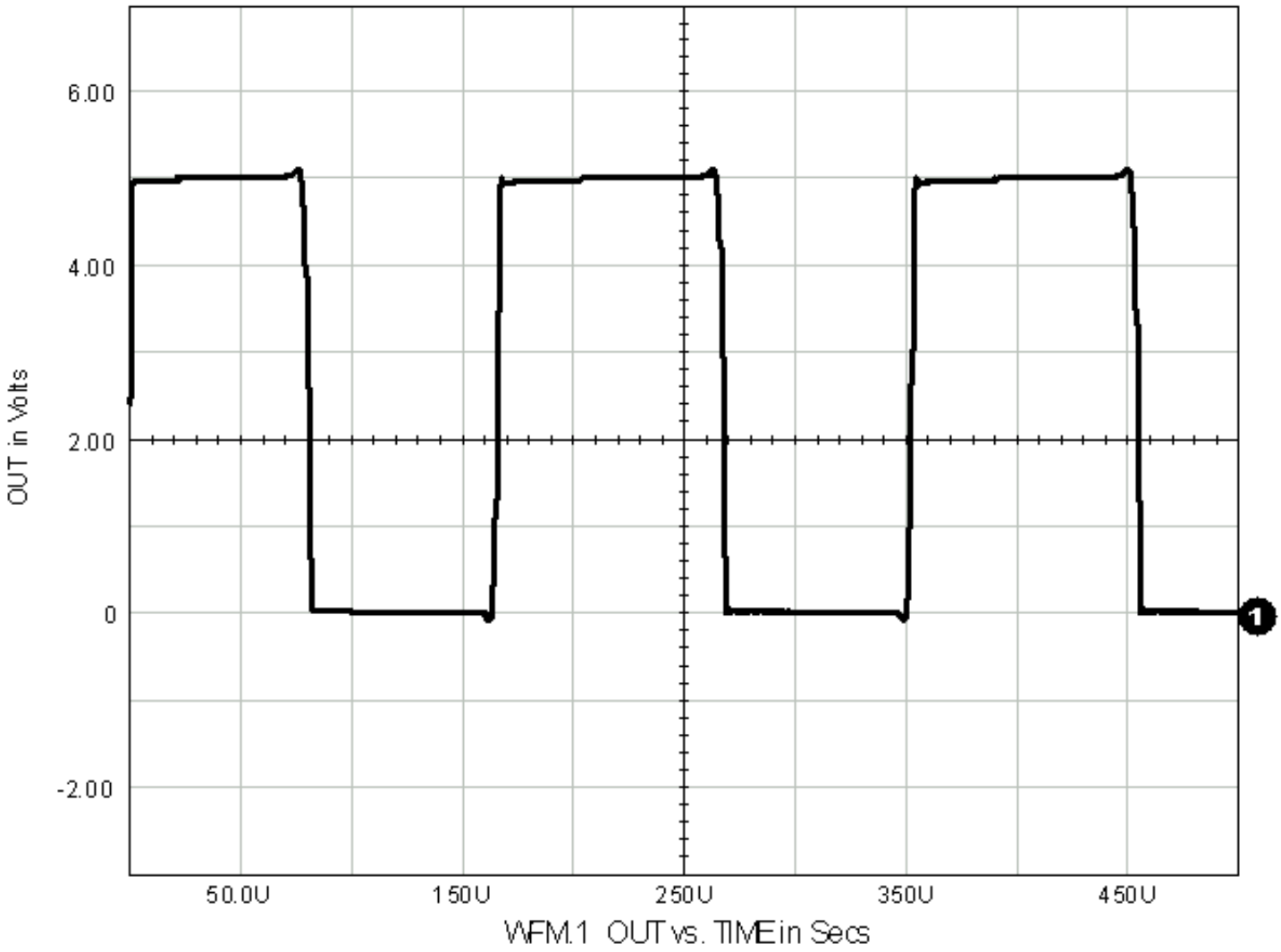
Filenames: lm_osc2 lm_osc2a (IsSpice) ps_osc2 (Pspice) lposc2 (Micro-Cap) four.xls (Excel)

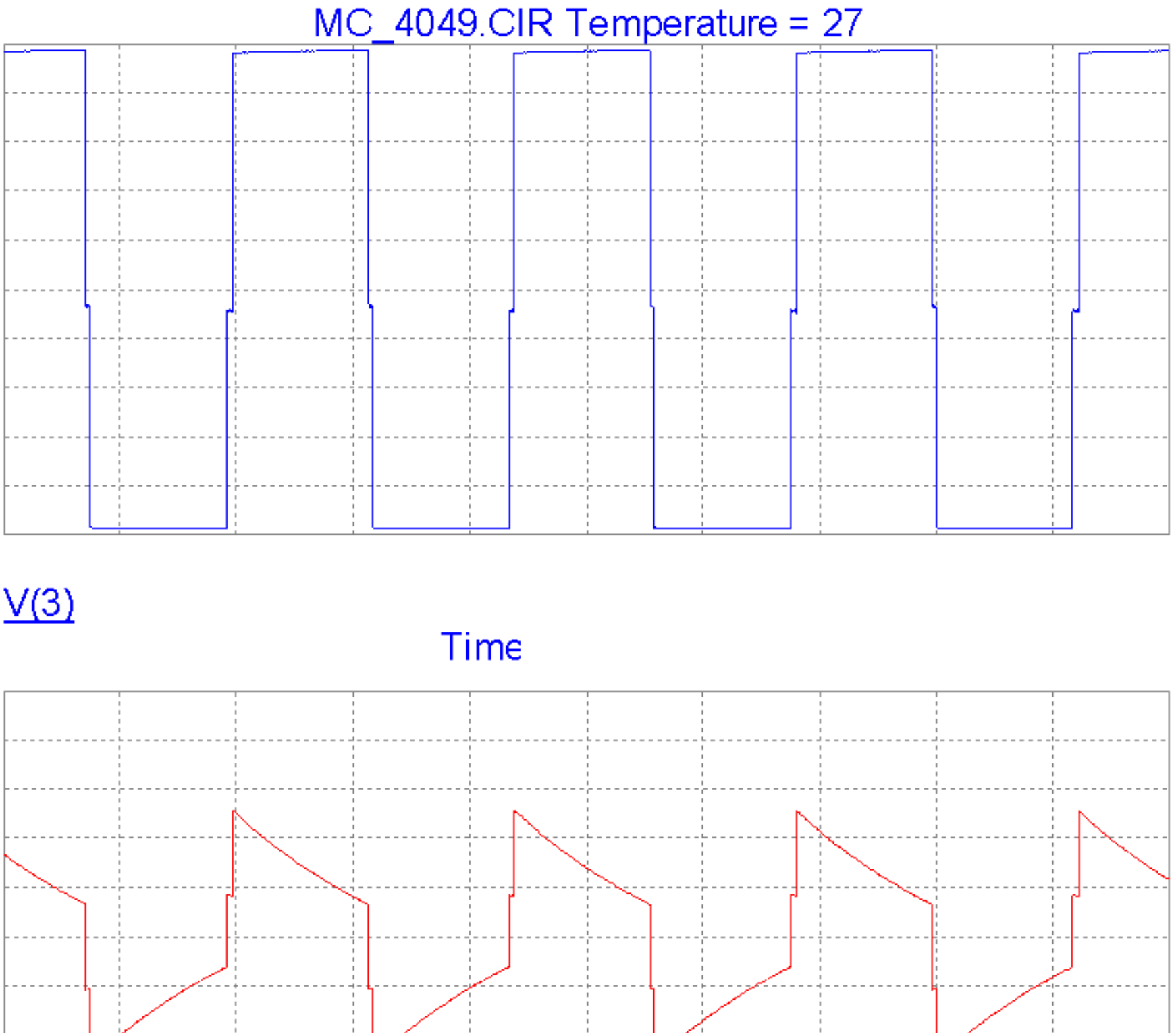

V1
5
+
2
5.00
VCC
VSS
1
2.92
3
2.92
VCC
VSS
4
919m
V@
OUT
R1
46.5K;42
5
919m
R2 98.6K;10
C1 1.088N;1

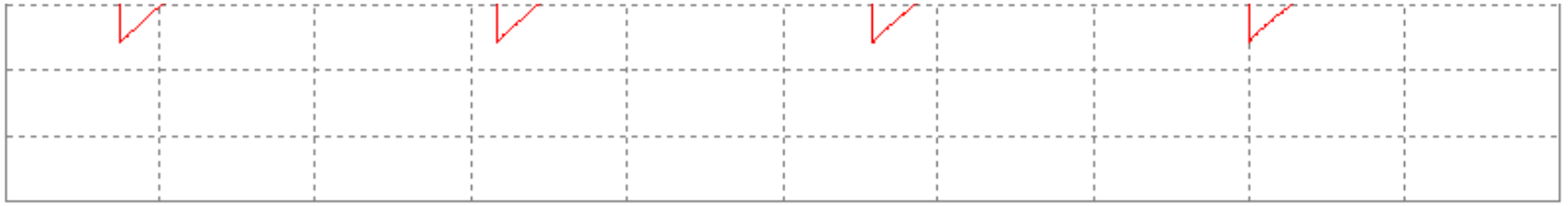

28.50
18.50
8.500
-1.500
-11.50
V(5) in Volts
15.00
5.000
-5.000
-15.00
-25.00
Output in Volts
1
2
50.00U
150.0U
250.0U
350.0U
450.0U
TIME in Secs



Top - Output
Bottom - Ramp


6.00
4.00
2.00
0
-2.00
OUT in Volts
50.0U
150U
250U
350U
450U
WFM.1 OUT vs. TIME in Secs
1


MC_4049.CIR Temperature = 27
V(3)
Time



V(2)

Time

#38: Harmonic Neutralized Sine Wave

This circuit is generated from a series of square wave pulses. Square waves are easier to generate than sine waves, and can accurately be produced by of digital logic integrated circuits. This circuit generates a series of square wave pulses, skewed in time and summed. This resultant summed waveform resembles a stepped representation of a sinusoidal wave. This waveform is passed through a filter and the final signal is a clean sine wave.

This version of the Harmonic Neutralized sine wave Oscillator uses a series of flip flop gates, configured as a shift register (supplied by an 74HC174 Integrated circuit) and an inverter (supplied by a CD4049) to provide the skewed square wave pulses. The schematic for the harmonic neutralized sine wave is shown in Figure 38-1.

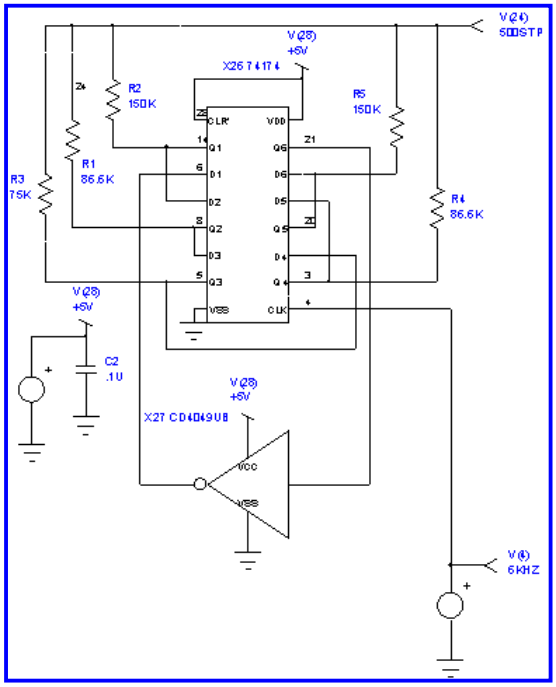


Figure 38-1: Schematic of multi-phase square wave generator

A 6 Khz square wave pulse from a function generator is fed into the clock of the 74HC174. Each of the outputs of the flip flops are summed in such a way as to eliminate the 3rd, 5th, 7th , and 9th harmonics. This is of great importance when attempting to filter the sine wave. The elimination of the 3rd, 5th, 7th , and 9th harmonics greatly simplifies the design of the output filter. The resulting sum of

this signal is shown in Figure 38-4. The top waveform in Figure 38-4 is the 6 Khz input square wave. The bottom waveform is the resultant quasi-square output waveform.

The skewed outputs of the 74HC174 are shown in Figure 38-4. The results of the simulation of this circuit is shown in Figure 38-3 and 38-5.

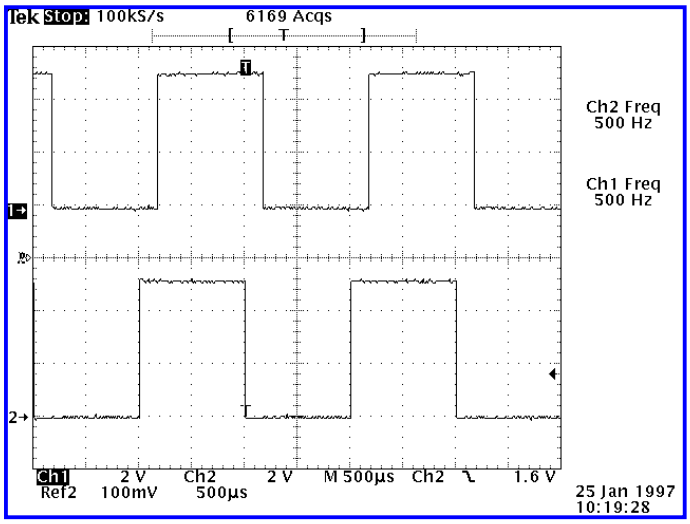


Figure 38-2: Skewed outputs of the 74HC174

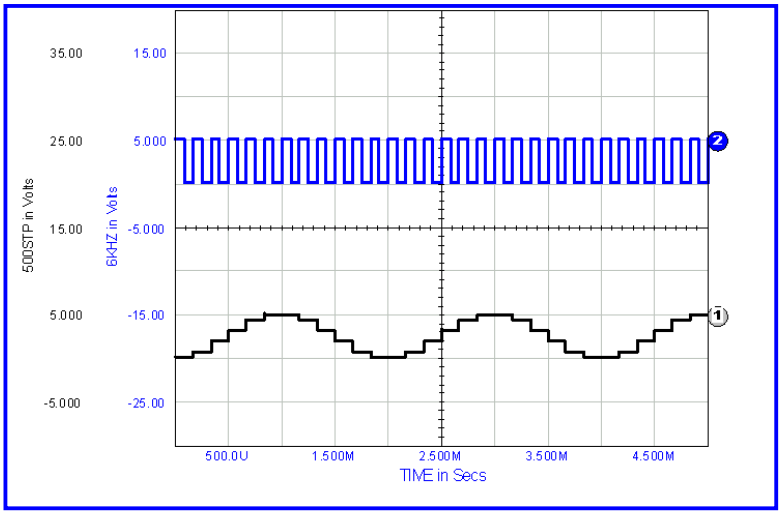


Figure 38-3: IsSpice result of Quasi-resonant 500 Hz output.

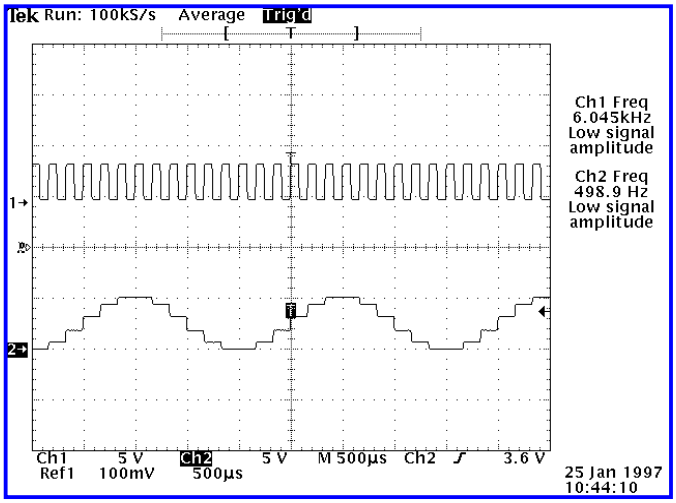


Figure 38-4: 6 Khz input square wave (top) and Quasi-resonant 500 Hz output of 74HC174 (bottom)

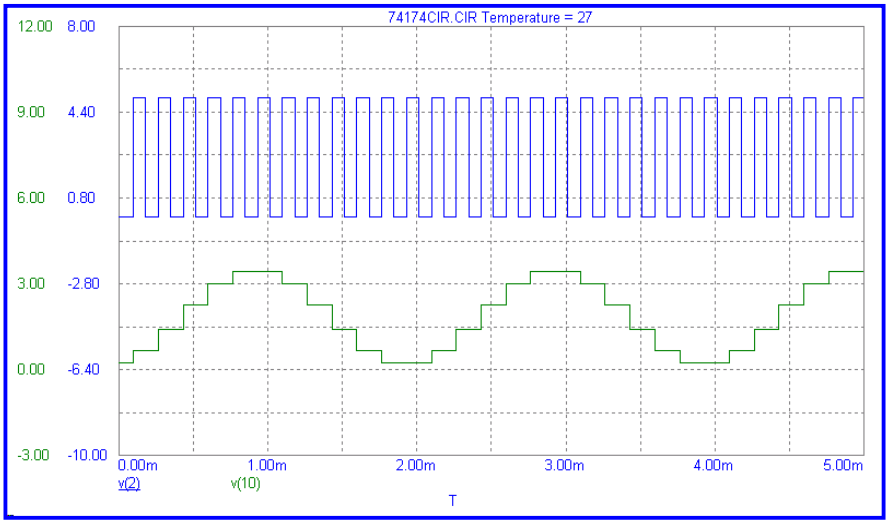


Figure 38-5: Micro-Cap result of Quasi-resonant 500 Hz output

The effects of the circuit in the frequency domain were also characterized. The Fourier transform of the quasi-square waveform in Figure 38-4 was taken, and the results shown in Figure 38-5. Note the 3rd, 5th, 7th , and 9th harmonics are suppressed by about 40db, while the 11th and 13th harmonics are about 20db less. The IsSpice simulation of this circuit was generated using the ICL feature of IsSpice. The format of the FOURIER command are shown below in Table 38-1. The resulting circuit characteristics in the frequency domain (Figure 38-6) compare favorably to the resulting output from the IsSpice file (Table 38-2), which is imported into Excel for graphing (Figure 38-7).

IsSpice: In the Edit Controls box of the schematic, type the following lines

.FOUR 1.2K V(10)

Pspice: In the Analysis menu, select Setup. Click the Transient button and check the Enable Fourier box. Then enter the center frequency, number of harmonics, and output varaibles.

Micro-Cap: In the Analysis menu, select Transient Anlaysis. In the box for Y expression, enter the following:

HARM (V(x))

where x is the node of interest.

Table 38-1: FOURIER command syntax for IsSpice Pspce, and MicroCap

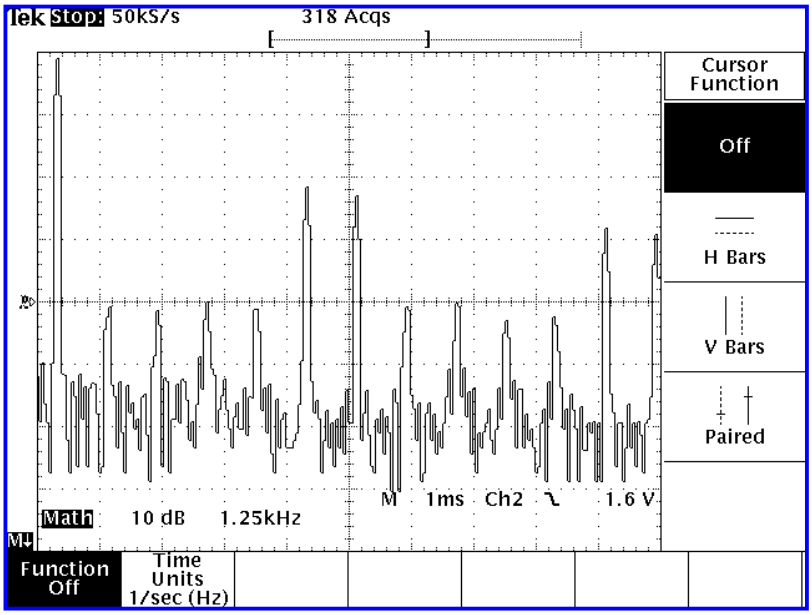


Figure 38-6: Fourier transform of 500 Hz output of 74HC174

Fourier analysis for v(18):

No. Harmonics: 25, THD: 0.48878 %, Gridsize: 200, Interpolation Degree: 1

Harmonic Frequency Magnitude Phase Norm. Mag Norm. Phase

-------- --------- --------- -- --------- -----------

0 0.000 122655 0 0 0

1 500 1.24307 96.3886 1 0

2 1000 0.00319095 -168.46 0.00256699 -264.85

3 1500 0.00166368 -172.57 0.00133837 -268.96

4 2000 0.00128604 -172.55 0.00103457 -268.94

5 2500 0.00109791 -171.91 0.000883227 -268.3

6 3000 0.000827279 -172.44 0.000665513 -268.83

7 3500 0.000628331 -169.82 0.000505467 -266.21

8 4000 0.00061474 -170.92 0.000494533 -267.3

9 4500 0.000631205 -171.98 0.000507779 -268.37

10 5000 0.000489693 -169.96 0.000393939 -266.35

11 5500 0.0036889 -176.92 0.00296757 -273.31

12 6000 0.000405014 -167.58 0.000325818 -263.96

13 6500 0.00192657 -0.25543 0.00154985 -96.644

14 7000 0.000349058 -166.88 0.000280803 -263.27

15 7500 0.000234937 -162.68 0.000188998 -259.07

16 8000 0.00030614 -164.37 0.000246278 -260.76

17 8500 0.000372014 -165.56 0.00029927 -261.95

18 9000 0.000271725 -163.62 0.000218591 -260.01

19 9500 0.000184528 -148.74 0.000148445 -245.13

20 10000 0.000247479 -160.65 0.000199087 -257.04

21 10500 0.000309538 -169.24 0.000249011 -265.63

22 11000 0.000223398 -160.26 0.000179715 -256.65

23 11500 0.000872786 -173.63 0.000702121 -270.02

24 12000 0.000205702 -157.21 0.000165479 -253.6

Table 38-2: FOURIER command results from IsSpice simulator

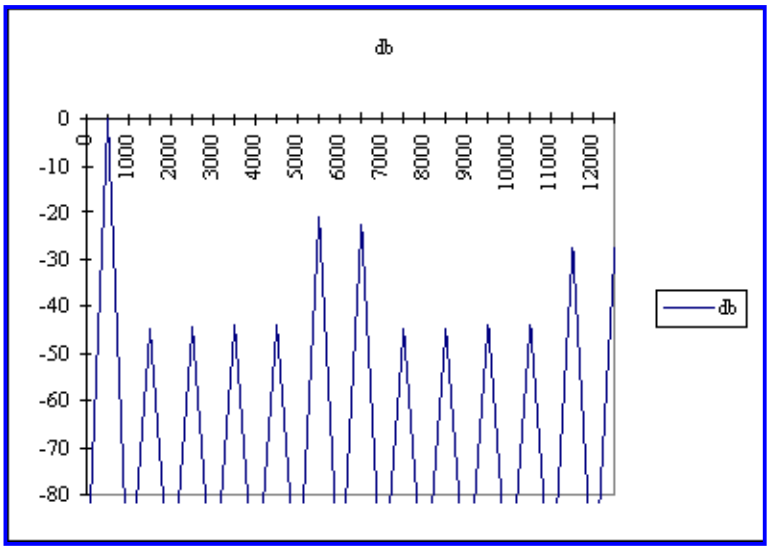


Figure 38-7: IsSpice results of Quasi-resonant 500 Hz output

- Circuit tip: If you are attempting to breadboard this circuit, you may need bypass capacitors (0.1 uF capacitors from Vdd to the local IC ground) in order to minimize jitter and noise effects. These IC's switch at a very fast rate, and can easily cause switching noise to appear on the outputs.

- IsSpice and Pspice tip: To import the data resulting from the FOURIER command (as shown in Table 38-2) into a spread sheet such as Excel, first, open the .out file. Highlight and copy the data you need in the .out file and open Excel. After Excel opens, paste the contents into the spreadsheet. The next step should be to pull down the DATA menu and select the TEXT TO COLUMNS command. Follow the steps to convert the pasted data into space delimited data. After this is completed, you should have columns for each of the data headings used by IsSpice to write the results of the FOURIER command. You may now use Excel's graphing features to view your data. This procedure works for normal output data as well. If you ever wish to extract data from an output simulation to Excel, follow these steps. Excel performs a dizzying array of mathematical operations that can be exploited by engineers.

This circuit is now ready to be connected to a band pass filter, shown in Figure 38-8.

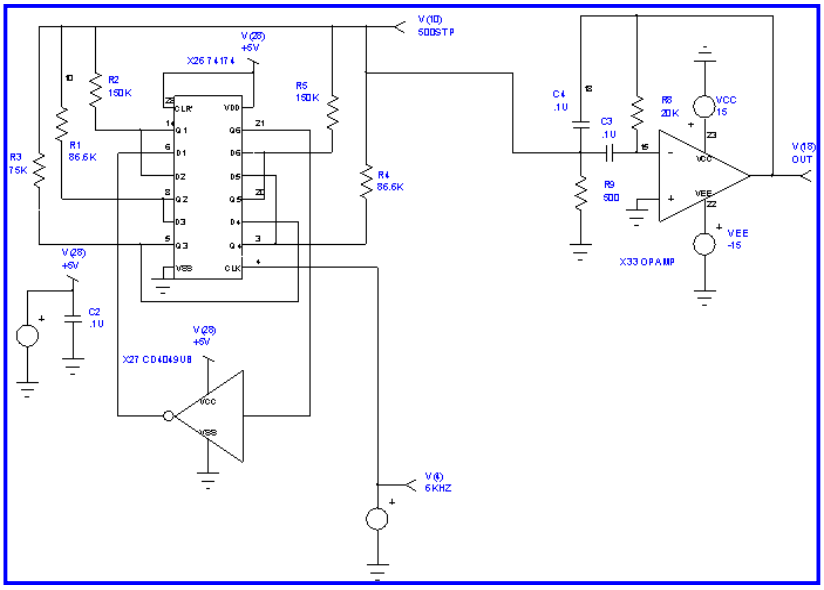


Figure 38-8: Schematic of multi-phase square wave generator connected to band pass filter

The resulting output of the breadboard is shown in Figure 38-9. The output of the Spice simulations are shown in Figure 38-10A and Figure 38-10B. The output of the circuit is a clean, low distortion 500 Hz sine wave.

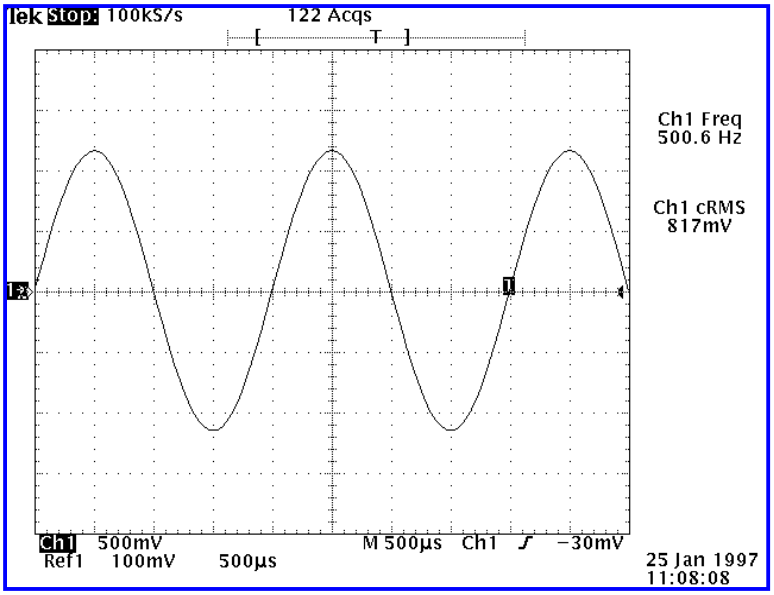


Figure 38-9: End result, 500 Hz Sine wave

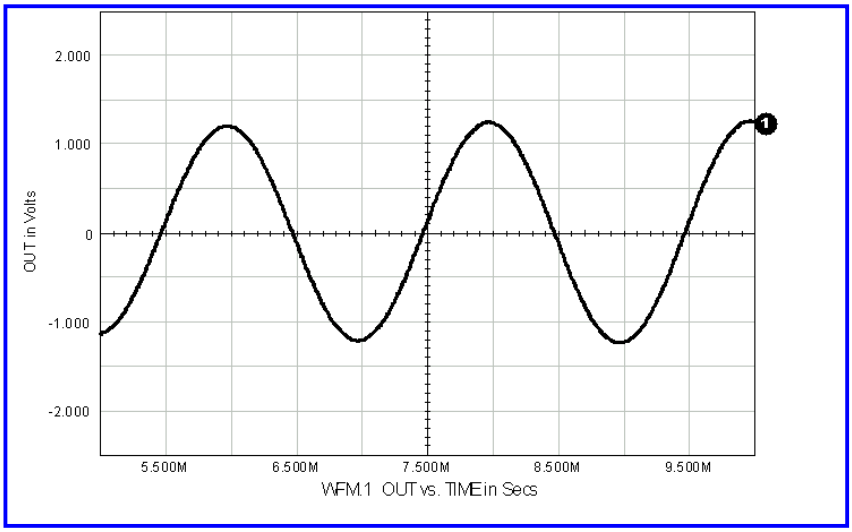


Figure 38-10A: IsSpice result of 500 Hz sine wave

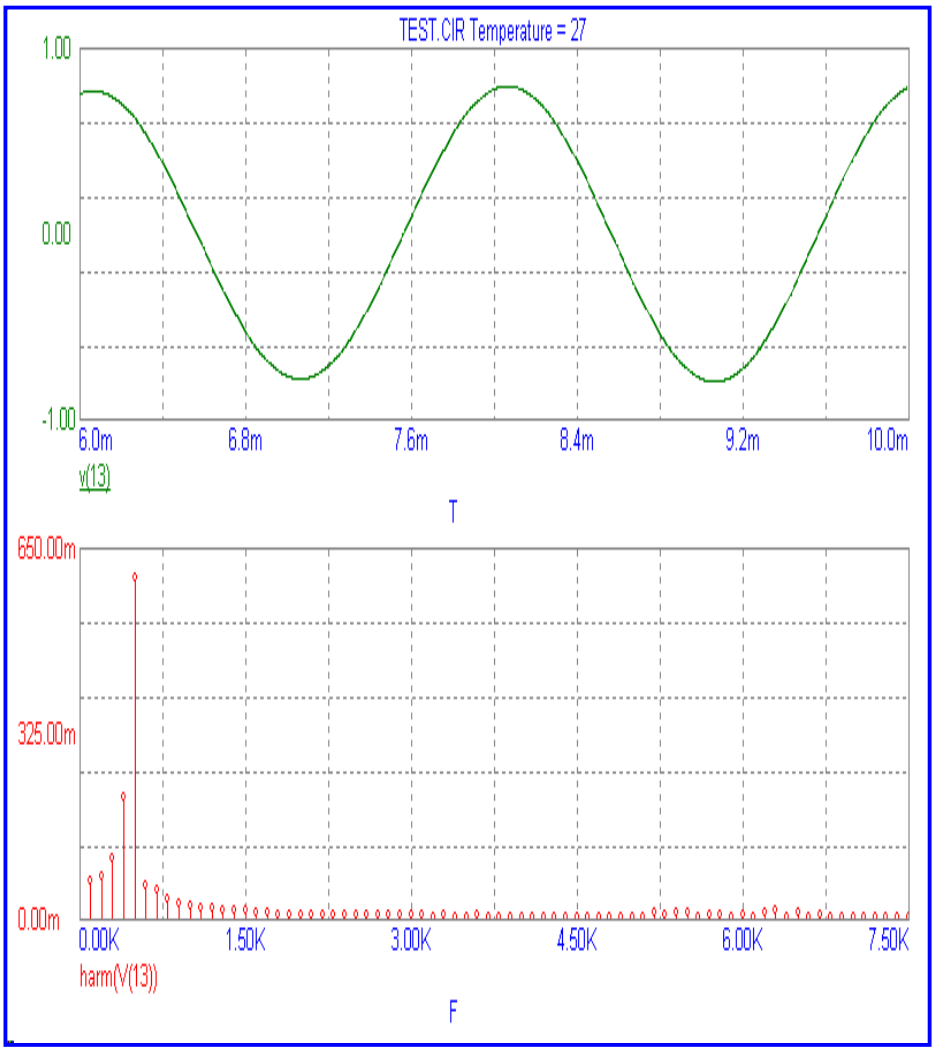


Figure 38-10B: Microcap result of 500 Hz sine wave

Examining the Frequency components of this output, our breadboard results are shown in Figure 38-11, while the Spice results are shown in Figure 38-12A and Figure 38-12B.

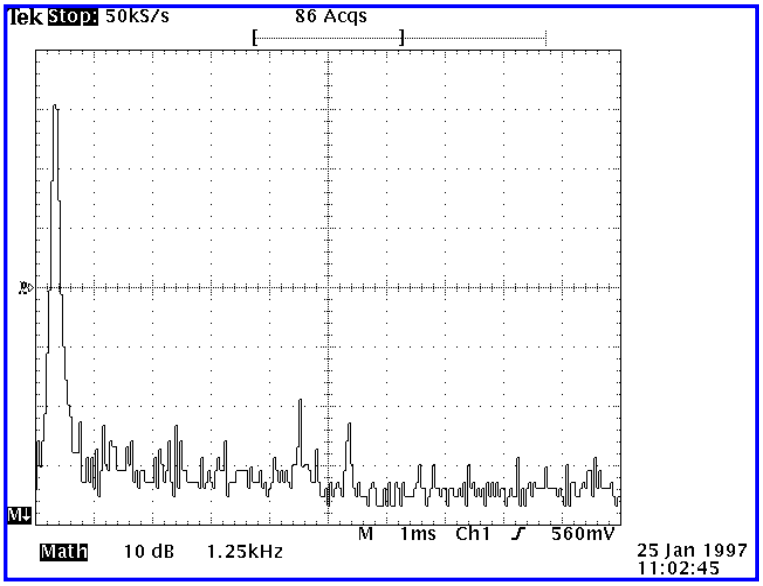


Figure 38-11: Fourier results of 500 Hz Sine wave after Band pass filter

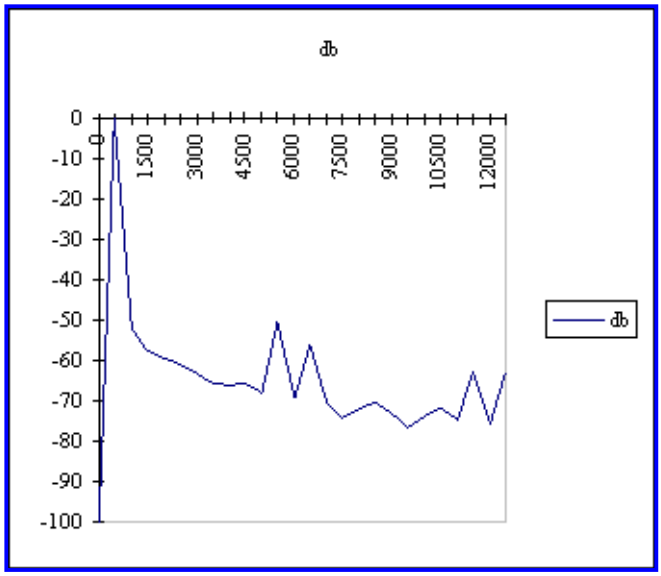


Figure 38-12A: IsSpice results of 500 Hz sine wave

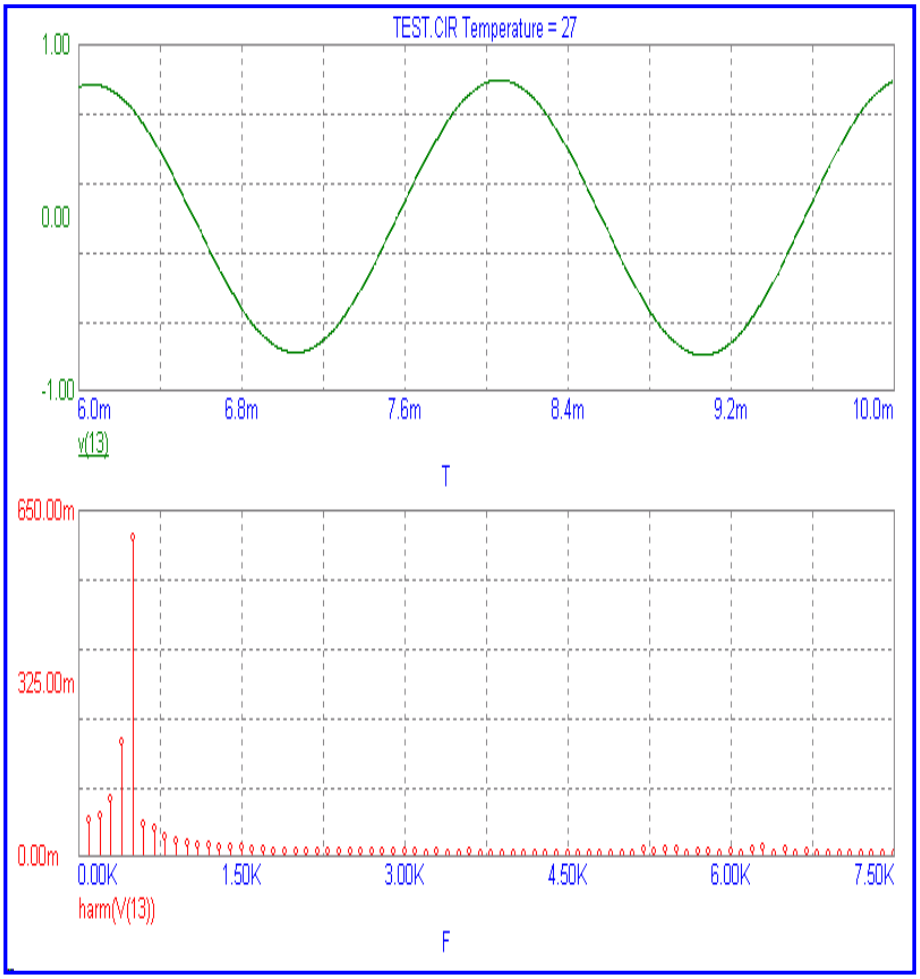
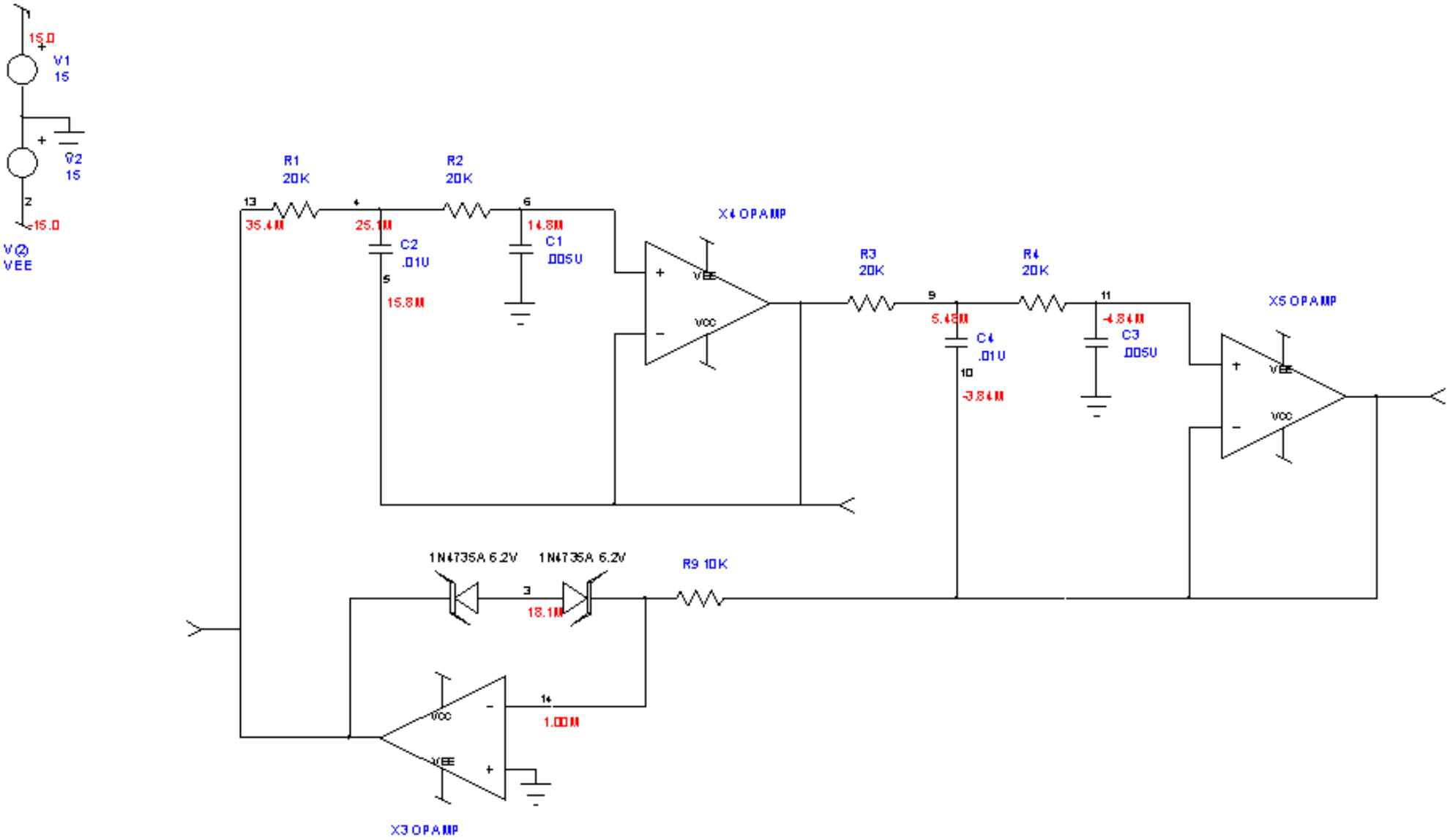
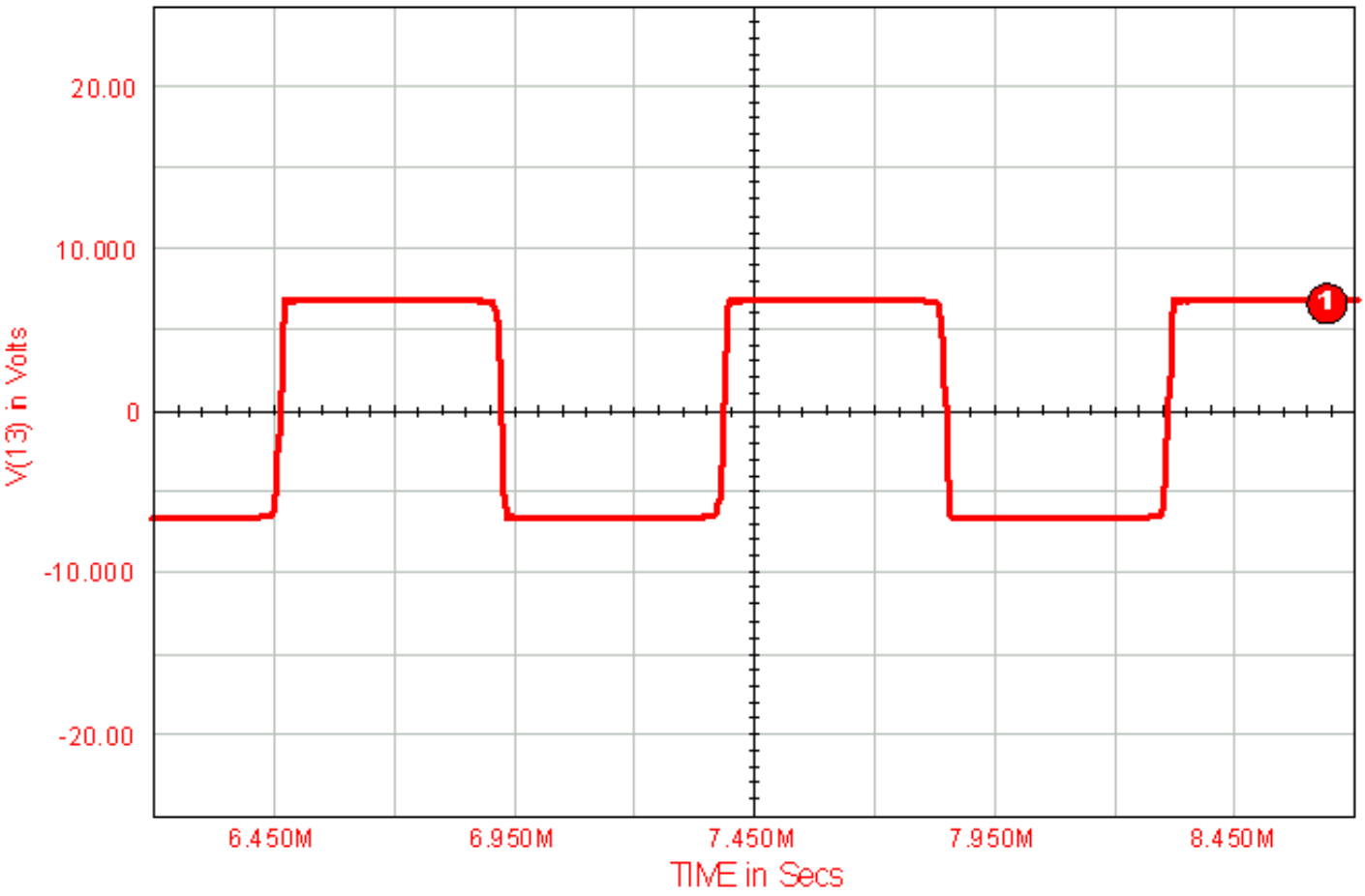


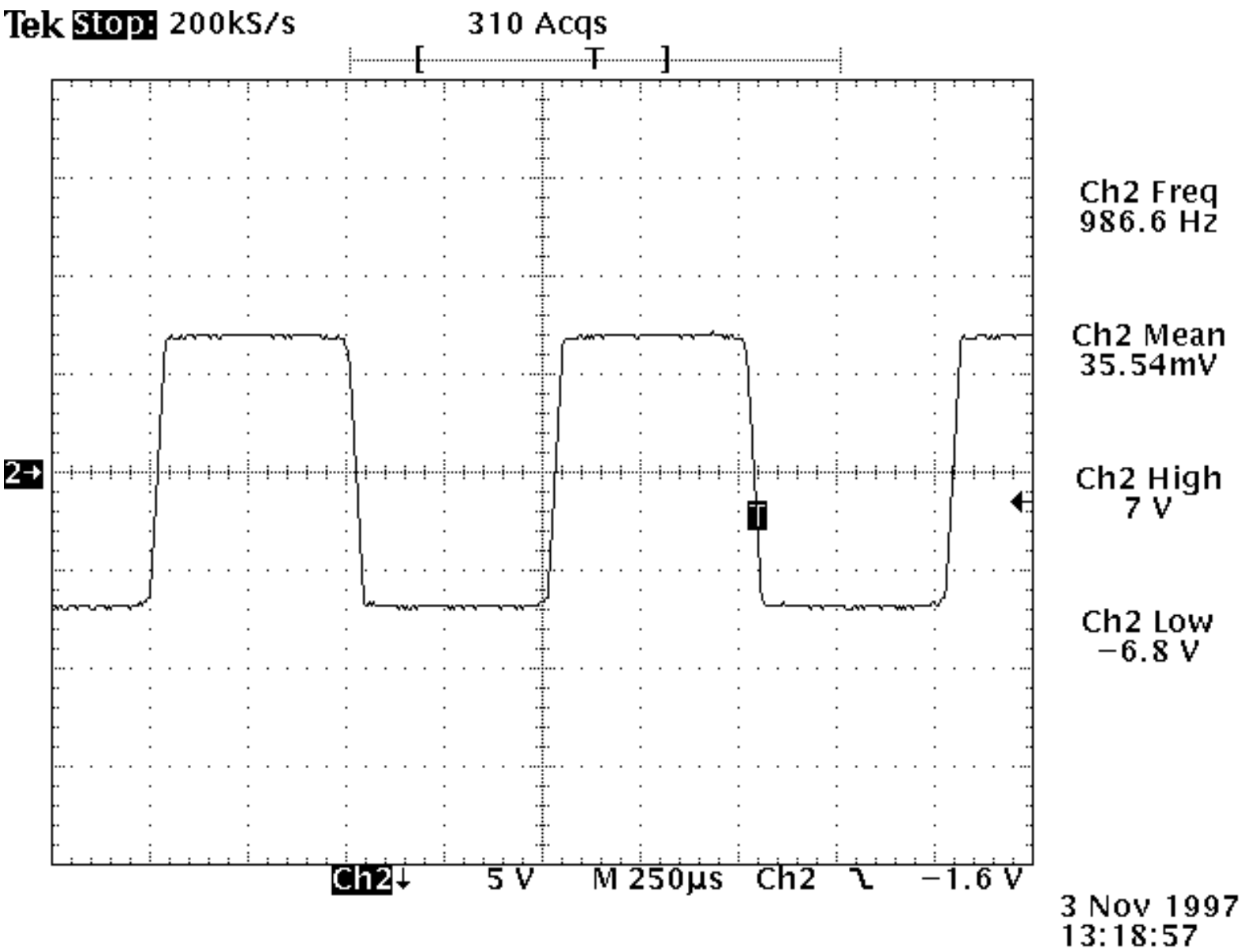
Figure 38-12B: Microcap results of 500 Hz sine wave

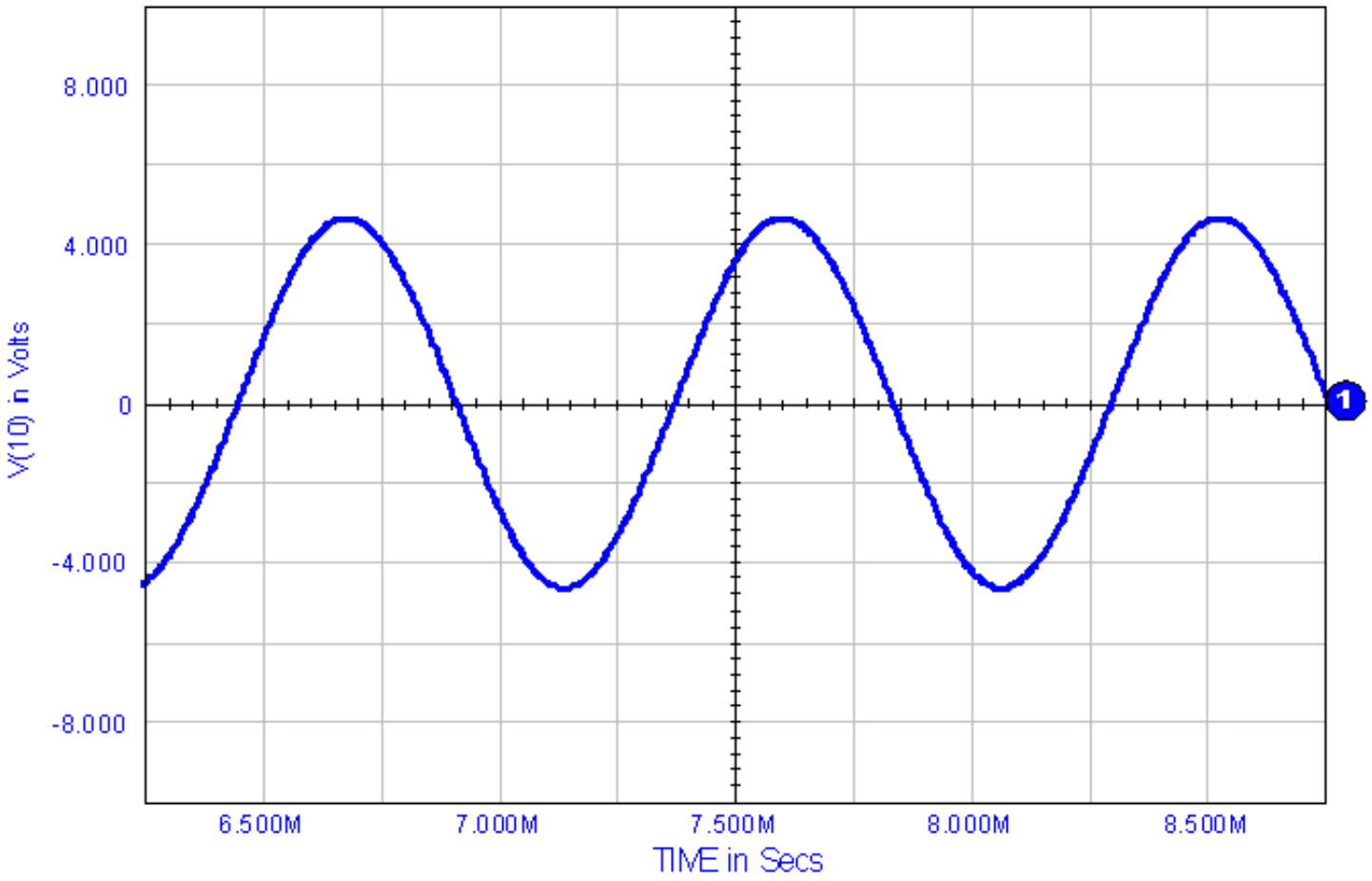
Run Time Summary		
IsSpice v 7.6	PsPice v 6.3	Micro-Cap V v2
151.7 Sec	N/A	172.6 Sec
Advantages: Good long term frequency stability, excellent distortion		
Disadvantages: High parts count, added complexity		

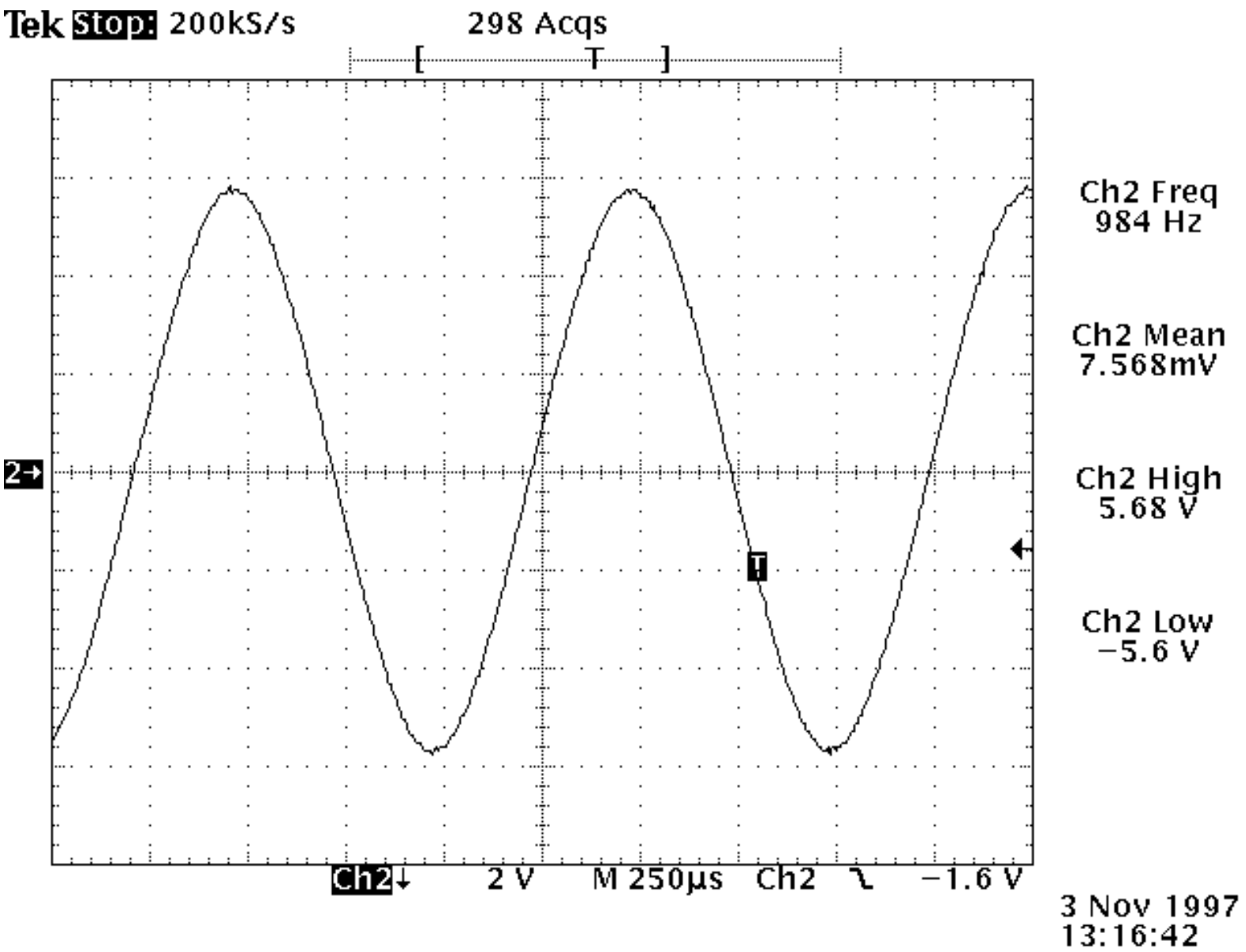
Filenames: sine (IsSpice) sine_mc (Mirco-cap)

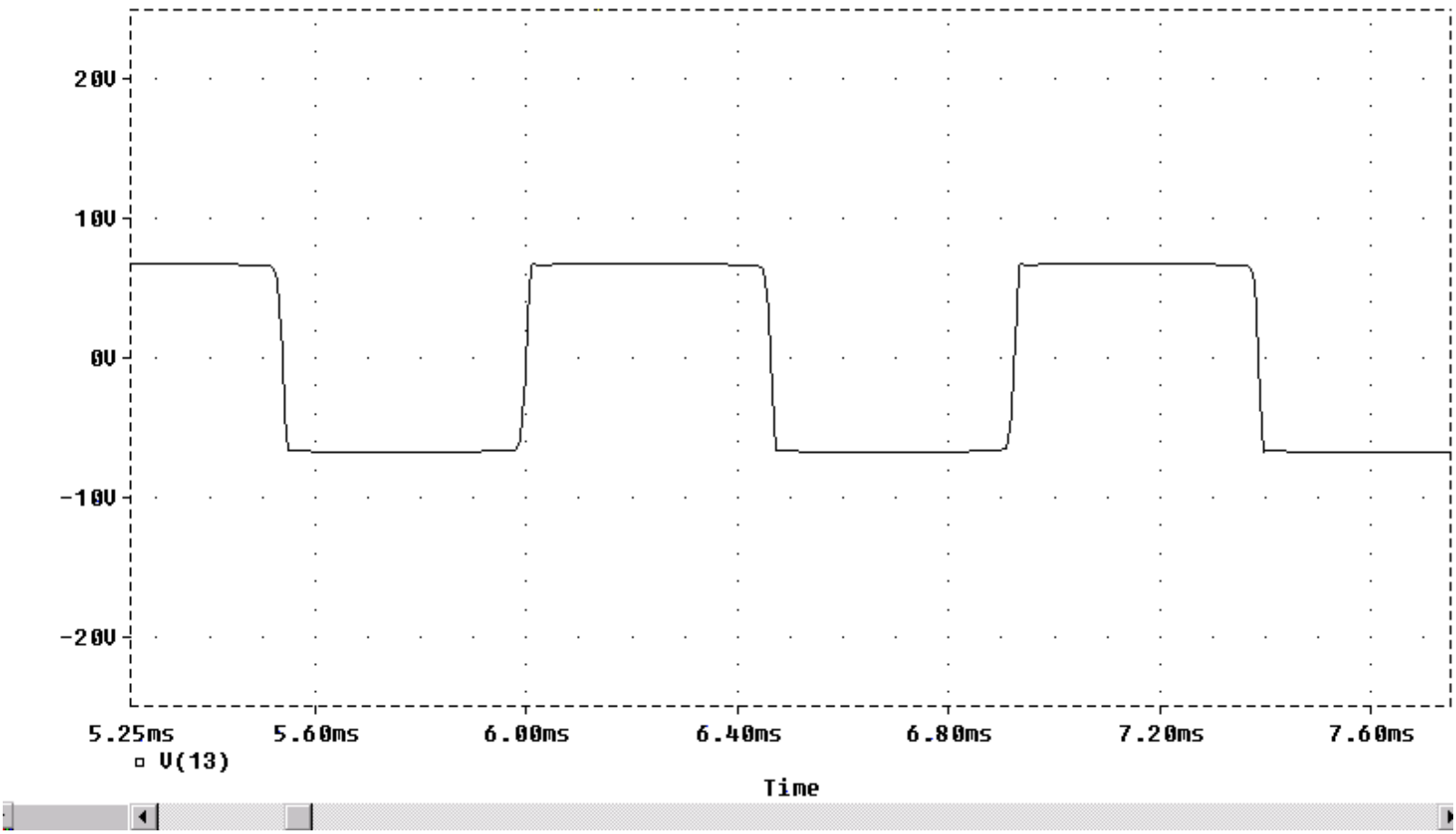

1
15.0
V1
15
2
15.0
V2
VEE
R1
20K
R2
20K
13
35.4M
4
25.1M
6
14.8M
C2
.01U
5
15.8M
C1
.005U
X4 OPAMP
VEE
VCC
R3
20K
R4
20K
9
5.48M
11
-4.84M
C4
.01U
10
-3.84M
C3
.005U
X5 OPAMP
VEE
VCC
1N4735A 6.2V
1N4735A 6.2V
3
18.1M
R9 10K
14
1.00M
VCC
VEE
X3 OPAMP

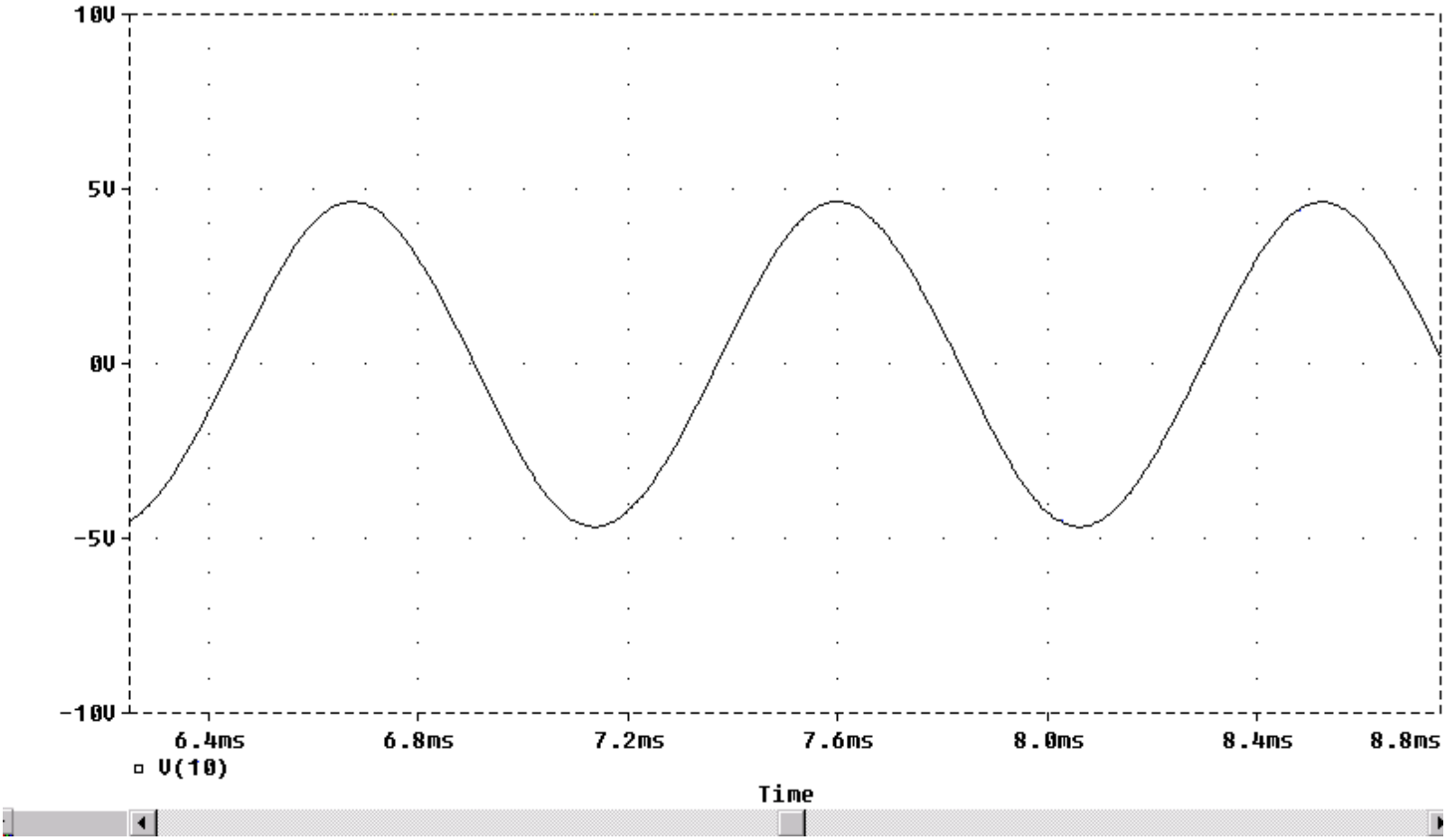

20.00
10.000
0
-10.000
-20.00
V(13) in Volts
6.450M
6.950M
7.450M
7.950M
8.450M
TIME in Secs
1

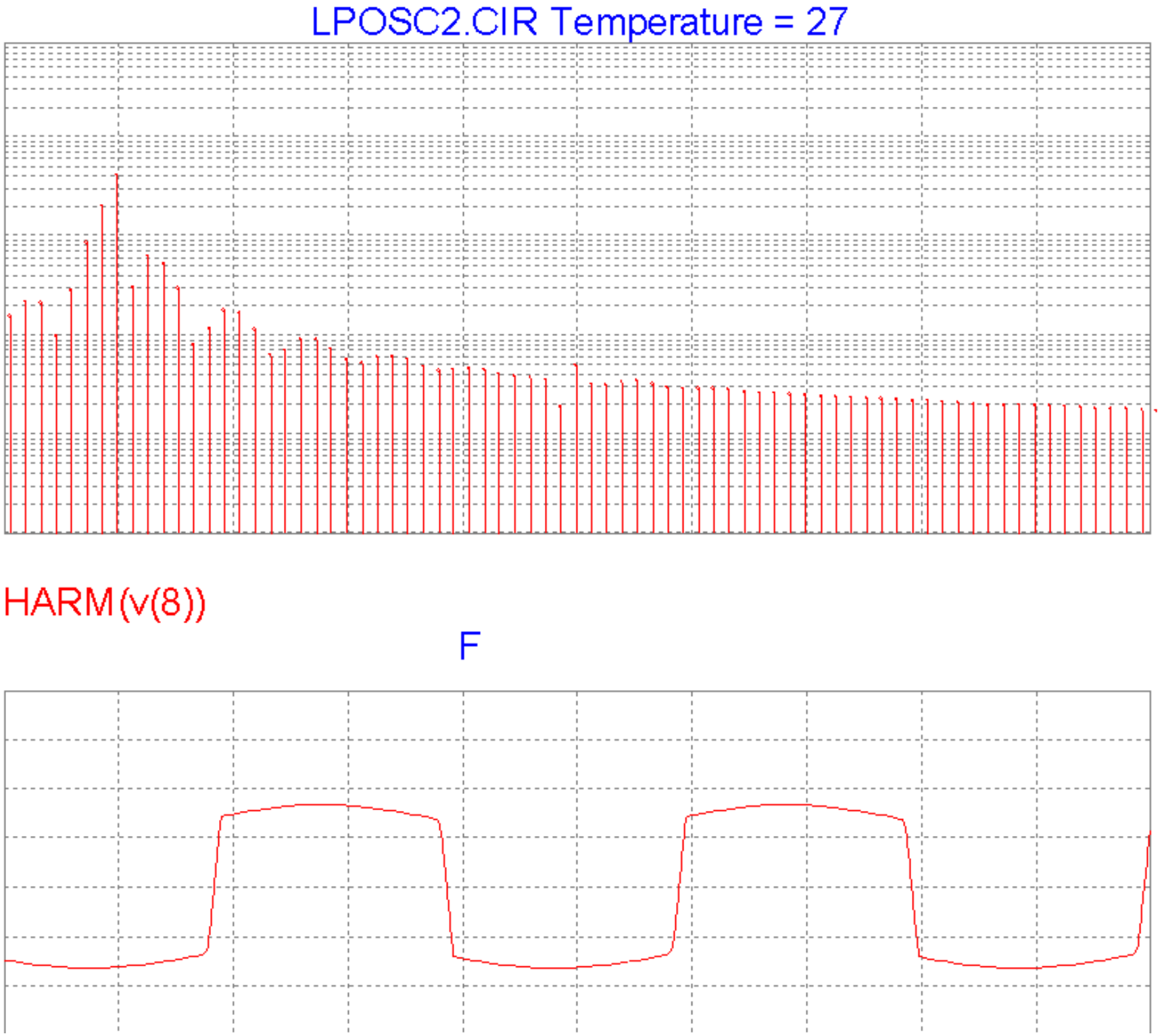

Tek Stop: 200kS/s
310 Acqs
Ch2 Freq
986.6 Hz
Ch2 Mean
35.54mV
Ch2 High
7 V
Ch2 Low
−6.8 V
Ch2↓ 5 V M 250µs Ch2 ⌊ −1.6 V
3 Nov 1997
13:18:57

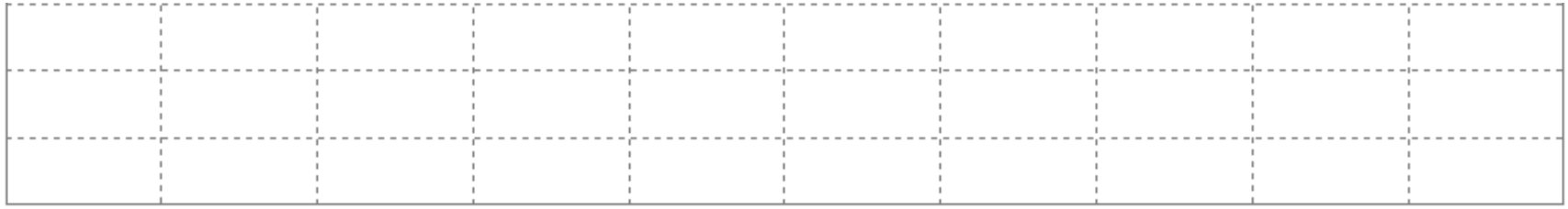

8.000
4.000
0
-4.000
-8.000
V(10) in Volts
6.500M
7.000M
7.500M
8.000M
8.500M
TIME in Secs
1


Tek Stop: 200kS/s
298 Acqs
Ch2 Freq
984 Hz
Ch2 Mean
7.568mV
Ch2 High
5.68 V
Ch2 Low
−5.6 V
Ch2↓ 2 V M 250µs Ch2 ⌊ −1.6 V
3 Nov 1997
13:16:42


20V
10V
0V
-10V
-20V
5.25ms
5.60ms
6.00ms
6.40ms
6.80ms
7.20ms
7.60ms
V(13)
Time

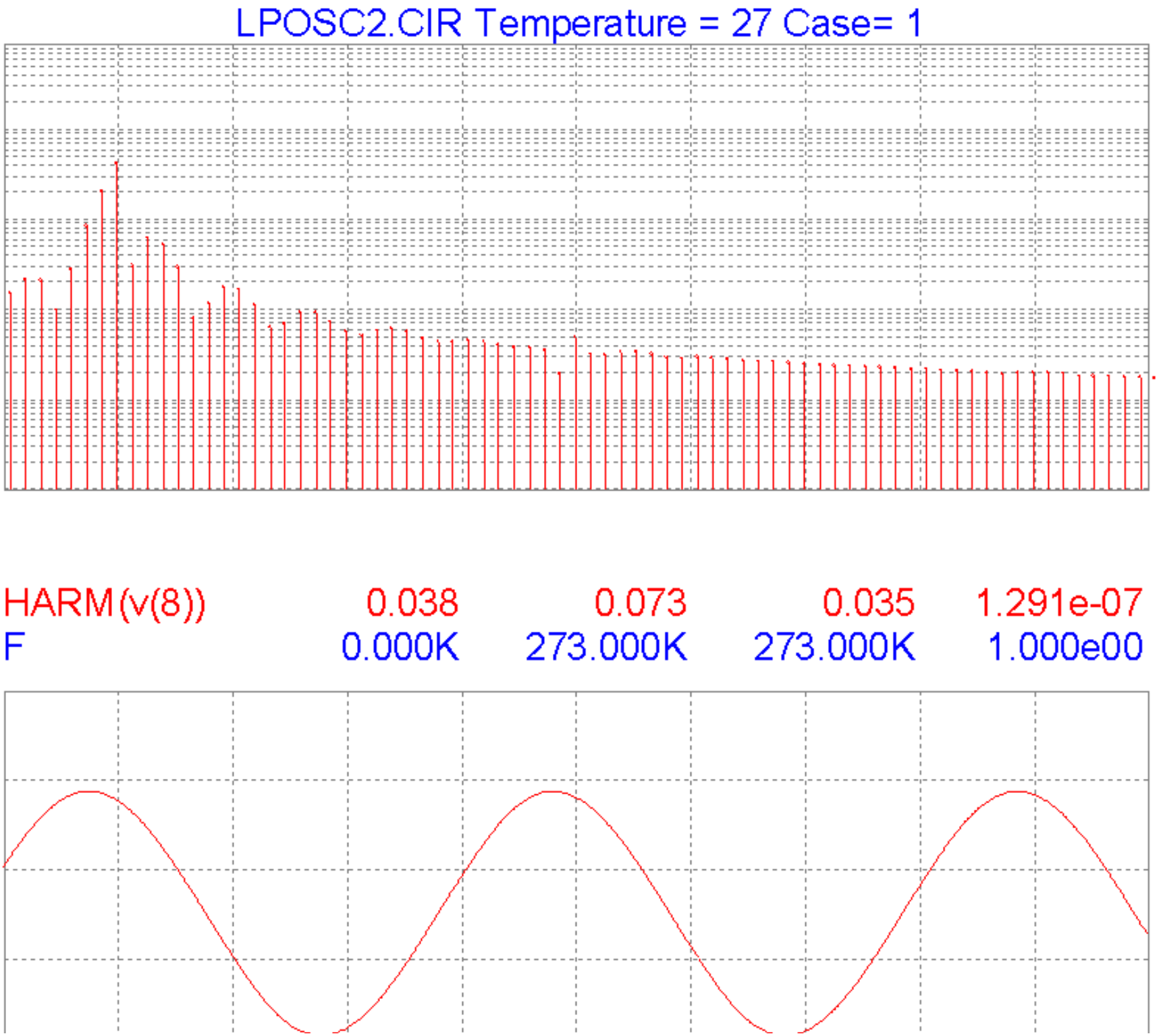

10V
5V
0V
-5V
-10V
6.4ms
6.8ms
7.2ms
7.6ms
8.0ms
8.4ms
8.8ms
V(10)
Time

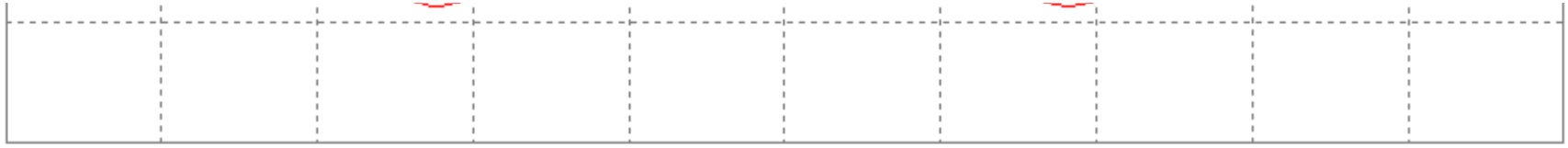

LPOSC2.CIR Temperature = 27
HARM(v(8))
F



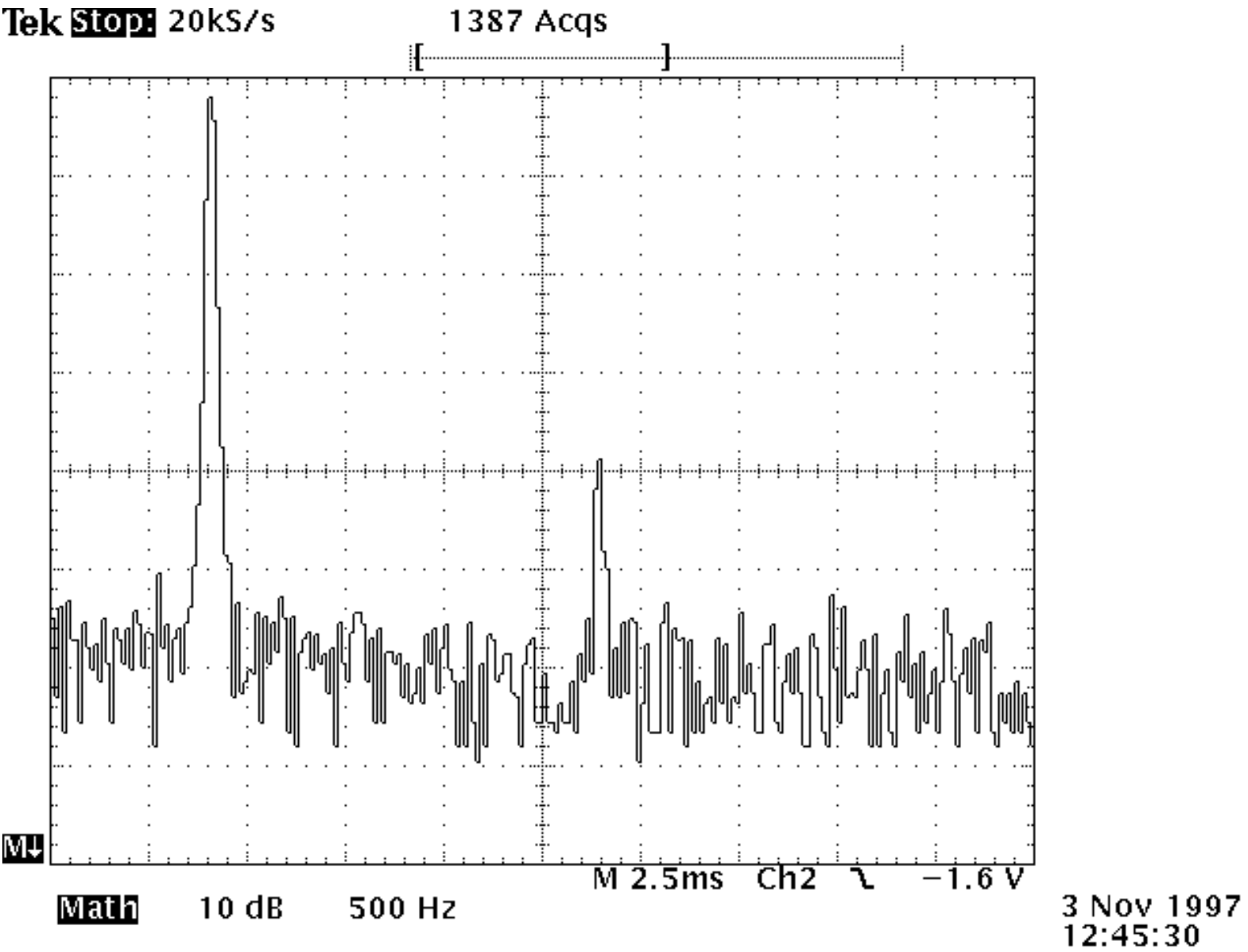
V(6)

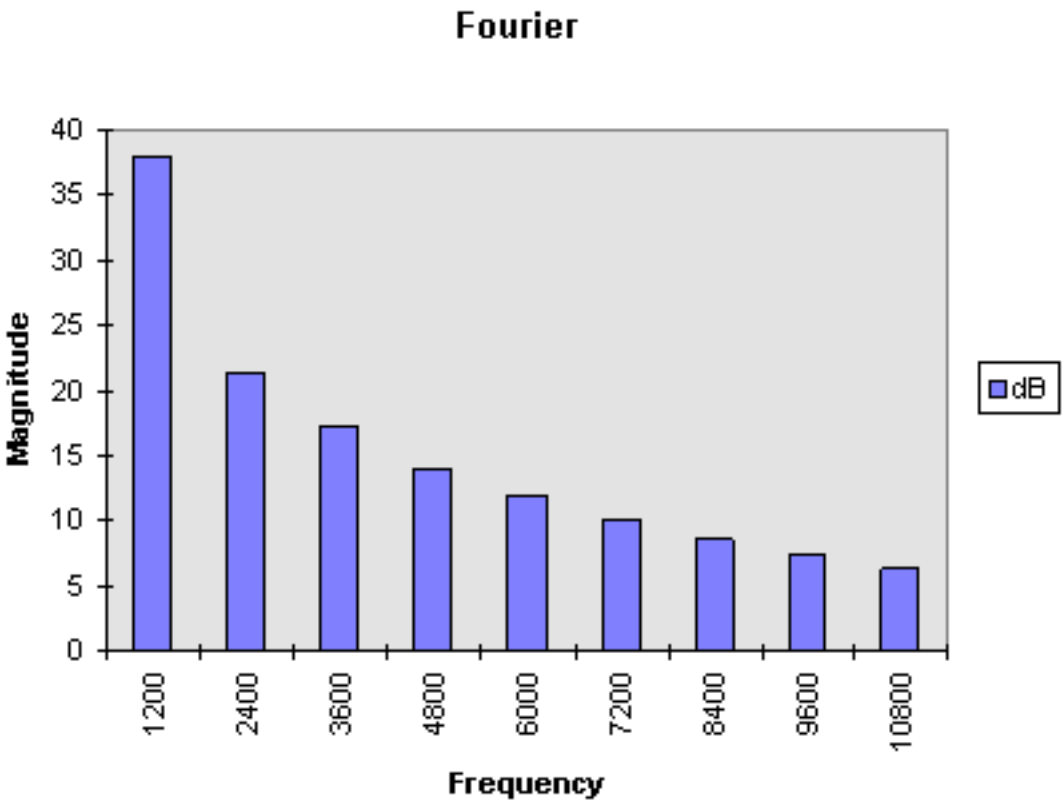
F

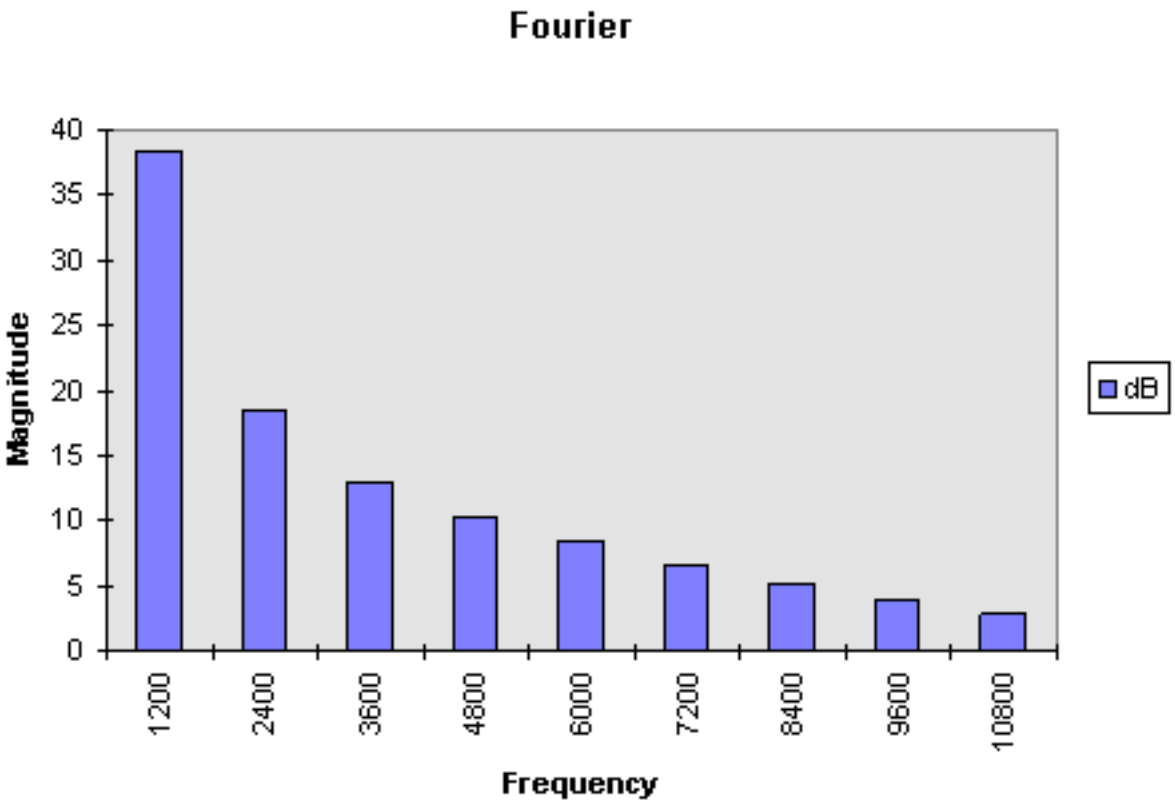

LPOSC2.CIR Temperature = 27 Case= 1
HARM(v(8)) 0.038 0.073 0.035 1.291e-07
F 0.000K 273.000K 273.000K 1.000e00

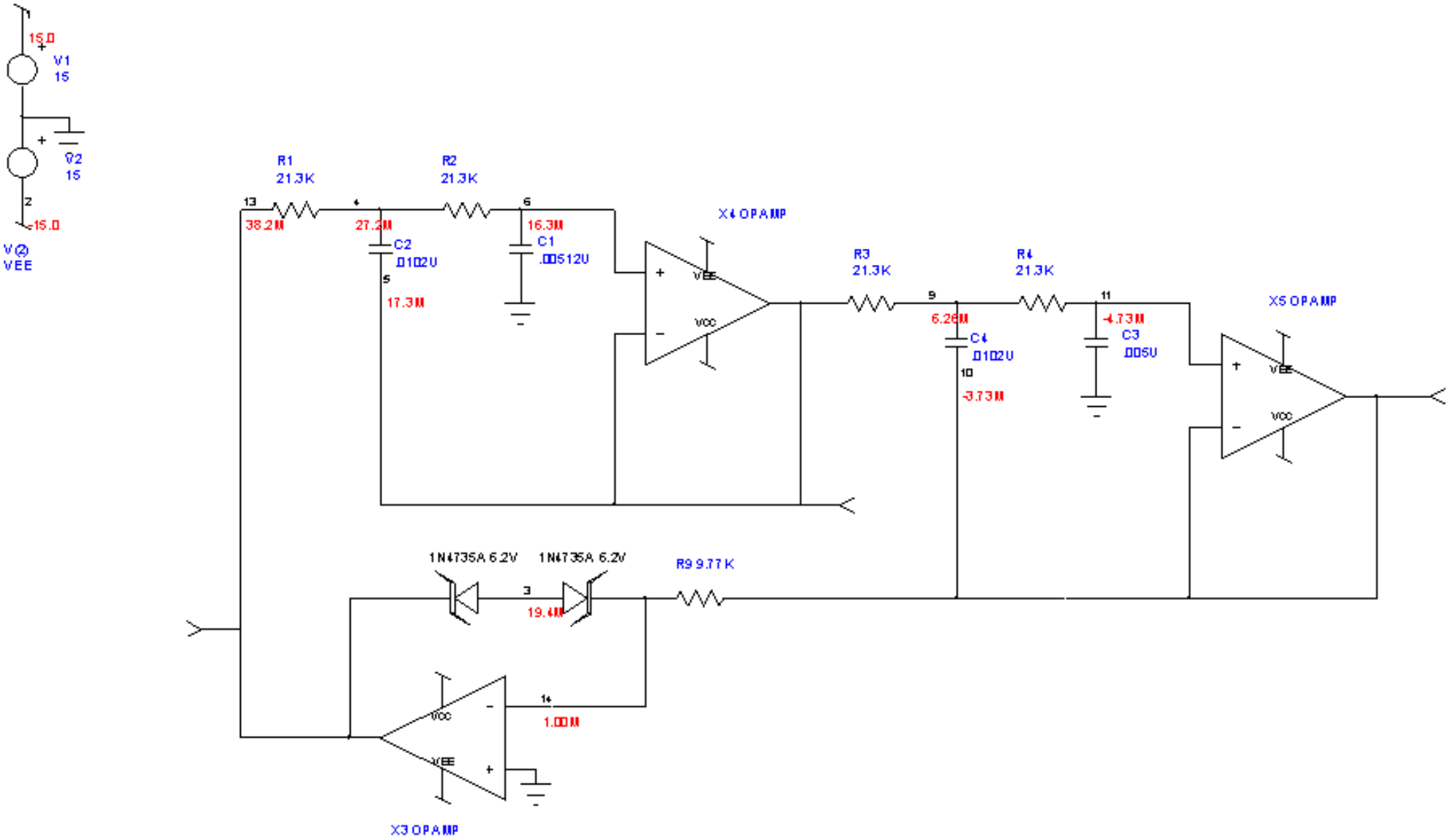


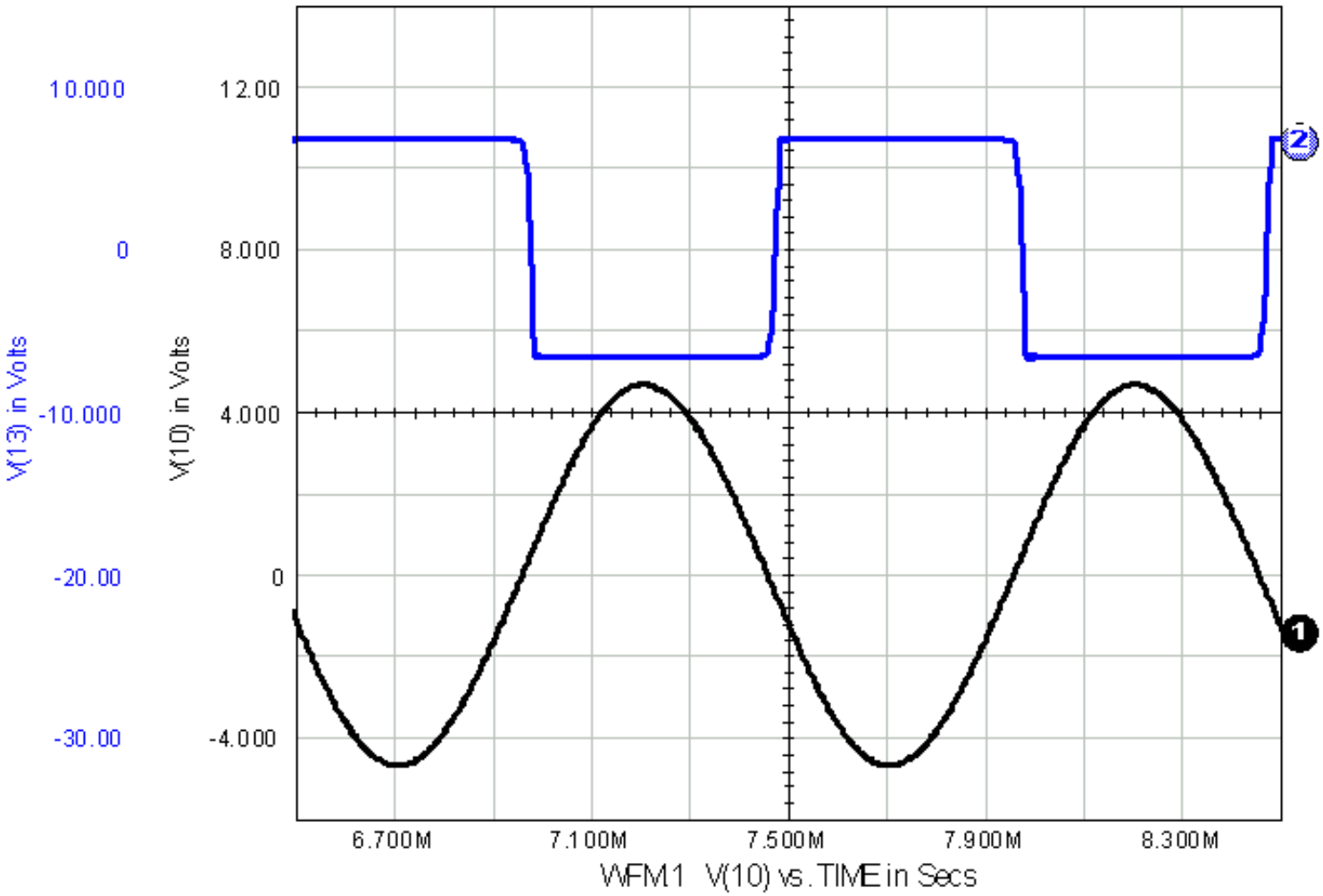
V(8)	0.002	-4.208	-4.210	-2.823e02
F	0.084m	14.996m	14.912m	1.000e00


Tek Stop: 20kS/s
1387 Acqs
M↓
M 2.5ms Ch2 ∖ −1.6 V
Math 10 dB 500 Hz
3 Nov 1997
12:45:30


Fourier
Magnitude
40
35
30
25
20
15
10
5
0
1200
2400
3600
4800
6000
7200
8400
9600
10800
Frequency
dB


Fourier
Magnitude
40
35
30
25
20
15
10
5
0
1200
2400
3600
4800
6000
7200
8400
9600
10800
Frequency
dB


1
15.0
V1
15
2
V2
15
-15.0
V(2)
VEE
R1
21.3K
R2
21.3K
13
4
6
38.2M
27.2M
16.3M
C2
.0102U
C1
.00512U
5
17.3M
X4 OPAMP
VEE
VCC
R3
21.3K
R4
21.3K
9
11
6.26M
-4.73M
C4
.0102U
C3
.005U
10
-3.73M
X5 OPAMP
VEE
VCC
1N4735A 6.2V
1N4735A 6.2V
3
19.4M
R9 9.77K
14
1.00M
VCC
VEE
X3 OPAMP


10.000
0
-10.000
-20.00
-30.00
V(13) in Volts
12.00
8.000
4.000
0
-4.000
V(10) in Volts
6.700M
7.100M
7.500M
7.900M
8.300M
WFM1 V(10) vs. TIME in Secs
2
1

#39: Colpitts Oscillator

This circuit uses the resonance of an LC filter to switch an inverter creating a square wave at the output of the inverter. The schematic is shown in Figure 39-1. This arrangement provides better stability then the RC resonating oscillator with an amazingly small parts count. The output is a square wave oscillation with a fixed frequency set by the LC time constant. The switching signal is driven by a sine wave resonance between the inductor and the capacitor.

An important feature of all spice packages is what type of estimation or curve fitting mathematics are available. All three of the packages used in this book default to the trapezoidal method. Microcap and IsSpice offer the gear method as an option. For this case, the gear method is proven to be more accurate in IsSpice. The results of this comparison are shown in Figure 39-1 and Figure 39-2.

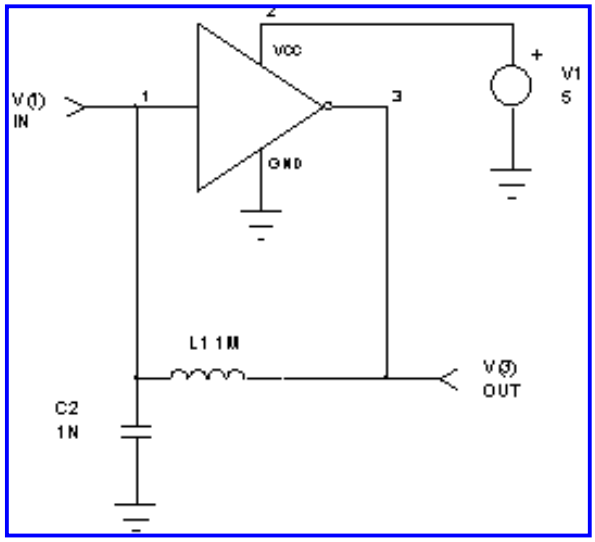


Figure 39-1: Schematic of Colpitts Oscillator

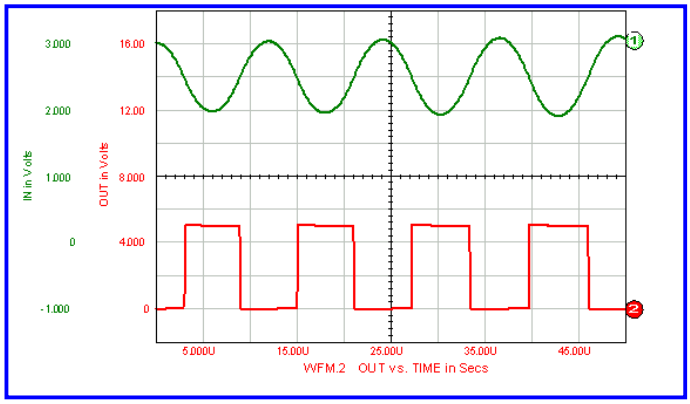


Figure 39-2: IsSpice results of Colpitts Oscillator (Trapezoidal integration)

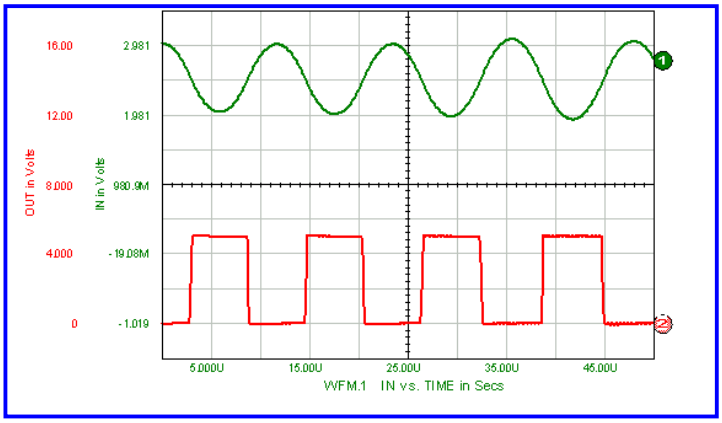


Figure 39-3: IsSpice results of Colpitts Oscillator (Gear integration)

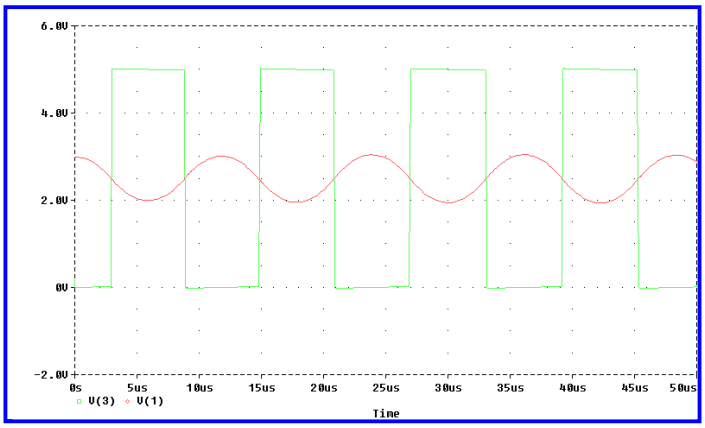


Figure 39-4: Pspice results of Colpitts Oscillator

- Simulation Note: Pspice does not offer the gear method, the model of the 74HC04 was taken from IsSpice because the evaluation version of Pspice does not offer an analog model.

The 74HC04 is commonly used as a digital inverter, when building this model it is important to know if the model you are using is capable of providing analog results. The Microcap model had an error in the interpretation of the parts specification. The 74HC04 model switched high at 30% of Vcc and Low at 70% of Vcc as if the part had hysterics. This decreased the amplitude of the input sine wave and greatly increased the output frequency. This model of the 74HC04 may work well with digital inputs, but is not correct for an analog

response. The results of the Microcap simulation and the lab data are contained in Figure 39-5 and Figure 39-6.

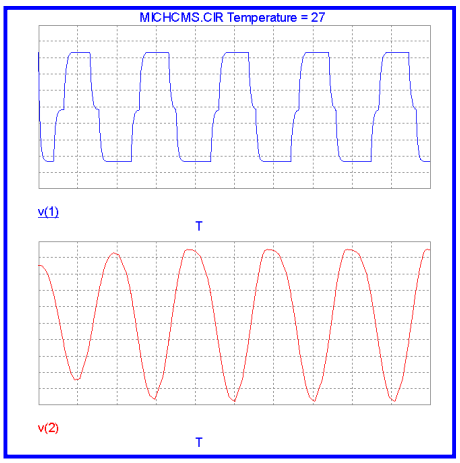


Figure 39-5: Microcap results of Colpitts Oscillator

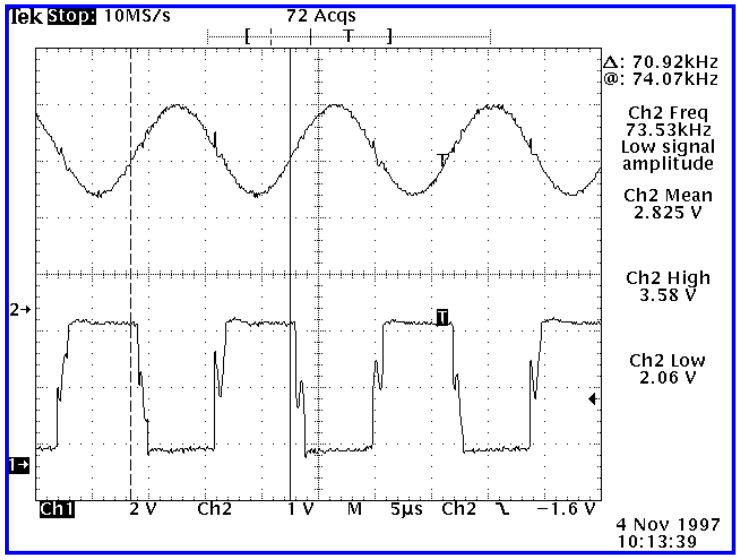


Figure 39-6: Hardware results of Colpitts Oscillator

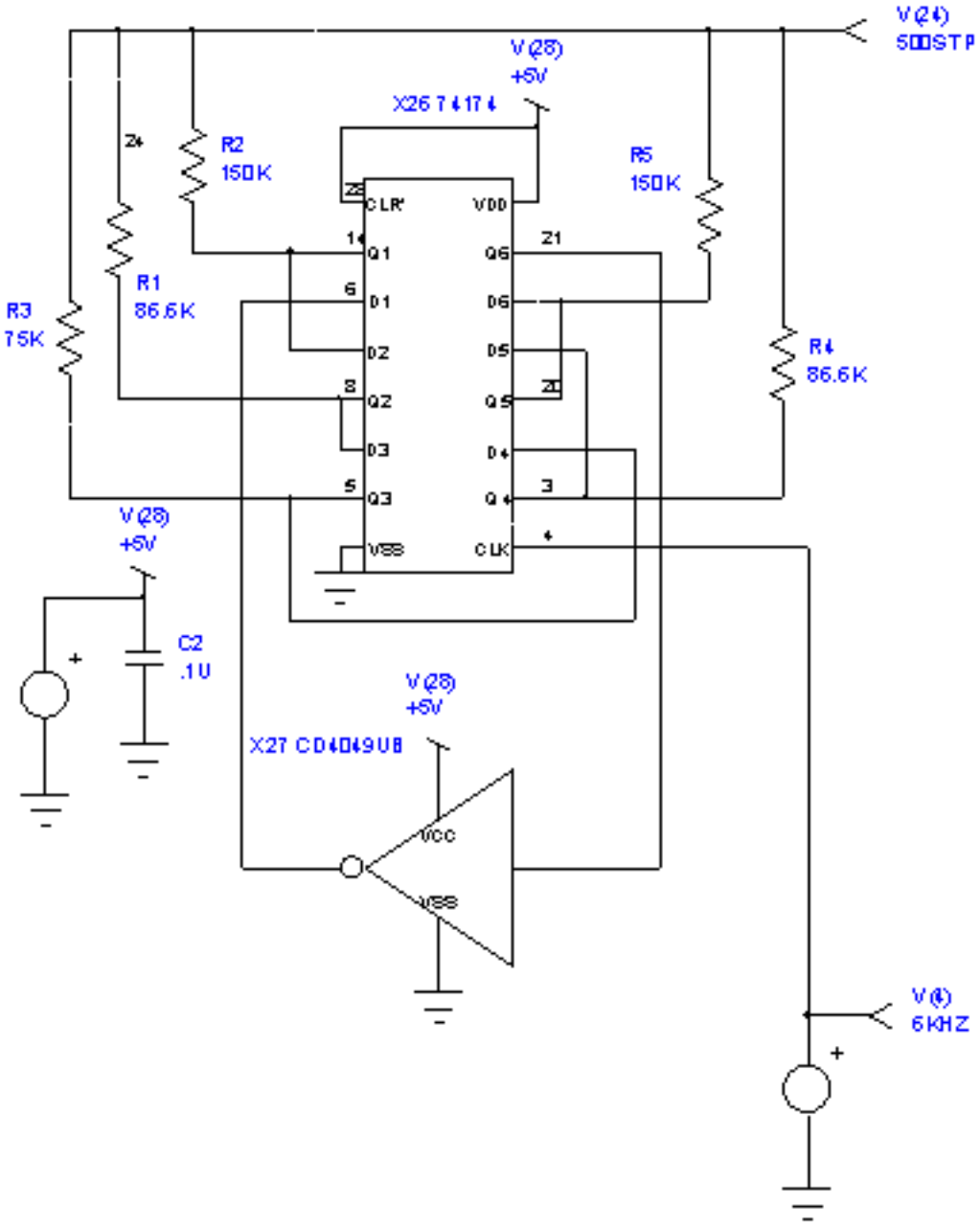
Comparison of Results				
Condition	IsSpice	Pspice	Microcap	Measured
Frequency (kHz)	80.97	82.5	494	73.5
Sine Max (volts)	3.06	3.04	5.58	3.58
Sine Min (volts)	1.9	1.94	-1.815	2.06

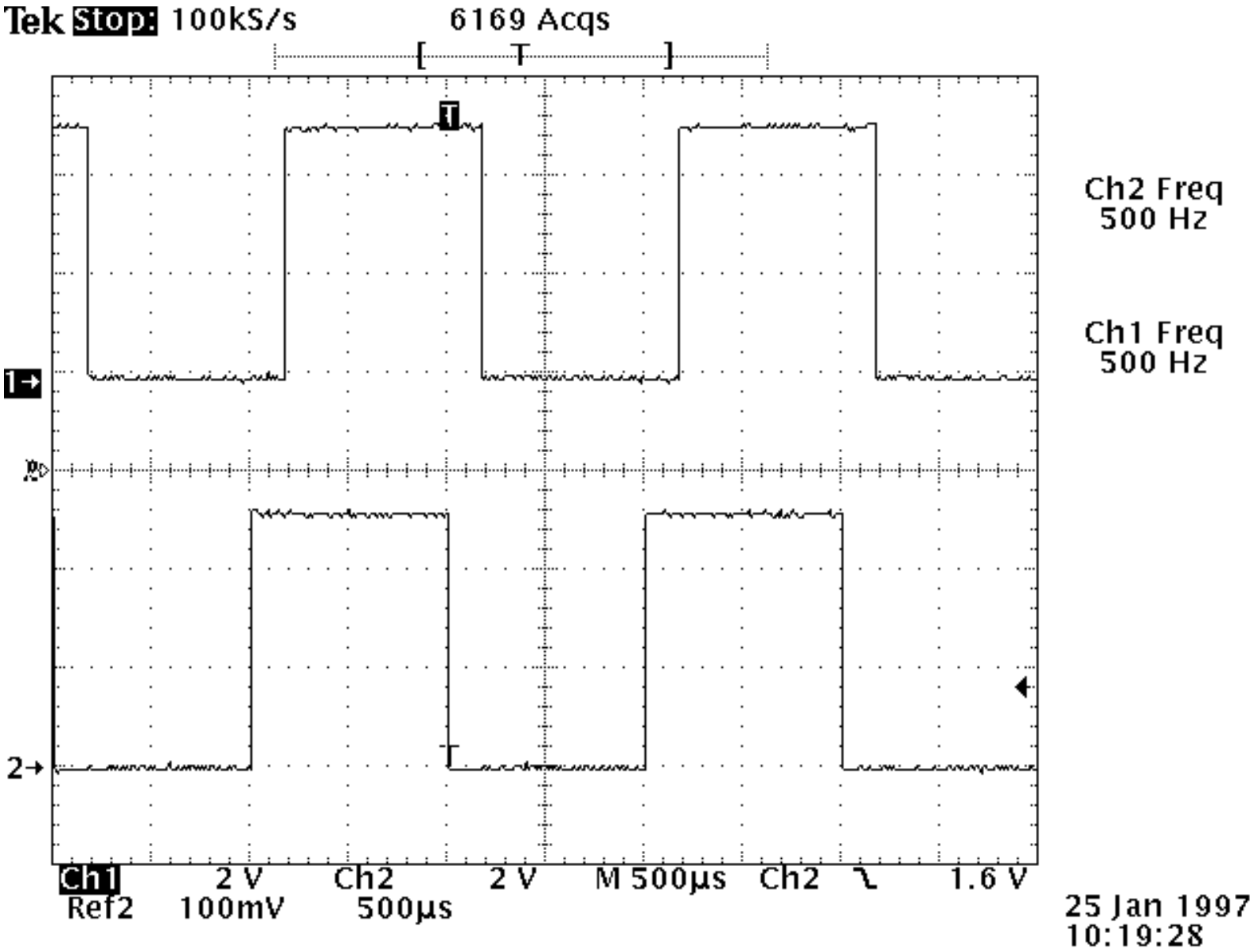
Table 39-1: Comparison between simulators

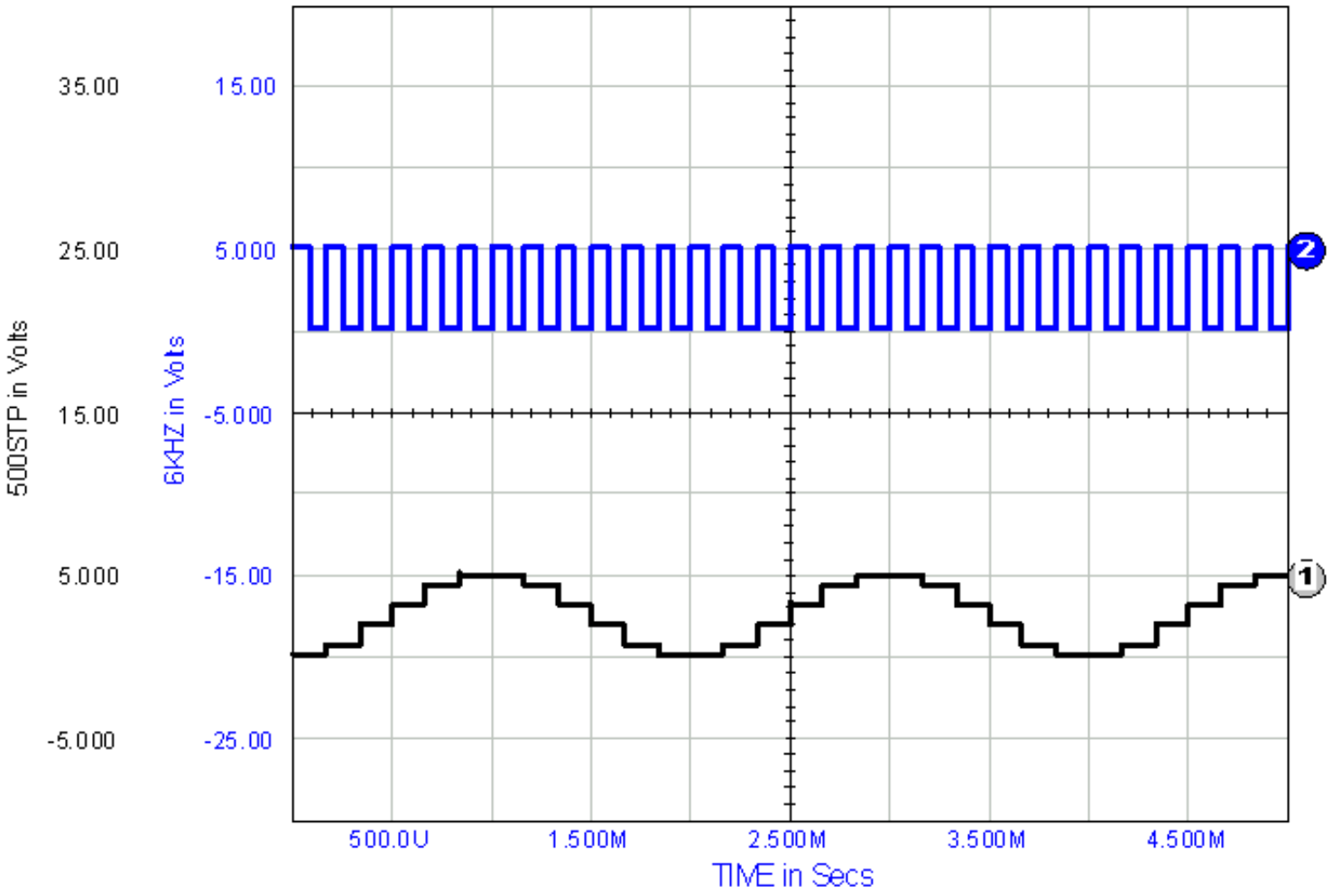
Run Time Summary		
IsSpice v 7.6	PsPice v 6.3	Micro-Cap V v2
1.904 Sec	2.79 Sec	4.032 Sec
Advantages: Low part count, moderate frequency stability		

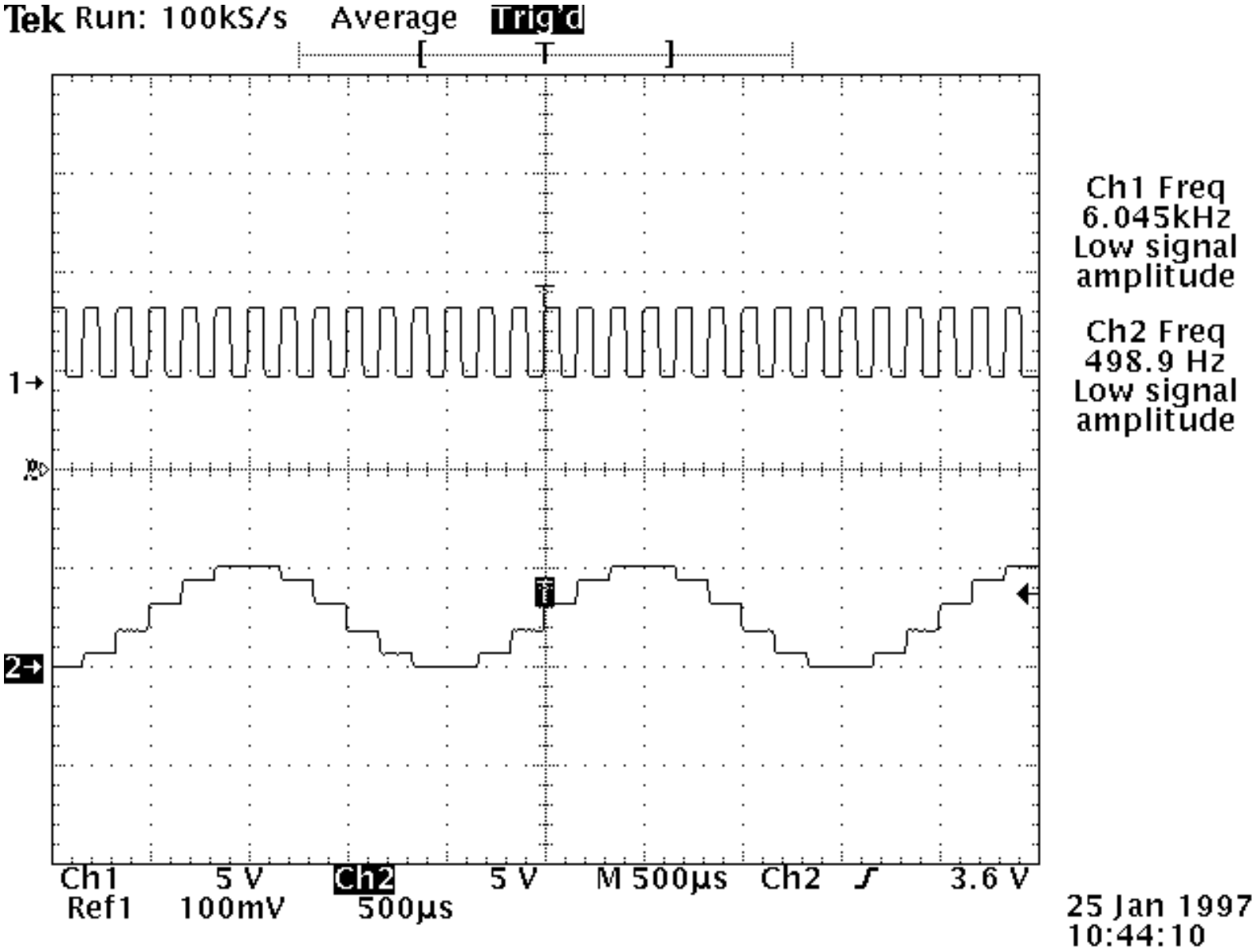
Disadvantages: Harmonic distortion not controlled

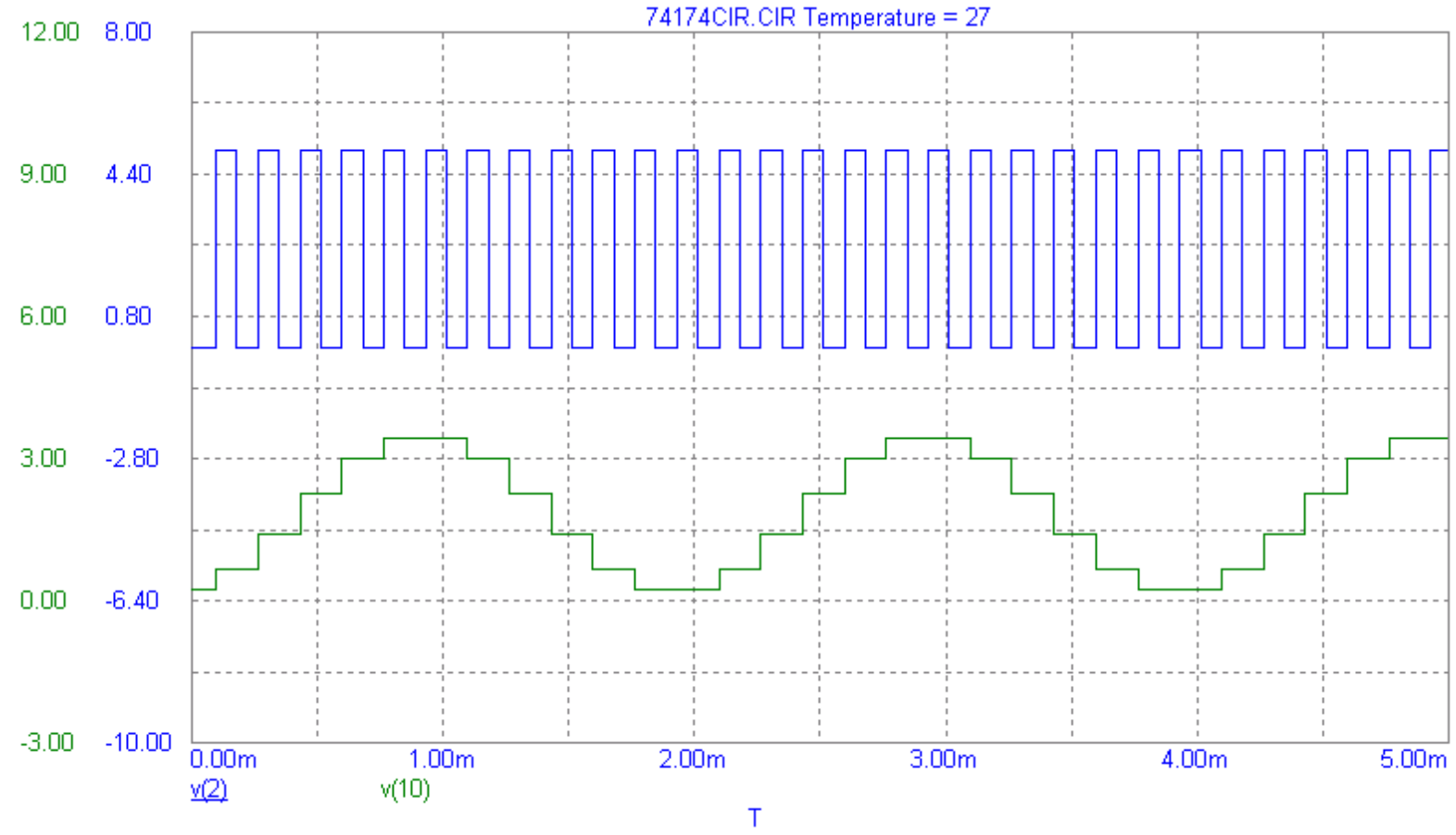
Filenames: HC04 (IsSpice) HC04mic (Mirco-cap) HC04ps (Pspice)

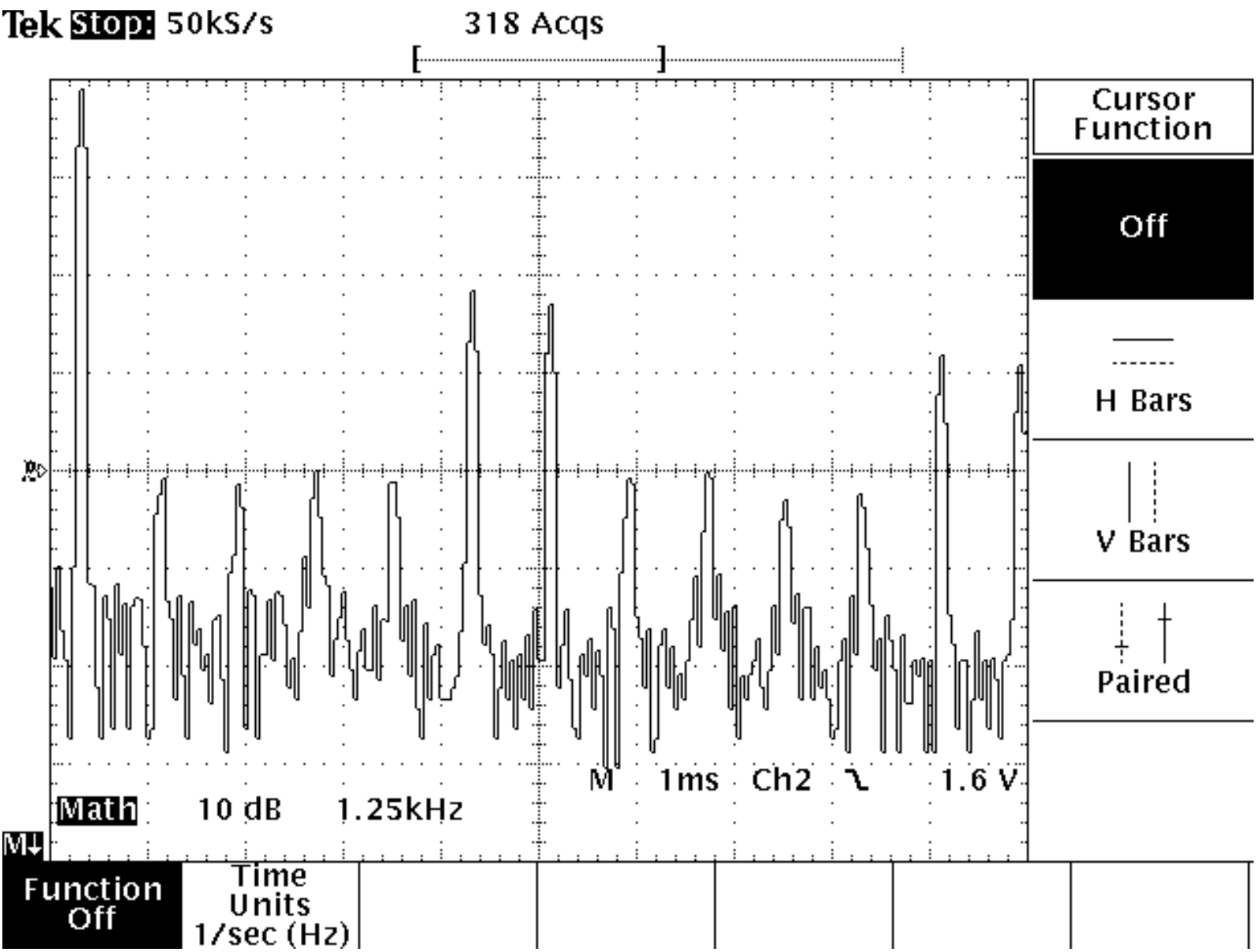

V(24)
5000STP
V(28)
+5V
X26 74174
R2
150K
R5
150K
R1
86.6K
R3
75K
R4
86.6K
CLR'
VDD
Q1
Q6
D1
D6
D2
D5
Q2
Q5
D3
D4
Q3
Q4
VSS
CLK
Z1
V(28)
+5V
C2
.1U
V(28)
+5V
X27 CD4049UB
VCC
VSS
V(1)
6KHZ

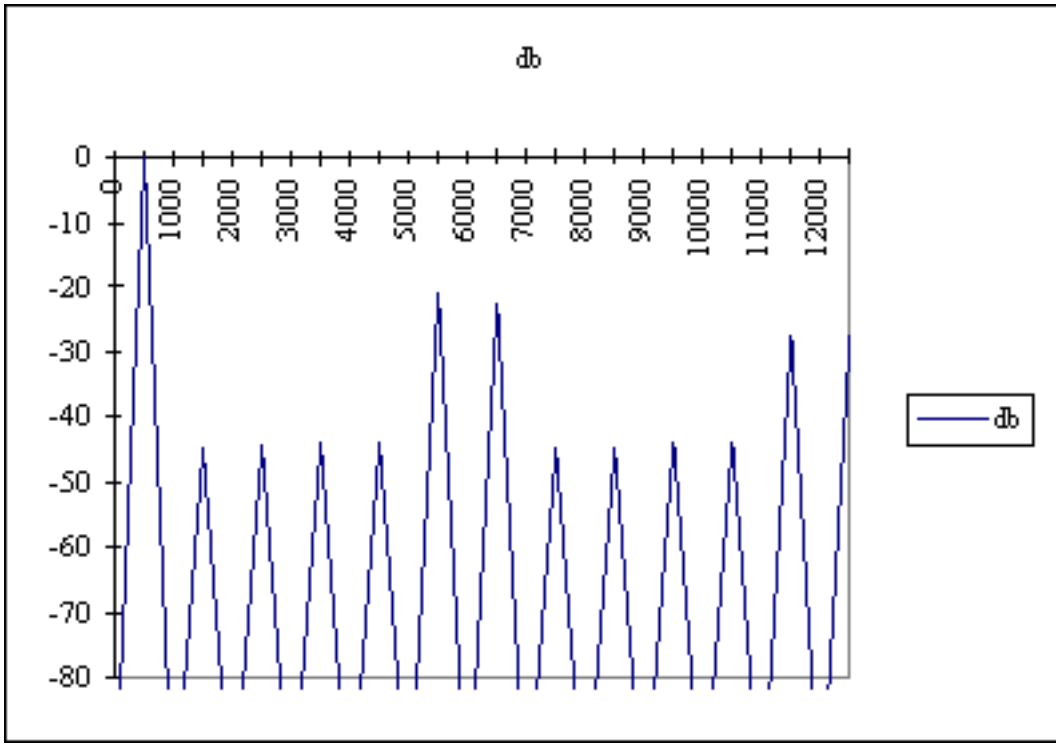

Tek Stop: 100kS/s
6169 Acqs
Ch2 Freq
500 Hz
Ch1 Freq
500 Hz
Ch1 2 V Ch2 2 V M 500µs Ch2 ⌊ 1.6 V
Ref2 100mV 500µs
25 Jan 1997
10:19:28

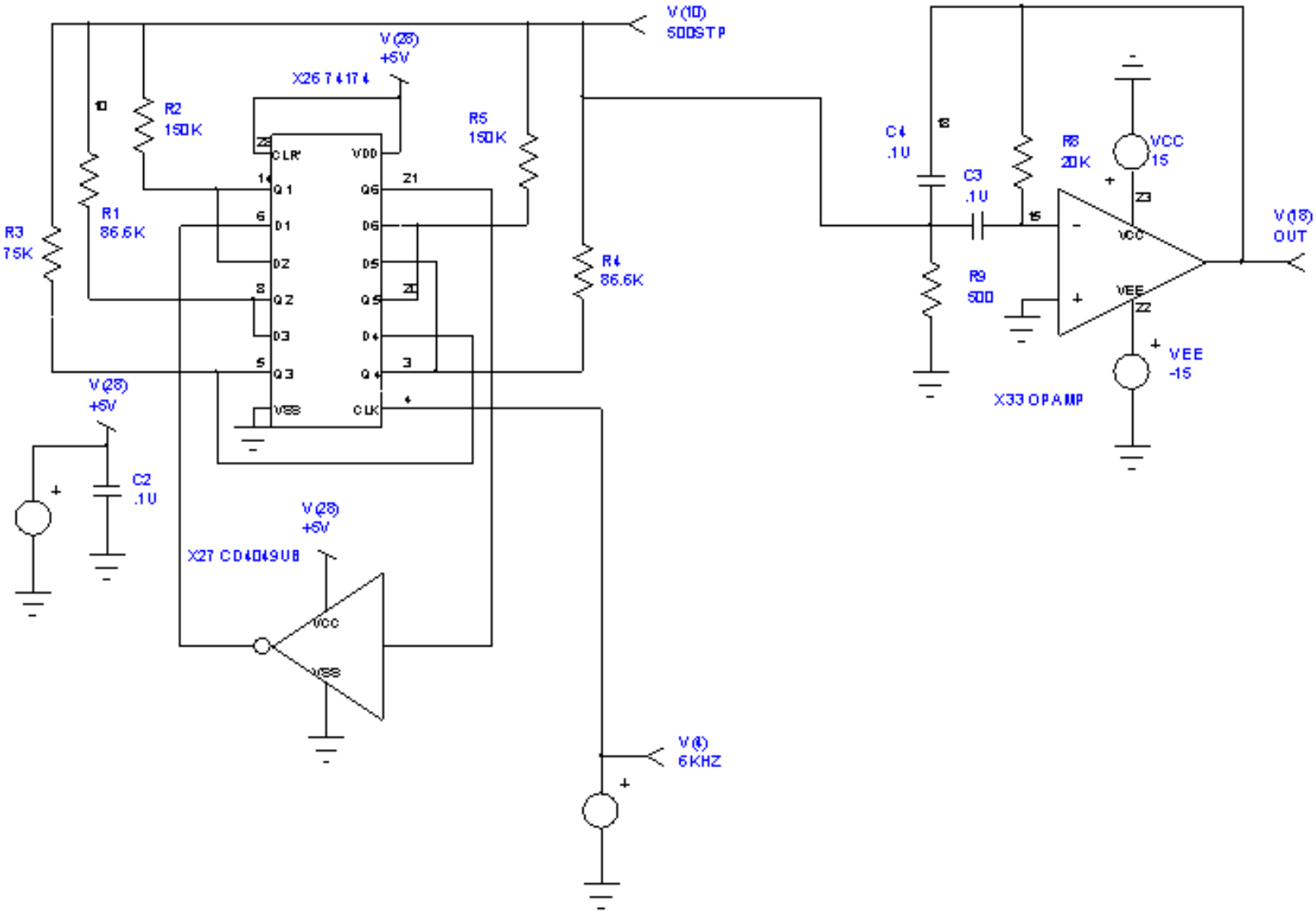

35.00
25.00
15.00
5.000
-5.000
15.00
5.000
-5.000
-15.00
-25.00
500STP in Volts
6KHZ in Volts
500.0U
1.500M
2.500M
3.500M
4.500M
TIME in Secs
2
1

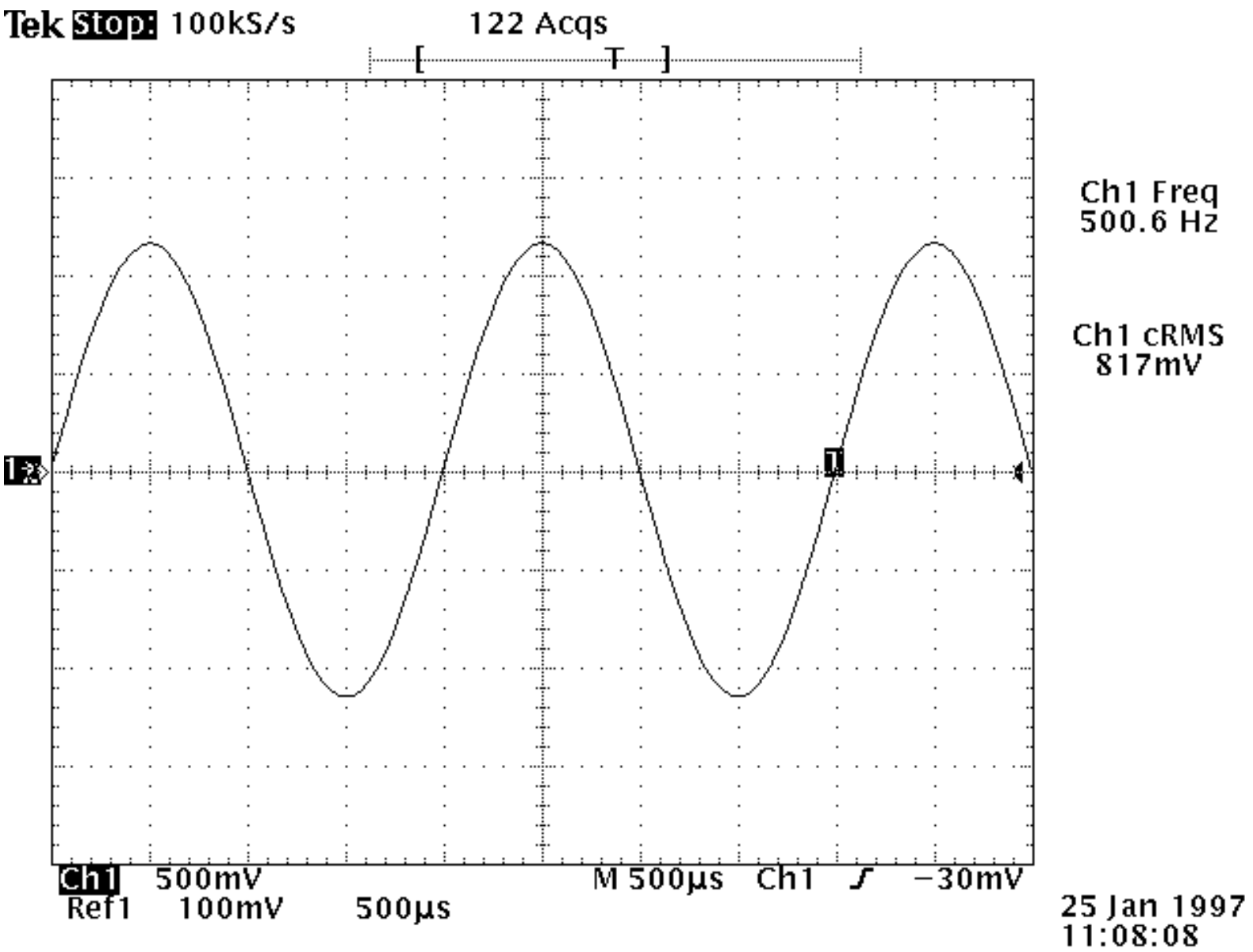

Tek Run: 100kS/s Average Trig'd
Ch1 Freq
6.045kHz
Low signal
amplitude
Ch2 Freq
498.9 Hz
Low signal
amplitude
Ch1 5 V Ch2 5 V M 500µs Ch2 ƒ 3.6 V
Ref1 100mV 500µs
25 Jan 1997
10:44:10

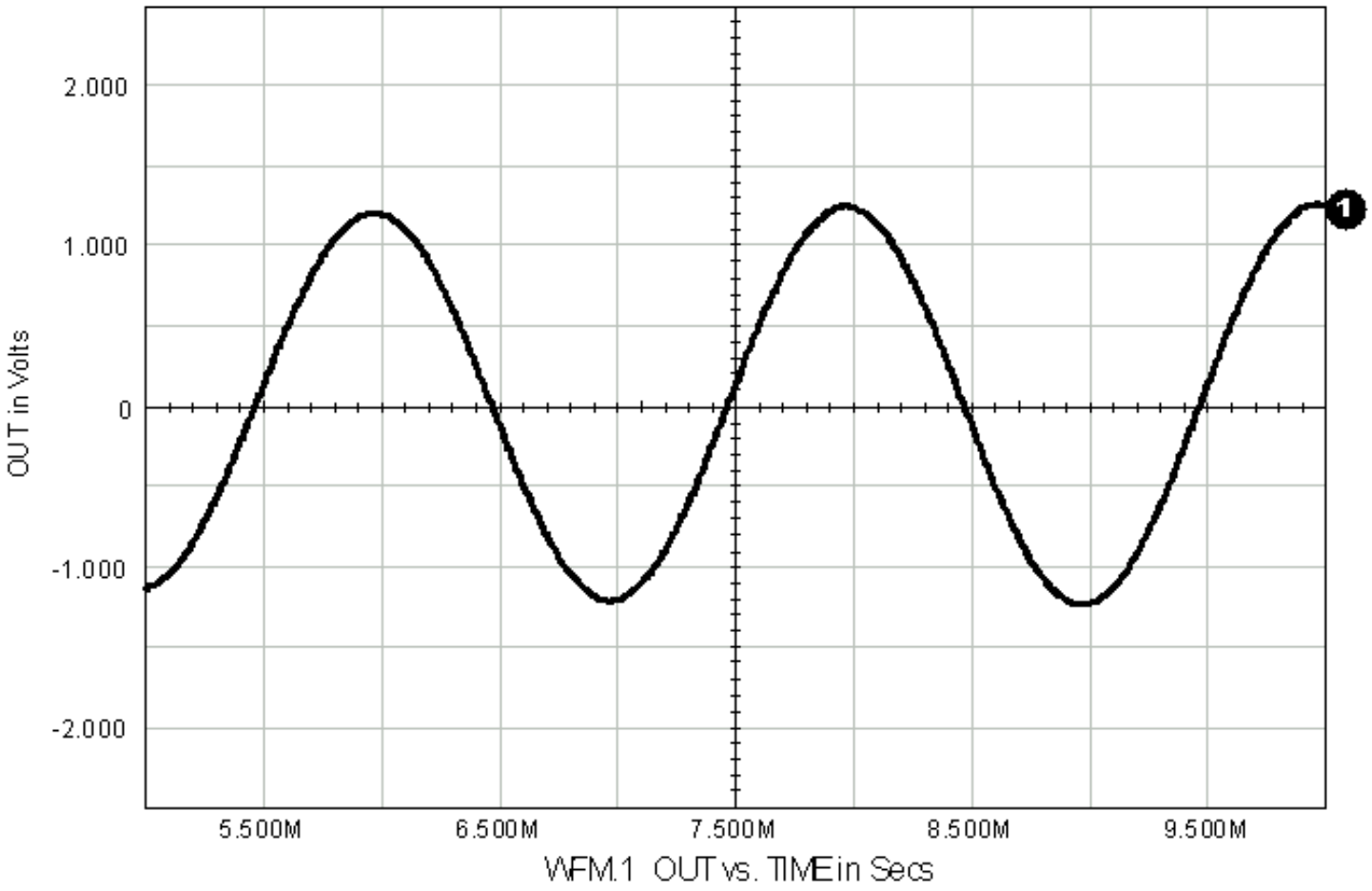

74174CIR.CIR Temperature = 27
12.00
8.00
9.00
4.40
6.00
0.80
3.00
-2.80
0.00
-6.40
-3.00
-10.00
0.00m
1.00m
2.00m
3.00m
4.00m
5.00m
v(2)
v(10)
T

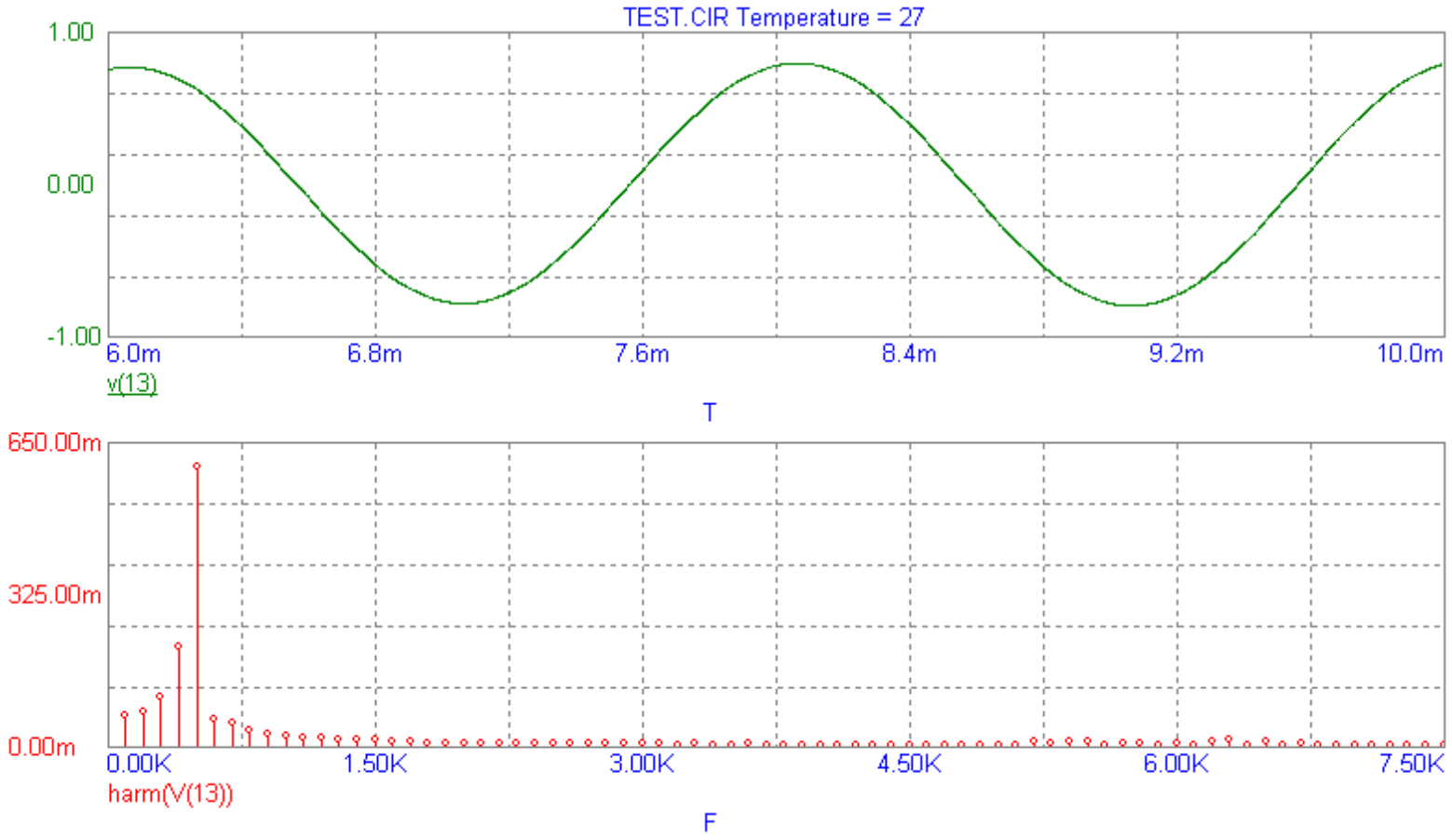

Tek Stop: 50kS/s
318 Acqs
Cursor Function
Off
H Bars
V Bars
Paired
M 1ms Ch2 ∖ 1.6 V
Math 10 dB 1.25kHz
M↓
Function Off
Time Units 1/sec (Hz)

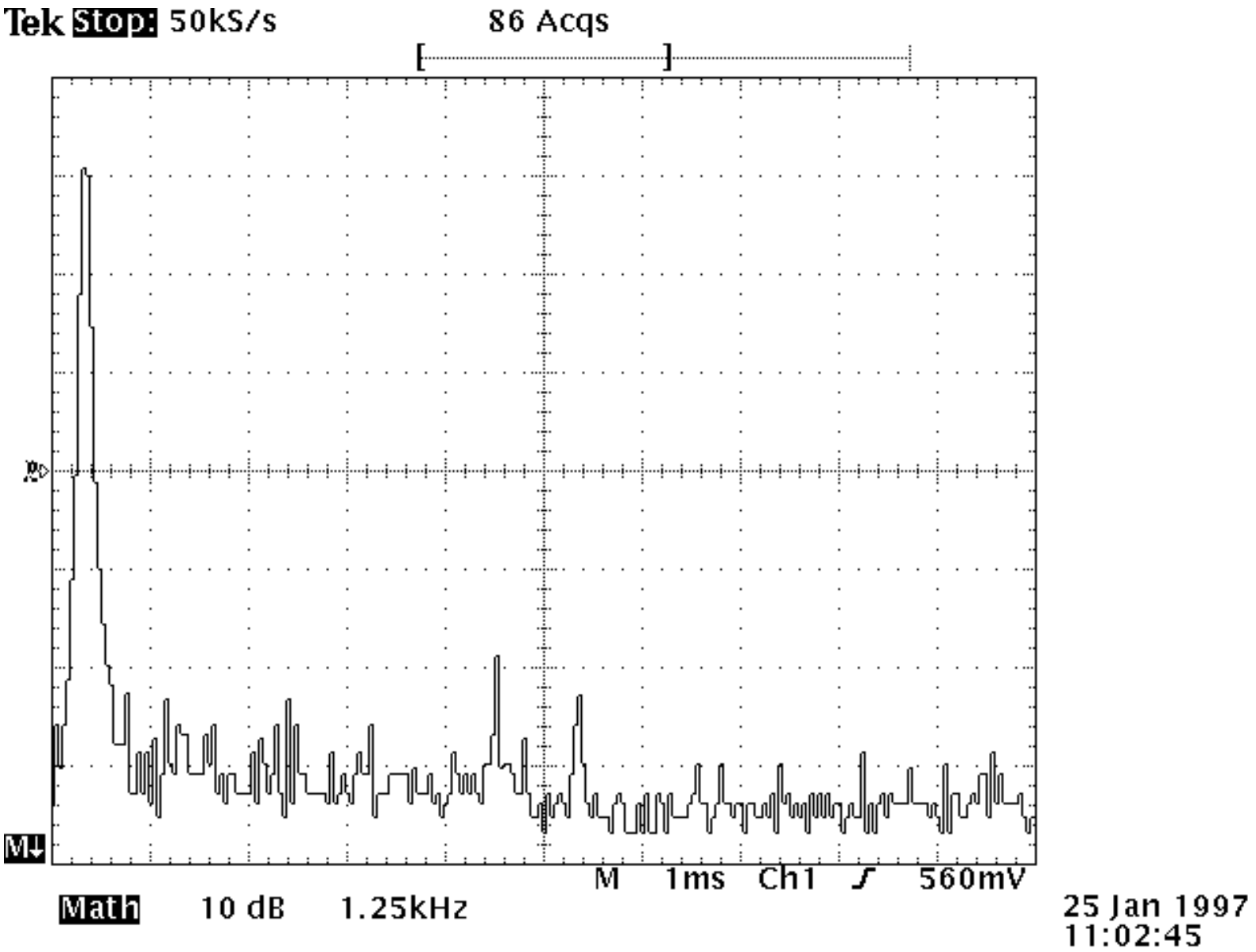

db
0
-10
-20
-30
-40
-50
-60
-70
-80
0
1000
2000
3000
4000
5000
6000
7000
8000
9000
10000
11000
12000
db

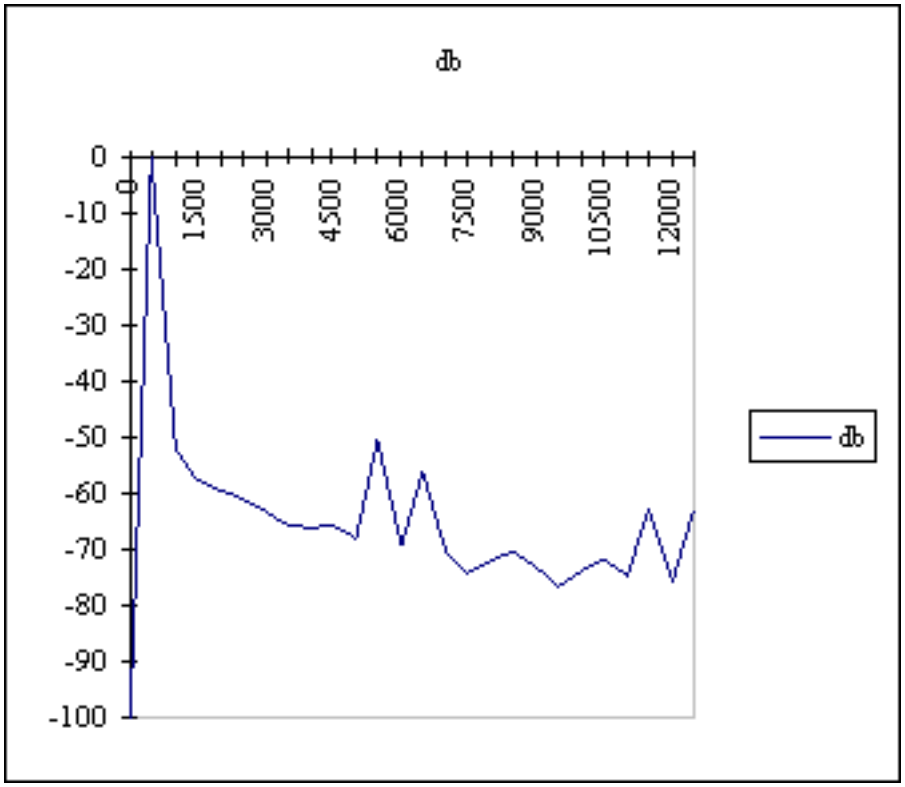

V(10)
500STP
V(28)
+5V
X26 74174
R2
150K
R5
150K
R1
86.6K
R3
75K
R4
86.6K
CLR'
VDD
Q1
Q6
D1
D6
D2
D5
Q2
Q5
D3
D4
Q3
Q4
VSS
CLK
C4
.1U
C3
.1U
R8
20K
VCC
15
R9
500
VEE
-15
V(16)
OUT
X33 OPAMP
V(28)
+5V
C2
.1U
V(28)
+5V
X27 CD4049UB
VCC
VSS
V(1)
6KHZ


Tek Stop: 100kS/s
122 Acqs
Ch1 Freq
500.6 Hz
Ch1 cRMS
817mV
Ch1 500mV
Ref1 100mV
500µs
M 500µs Ch1 ∫ −30mV
25 Jan 1997
11:08:08


2.000
1.000
0
-1.000
-2.000
OUT in Volts
5.500M
6.500M
7.500M
8.500M
9.500M
WFM.1 OUT vs. TIME in Secs
1


TEST.CIR Temperature = 27
1.00
0.00
-1.00
6.0m
6.8m
7.6m
8.4m
9.2m
10.0m
v(13)
T
650.00m
325.00m
0.00m
0.00K
1.50K
3.00K
4.50K
6.00K
7.50K
harm(V(13))
F


Tek Stop: 50kS/s
86 Acqs
M 1ms Ch1 ∫ 560mV
Math 10 dB 1.25kHz
25 Jan 1997
11:02:45


db
0
-10
-20
-30
-40
-50
-60
-70
-80
-90
-100
0
1500
3000
4500
6000
7500
9000
10500
12000
db

#40 Schmidt Trigger Oscillator

Like the Wein bridge oscillator, the Schmidt trigger only needs a power supply of 5 to 15 volts to begin its oscillation. This entails that the maximum lead that the clock pulse can drive is in the 1 milliamp range. The oscillation is controlled by the RC time constant and the hysterics native to the Schmidt trigger. The output of the Schmidt trigger charges the timing capacitor through the resistor creating the ramp signal. The ramp signal bounces back and forth between the positive and negative hysterisis point of the Schmidt trigger.

To write a model for a Schmidt trigger, the most key parameter is the positive and negative hysterisis points. Unfortunately, manufactures of the Schmidt trigger give a loose specification as to what these points are. Figure 40-1 shows data taken from the Harris Semiconductor Databook on the CD4093BMS NAND Schmidt Trigger.

Figure 40-1: CD4093BMS NAND Schmidt Trigger Specifications

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	MAX	UNITS
Positive Trigger Threshold Voltage	VP5V	VDD=5V (Note 4)	-55 - +125	2.6	4	V
Negative Trigger Threshold Voltage	VN5V	VDD=5V (Note 4)	-55 - +125	1.4	3.2	V
Hysteresis Voltage	VH5V	VDD=5V (Note 4)	-55 - +125	0.3	1.6	V

As you can see, it is unclear at what voltage level the hysterisis will center around or what the separation between the positive and negative switching points will be. A good model should hit the average of the specification, but it is unlikely that a part will perform in a similar manner. Realistically, the person who wrote the spice model, wrote it for a single part. Any model that performs within the specification limits of the device could be considered as correct. This makes for some interesting results from the models included with the different packages.

Consider the CD4093B model contained in the IsSpice package. The circuit is shown as figure 40-2.

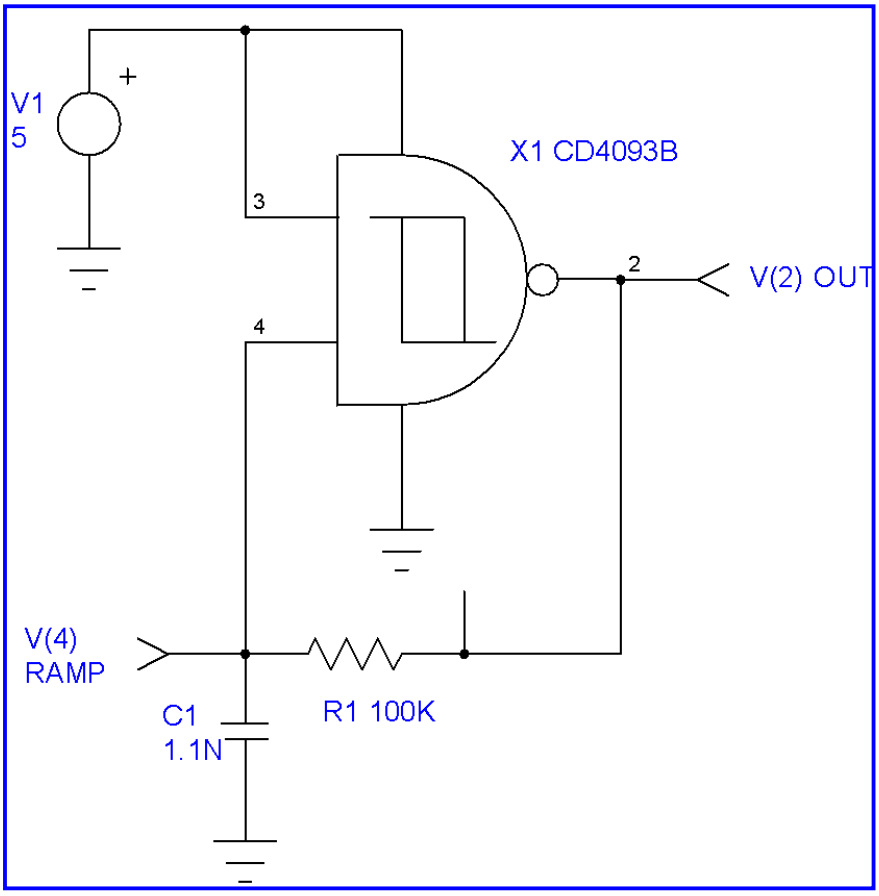


Figure 40-2: Schmidt Trigger Oscillator

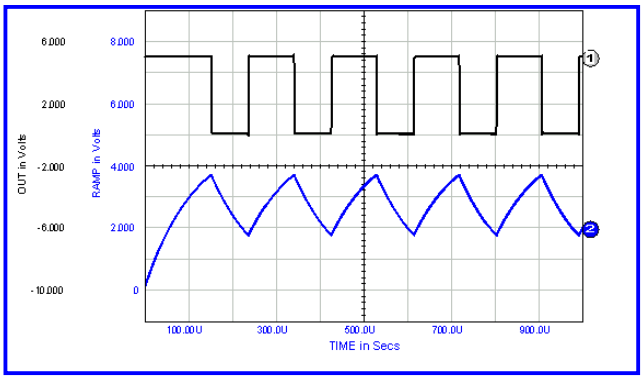


Figure 40-3: Results of IsSpice Schmidt Trigger

The IsSpice model shows that the ramp voltage peaks at 3.7 volts and has a minimum of 1.75 volts. The maximum is below the extreme high specification of 4 volts, and the minimum is above the extreme minimum specification of 1.4 volts. This seems to line up pretty close to the data sheet, but the models hysterisis voltage is 1.95 volts and the specified maximum is only 1.6 volts. The IsSpice version of the Schmidt trigger would work for some applications where the hysterisis voltage is not so critical, but for this application, the large hysterisis value caused a much lower frequency then expected. The IsSpice models frequency is 5.29 kHz.

The Pspice program did not contain model for the CD4093, so a 7414 was used in its place. The 7414 is the digital model for the Schmidt trigger inverter. To use the digital device for an analog measurement, E sources (voltage controlled voltage sources) were used as buffers. The schematic used for the Pspice model is shown as figure 40-4. The results are displayed as figure 40-5.

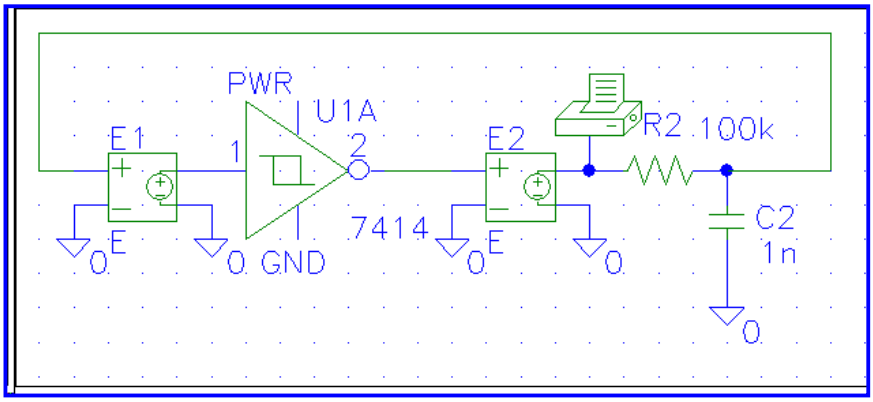


Figure 40-4: Pspice using digital Schmidt trigger

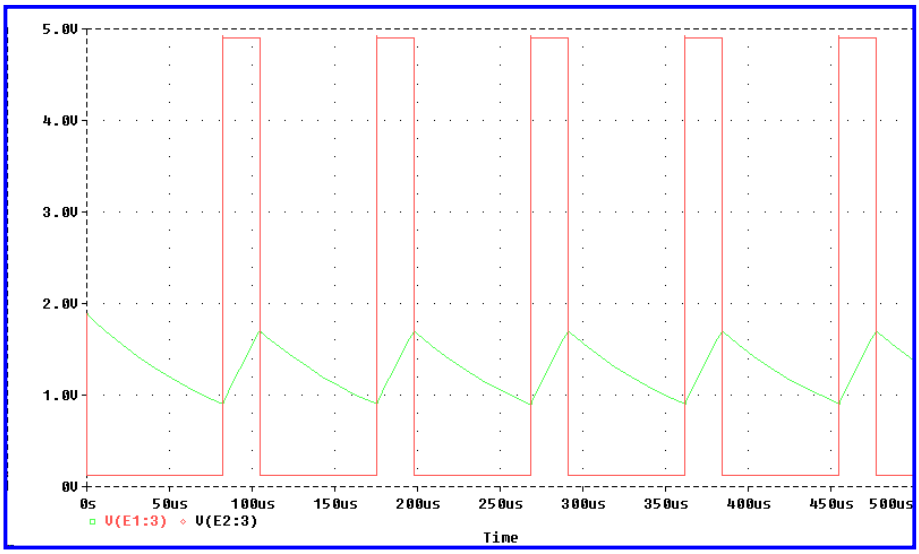


Figure 40-5: Pspice results of Schmidt trigger oscillator

The results of the Pspice digital model show that the hysterisis voltage is within the specification limits at 790 mV. The minimum positive threshold voltage is 1.65 V and model shows it at 1.69, meeting this specification also. The only problem is the model does not meet the minimum negative threshold of 1.1 V, the model shows it down at 0.9 V. With the exception of the negative threshold, Pspice has a valid model of the schmidt trigger. Unfortunately the negative threshold of the Pspice model causes an this particular circuit to not report the a proper duty cycle or frequency.

Microcap has a model of the CD4093A. The results of the simulation of the Microcap model are shown as figure 40-6.

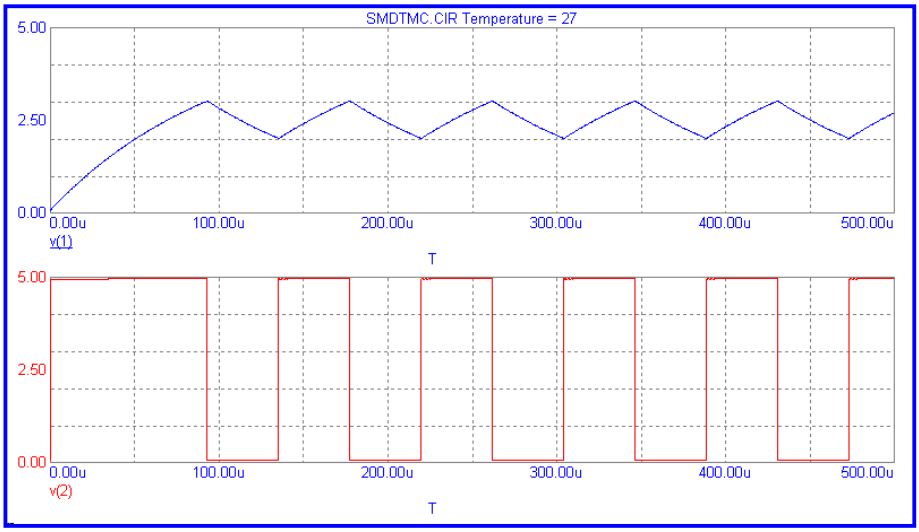


Figure 40-6: Microcap results of Schmidt trigger oscillator

The microcap results correlate very well to the data sheet. The hysterisis voltage is right at one volt, well within the limits of the 0.3 to 1.6 volt limits. The positive threshold voltage is 3 volts which is within the 2.6 to 4 volt limit. The negative threshold voltage is 2 volts which is between the 1.4 to 3.2 volt limit. Microcap's model of the schmidt trigger is clearly valid from the for the parameters evaluated in this comparison.

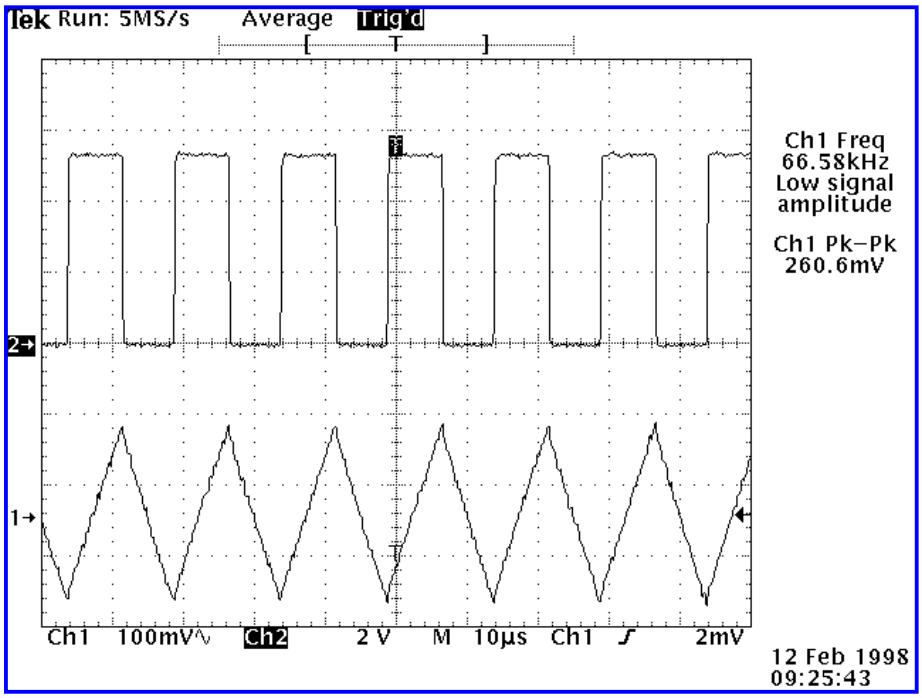


Figure 40-7: Circuit board data from Schmidt trigger oscillator

Comparing the Spice models to the measured data shown in figure 40-7 is difficult to do. The measured data shows the hysterisis voltage to be 250 mV. This does not meet the minimum specification limit of 300 mV. The minimum and maximum threshold voltages were close to 2.5 volts which does meet the specification limit. These measurements bring out a serious problem with this type of circuit. The frequency of oscillation can change dramatically due to the wide variance of hysterisis voltage, causing difficulty in modeling this circuit.

Run Time Summary

IsSpice v 7.6	PsPice v 6.3	Micro-Cap V v2
154.233 Sec	204.11 Sec	255.488 Sec
Advantages: Low part count, good drive capability.		
Disadvantages: Frequency of oscillation and duty cycle unpredictable due to poor tolerance of hysterisis voltage and voltage thresholds.		

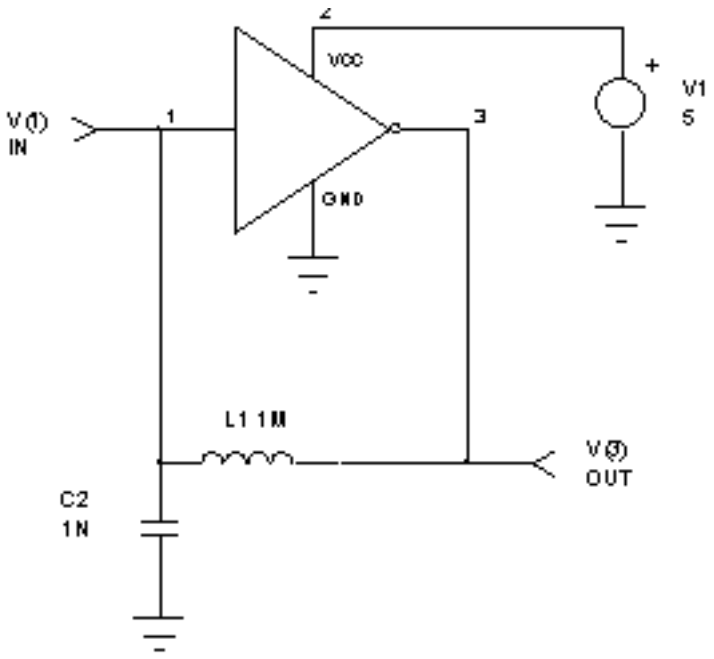
References

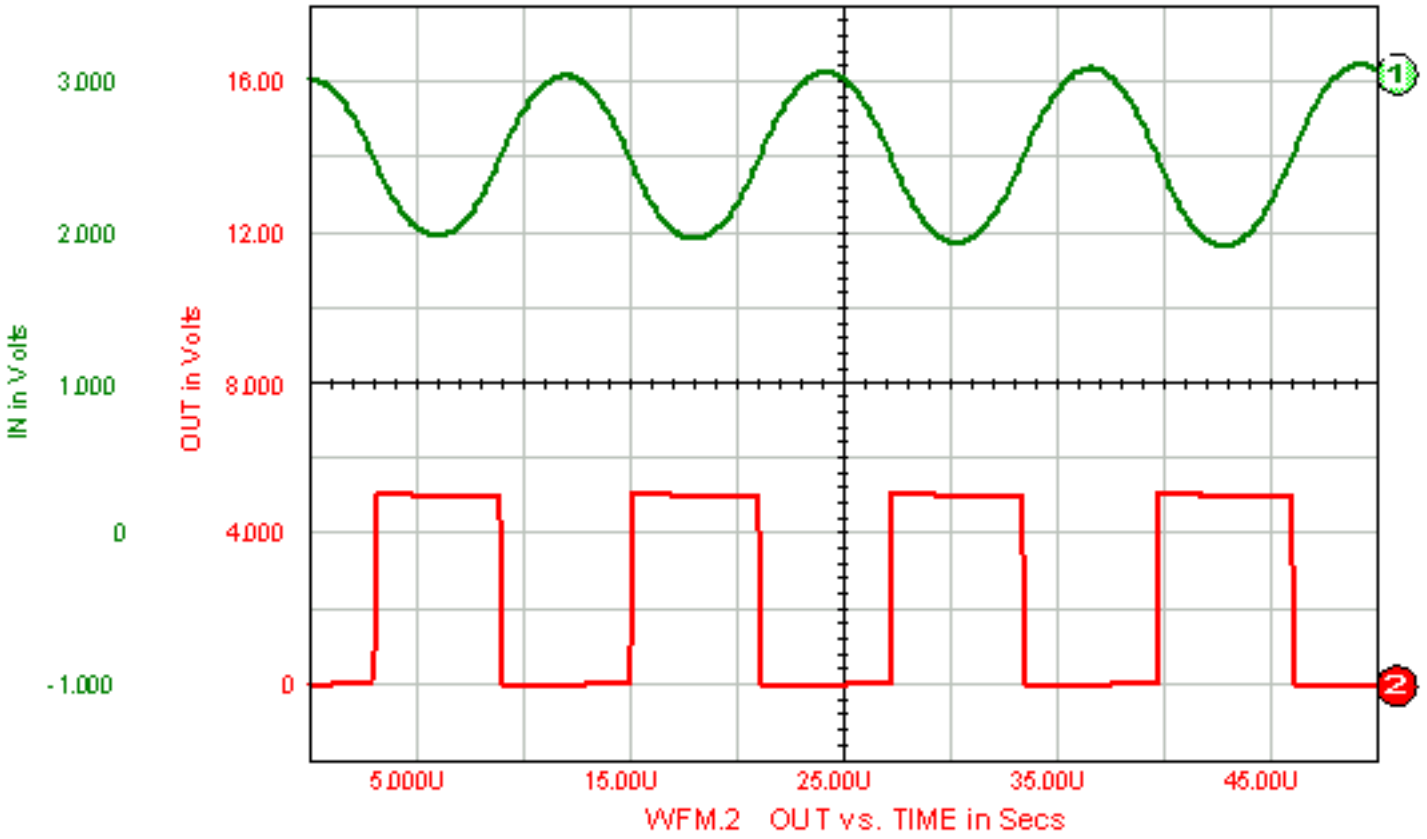
Kielkowski, Ron M. 1994. Inside Spice. New York: McGraw Hill.

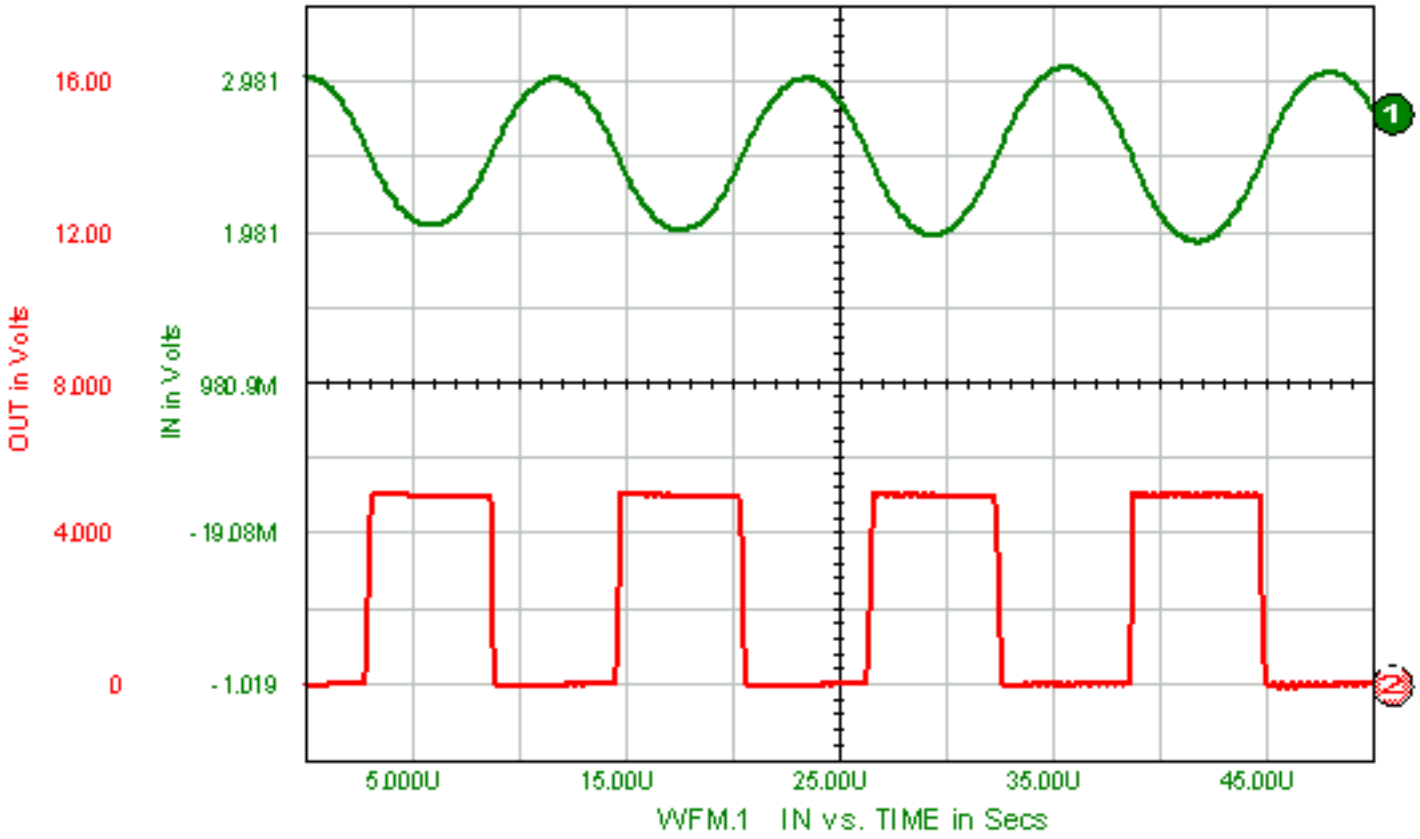
National Semiconductor, 1994. Linear Applications Handbook.

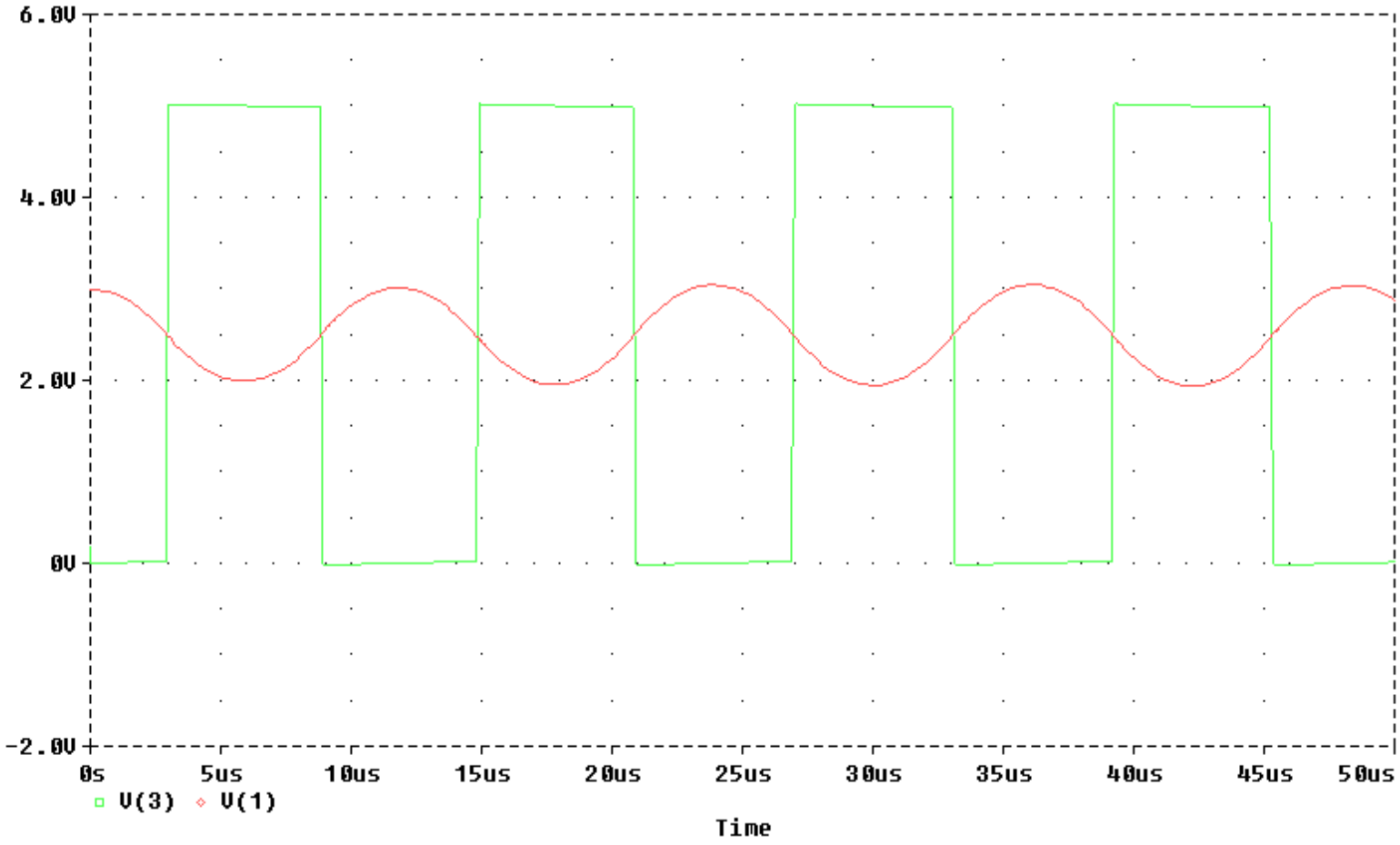
Parker, Sybil, ed. 1984. Concise Encyclopedia of Science and Technology. New York: McGraw Hill

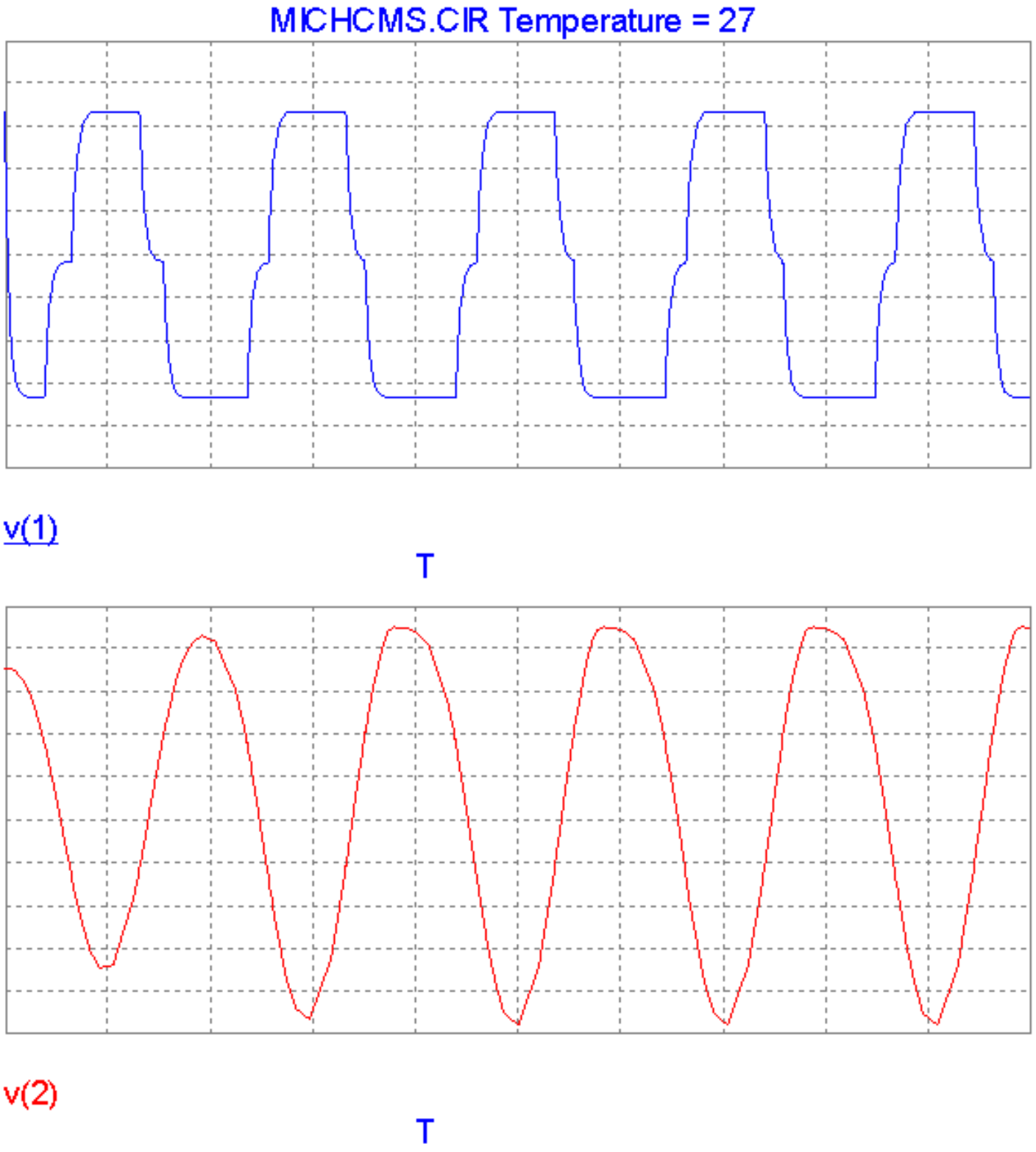
Harris Semiconductor, 1993. Radiation Hardened Product Databook.

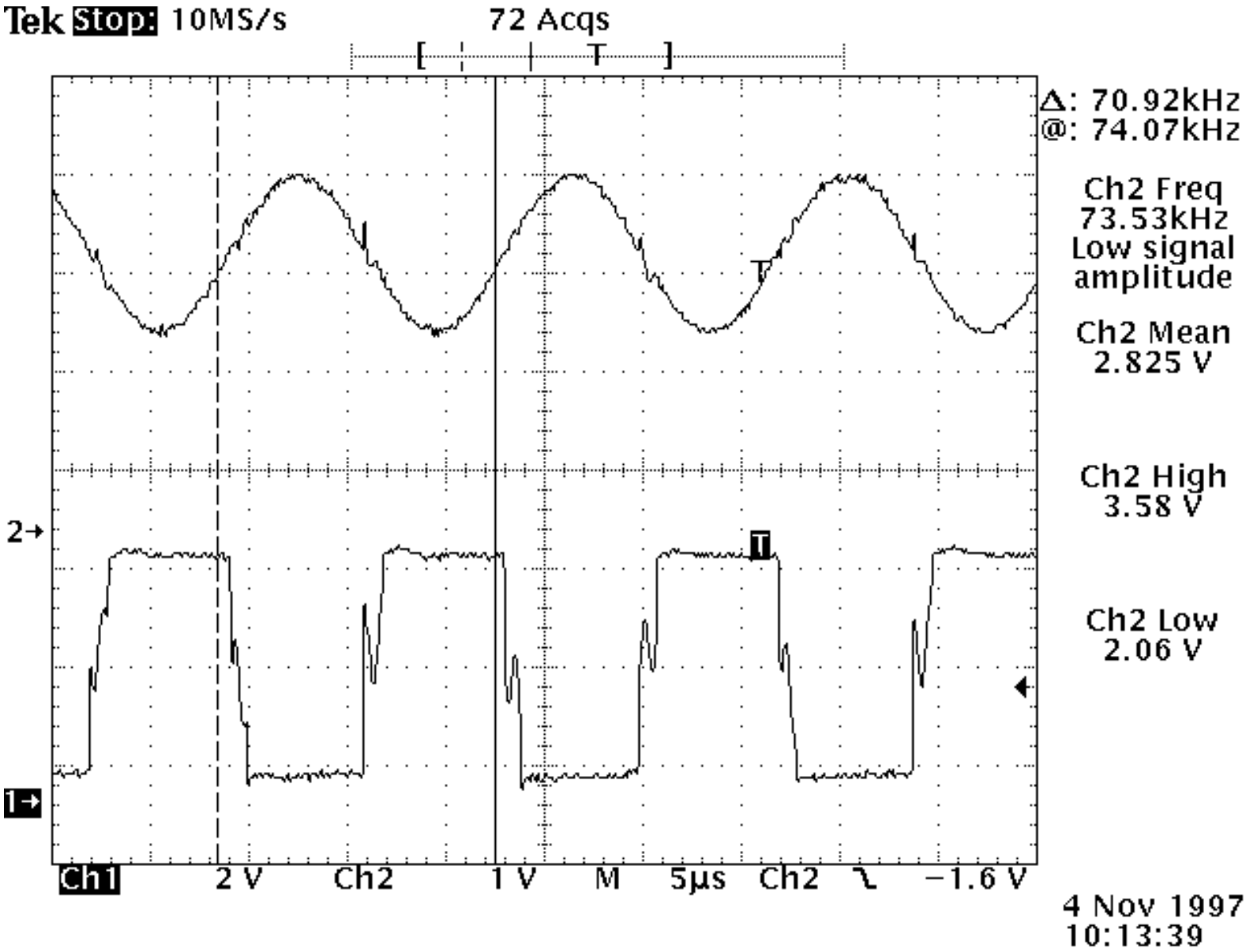

2
VCC
+
V1
5
V(1)
IN
1
3
GND
L1 1M
V(3)
OUT
C2
1N


3.000
2.000
1.000
0
-1.000
IN in Volts
16.00
12.00
8.000
4.000
0
OUT in Volts
1
2
5.000U
15.00U
25.00U
35.00U
45.00U
WFM.2 OUT vs. TIME in Secs


16.00
12.00
8.000
4.000
0
OUT in Volts
2.981
1.981
980.9M
-19.08M
-1.019
IN in Volts
5.000U
15.00U
25.00U
35.00U
45.00U
WFM.1 IN vs. TIME in Secs
1
2


6.0V
4.0V
2.0V
0V
-2.0V
0s
5us
10us
15us
20us
25us
30us
35us
40us
45us
50us
V(3)
V(1)
Time


MICHCMS.CIR Temperature = 27
v(1)
T
v(2)
T


Tek Stop: 10MS/s
72 Acqs
Δ: 70.92kHz
@: 74.07kHz
Ch2 Freq
73.53kHz
Low signal
amplitude
Ch2 Mean
2.825 V
Ch2 High
3.58 V
Ch2 Low
2.06 V
2→
1→
Ch1 2 V Ch2 1 V M 5µs Ch2 ⌊ −1.6 V
4 Nov 1997
10:13:39

#41: LM111 Oscillator

The LM111 makes an interesting oscillating circuit. The reference lead of the comparator changes as the comparator changes states. When the output lead of the comparator is low it acts as a ground putting R16 and R6 in parallel, thus setting the reference of the comparator to its low value. C10 is then allowed to discharge through R17 and the output of the comparator until it reaches the low state of the reference pin. The comparator switches just after these pins match and essentially open circuits the output of the comparator. This causes R43 and R16 to be in parallel with R7, which causes the voltage at the reference pin to reach its high state. C10 is charged up through R43 and R17 until it matches the reference voltage, then the process repeats itself creating the oscillation. The circuit is shown in figure 1 and the output of the actual and simulated circuits are shown in figure 2 Through figure 5 respectively. The simulation results are shown in Table 1.

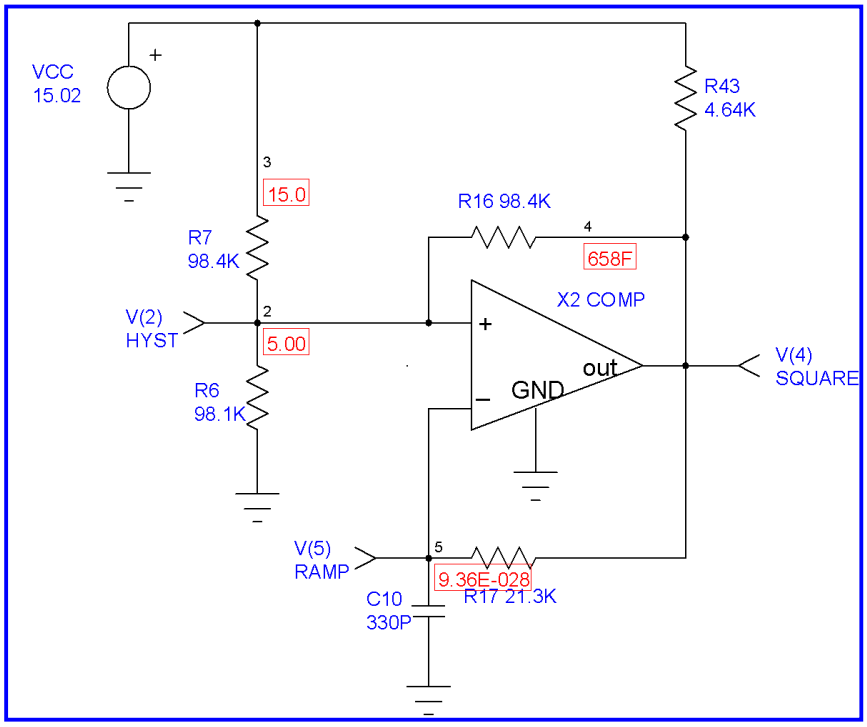


Figure 41-1: LM111 Oscillator Circuit

Simulator	File Name	Frequency	Run Time
Hardware	NA	90.98 KHZ	NA
Pspice	LM111ps	94.5 KHz	1.59 Sec
Micro-Cap V	LM111mc	95.1 KHZ	4.99 Sec
Ispice	LM111is	95.2 KHz	2.016 Sec

Table 41-1: Simulation Results

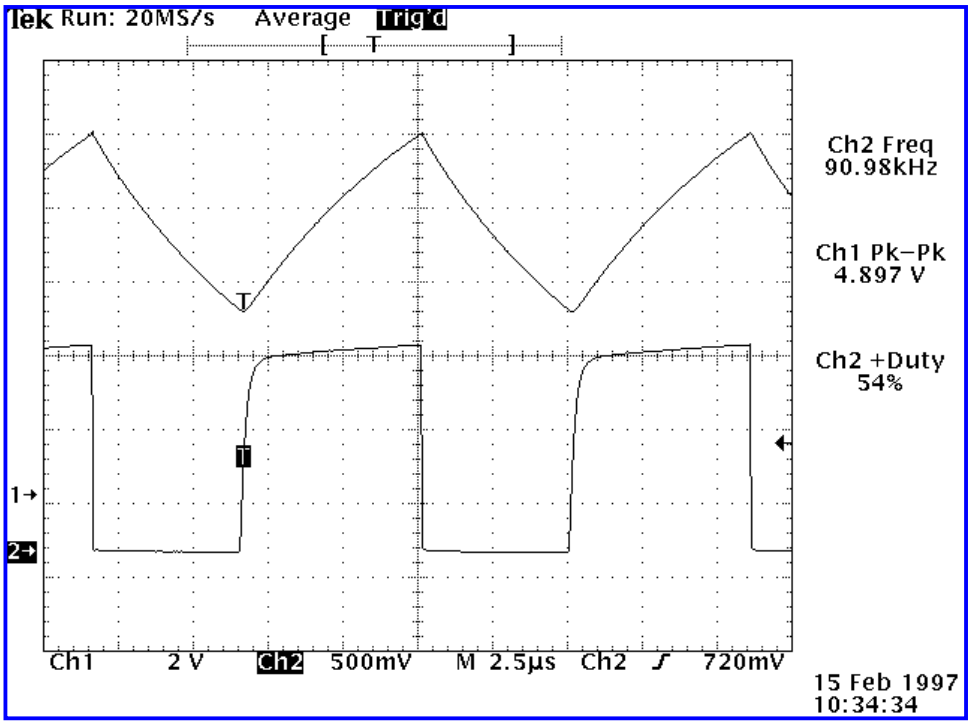


Figure41-2: LM111 Oscillator Measured Results

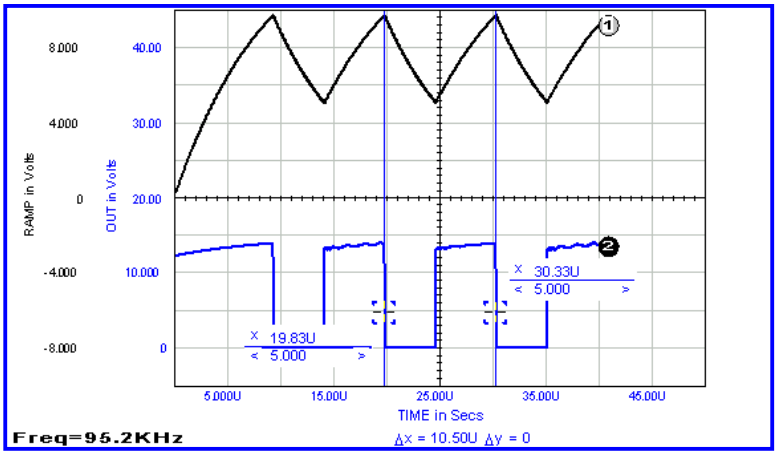


Figure 41-3: Ispice LM111 Oscillator Simulated Results

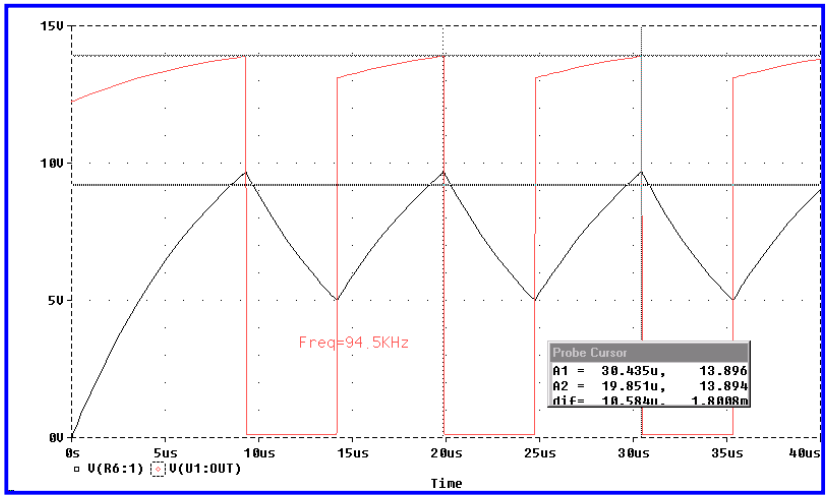


Figure 41-4: Pspice LM111 Oscillator Simulated Results

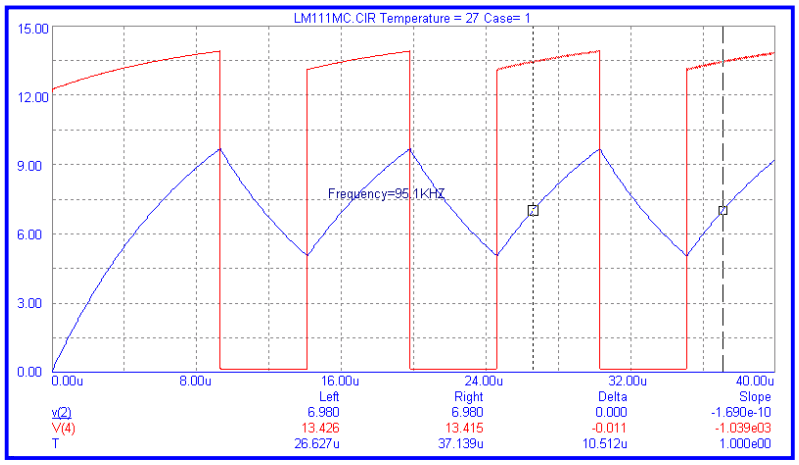
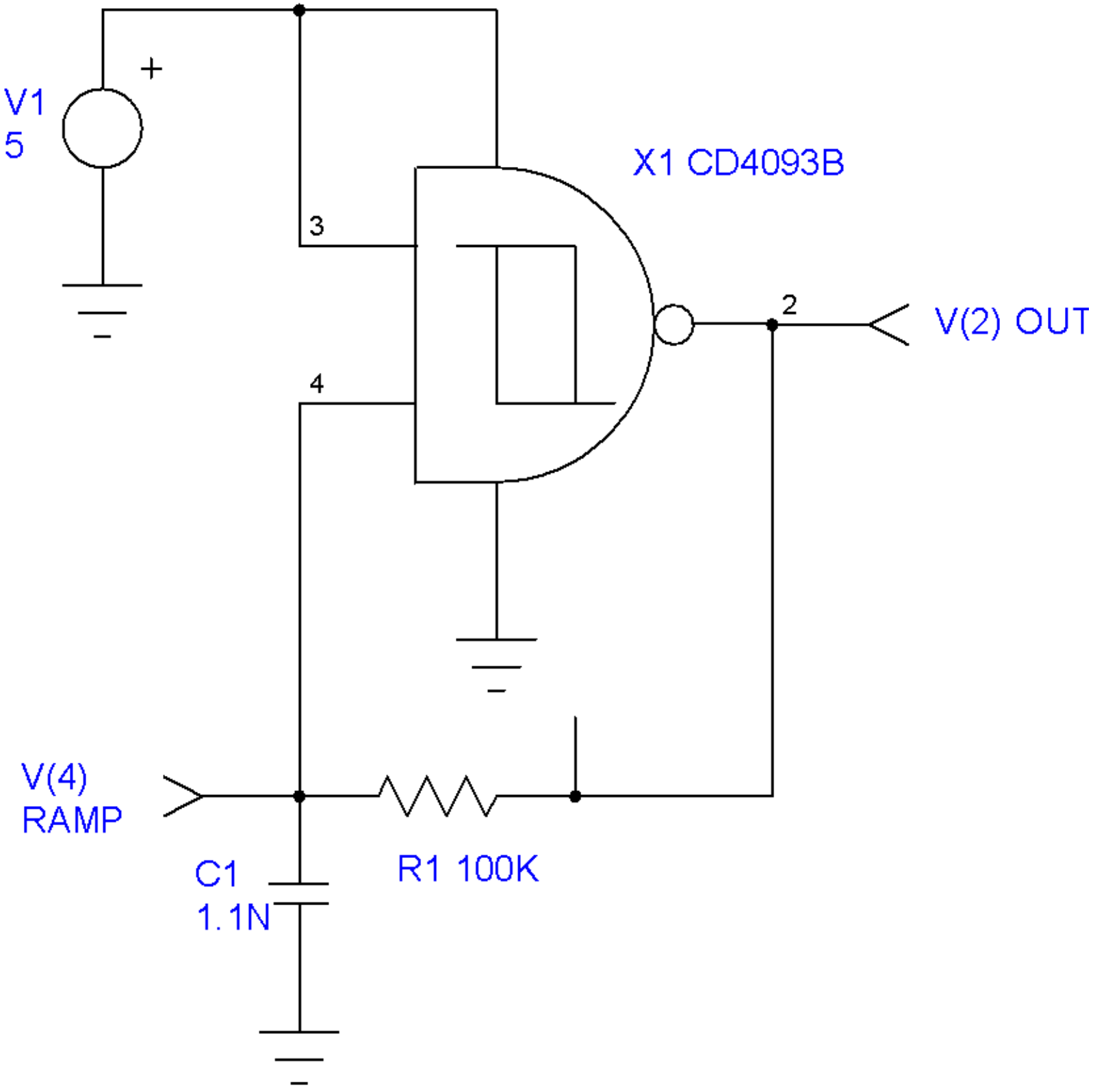
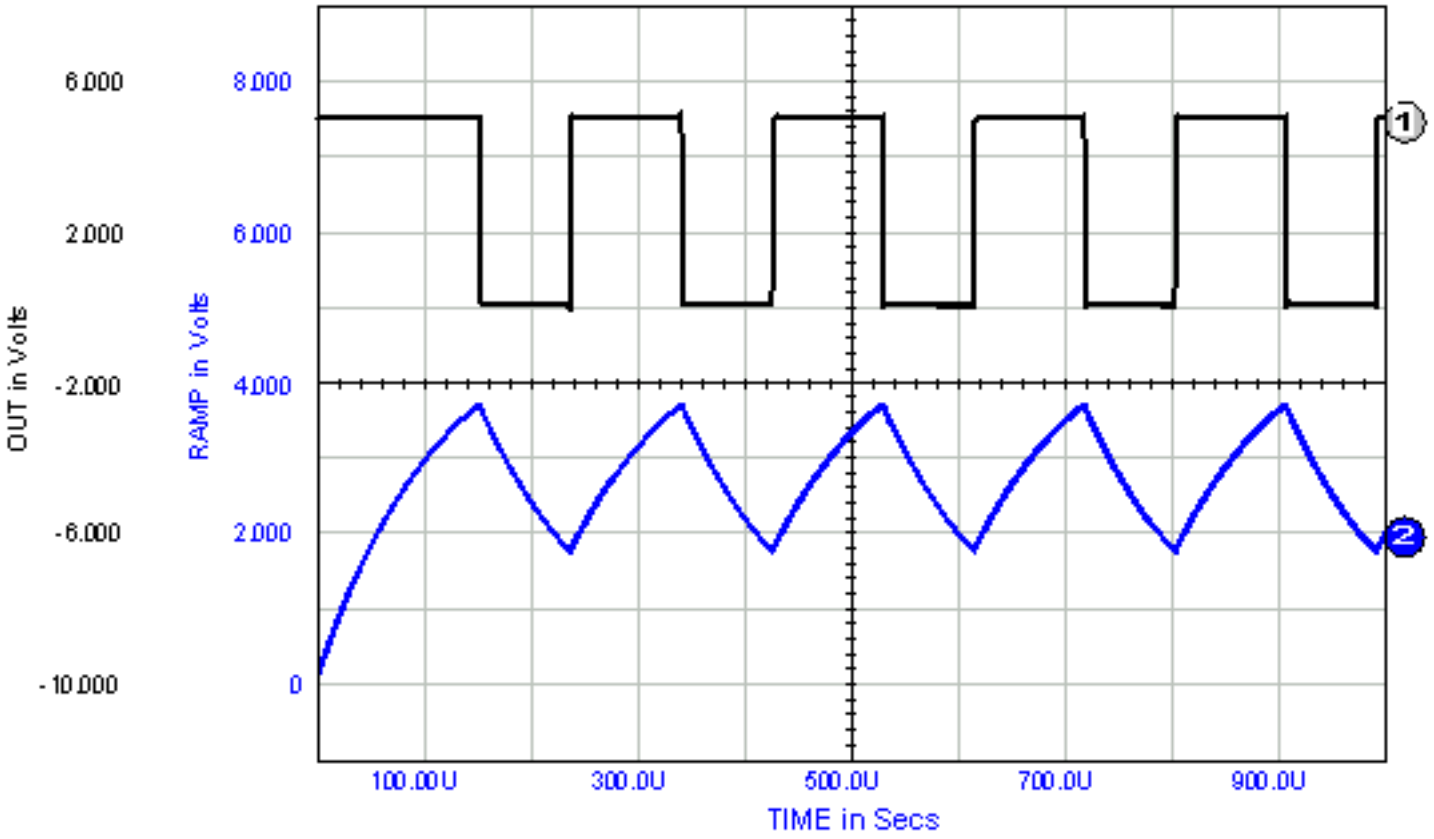
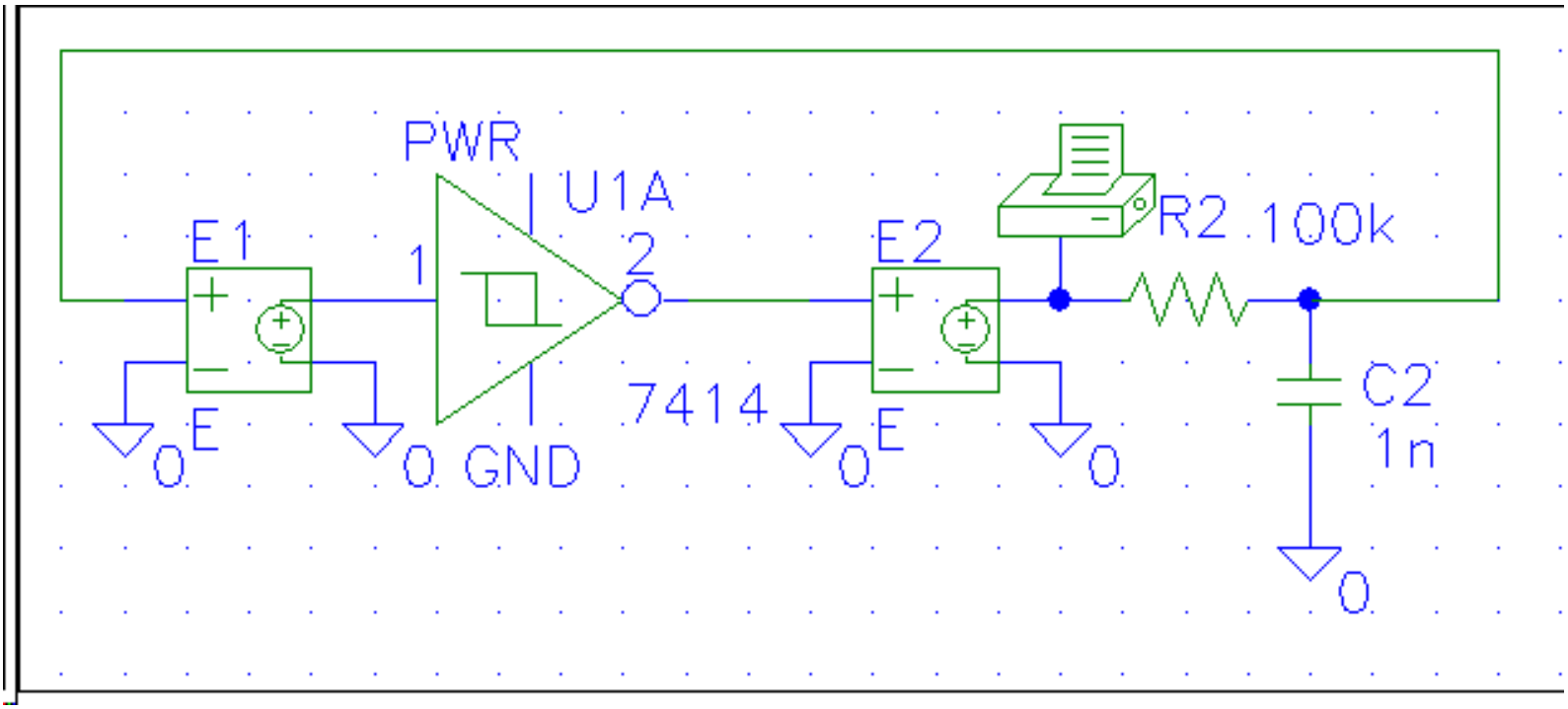
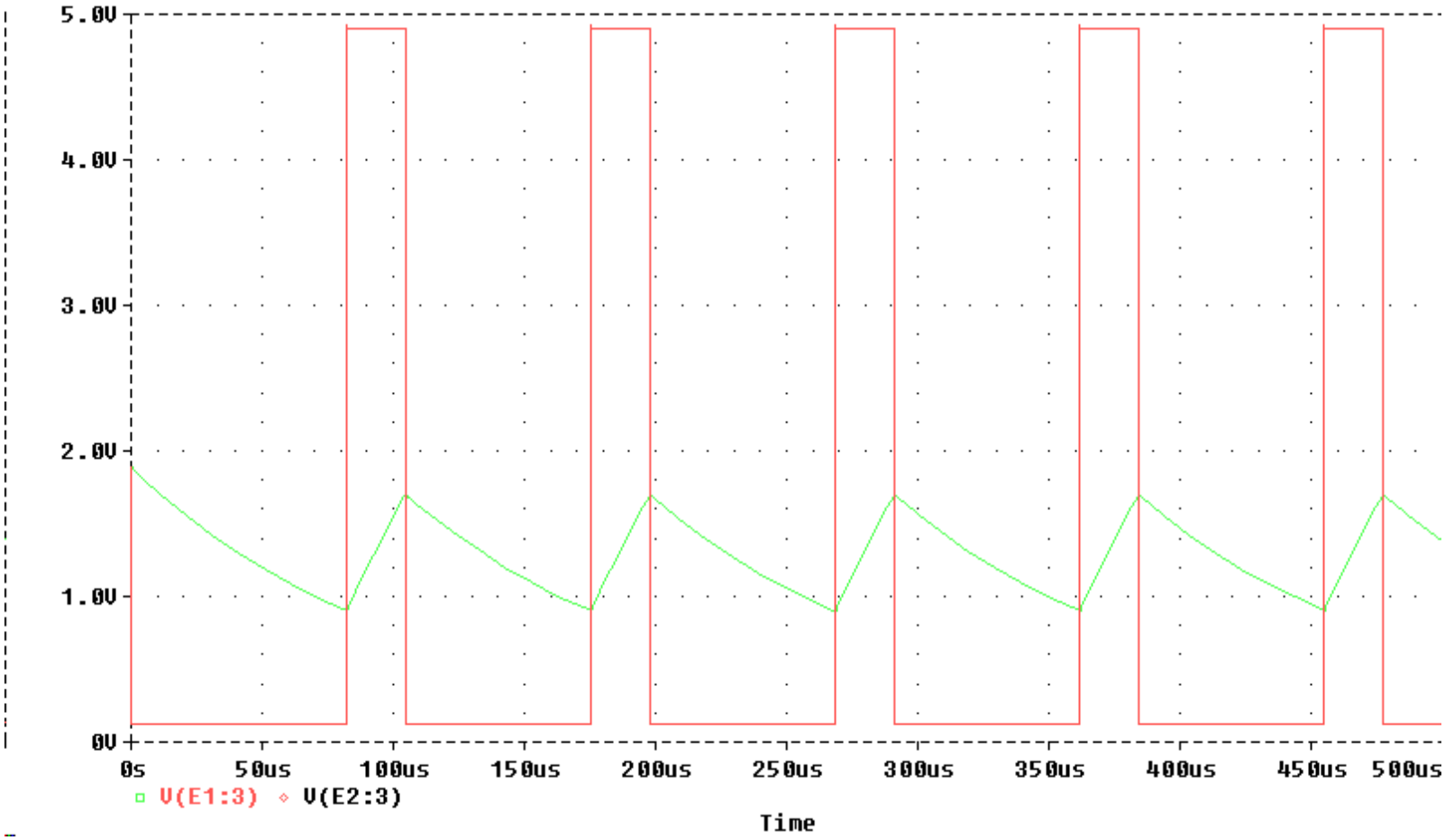


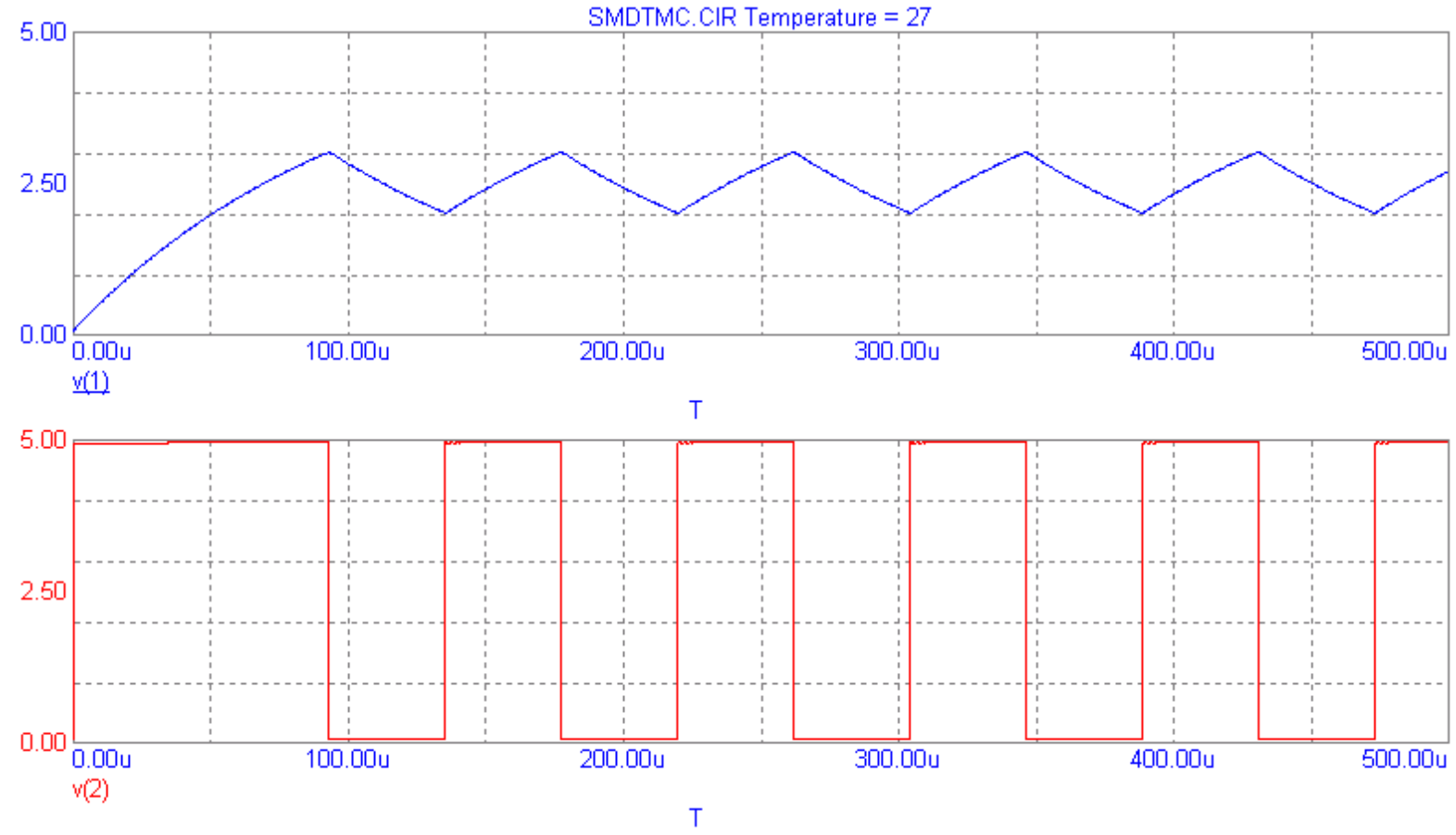
Figure 41-5: Micro-Cap V LM111 Oscillator Simulated Results

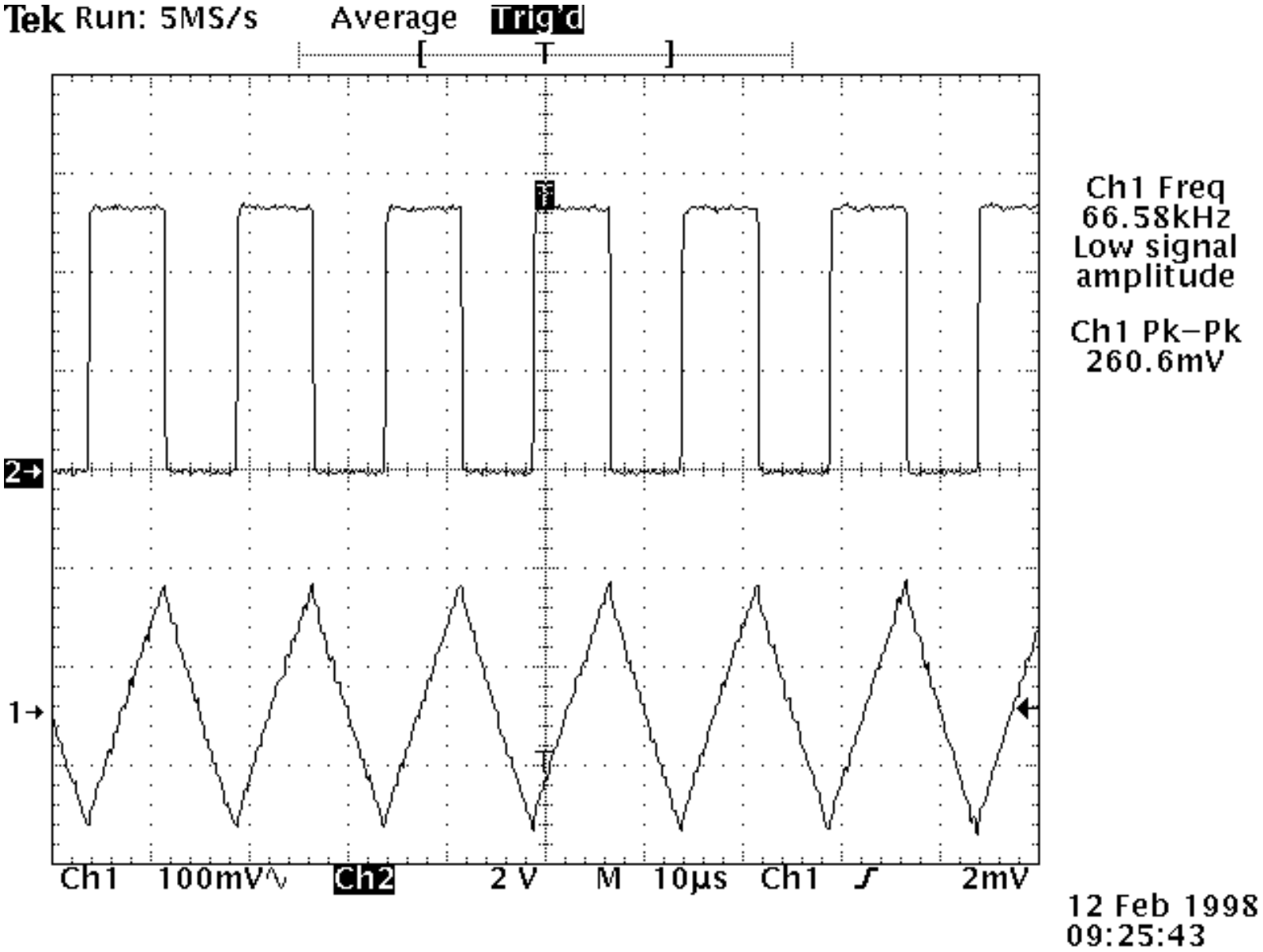

V1
5
+
X1 CD4093B
3
4
2
V(2) OUT
V(4)
RAMP
C1
1.1N
R1 100K


6.000
2.000
-2.000
-6.000
-10.000
OUT in Volts
8.000
6.000
4.000
2.000
0
RAMP in Volts
100.00U
300.0U
500.0U
700.0U
900.0U
TIME in Secs
1
2


PWR
U1A
E1
1
2
E2
R2
100k
7414
E
E
C2
1n
0
0
GND
0
0
0


5.0V
4.0V
3.0V
2.0V
1.0V
0V
0s
50us
100us
150us
200us
250us
300us
350us
400us
450us
500us
V(E1:3)
V(E2:3)
Time


SMDTMC.CIR Temperature = 27
5.00
2.50
0.00
0.00u
100.00u
200.00u
300.00u
400.00u
500.00u
v(1)
T
5.00
2.50
0.00
0.00u
100.00u
200.00u
300.00u
400.00u
500.00u
v(2)
T

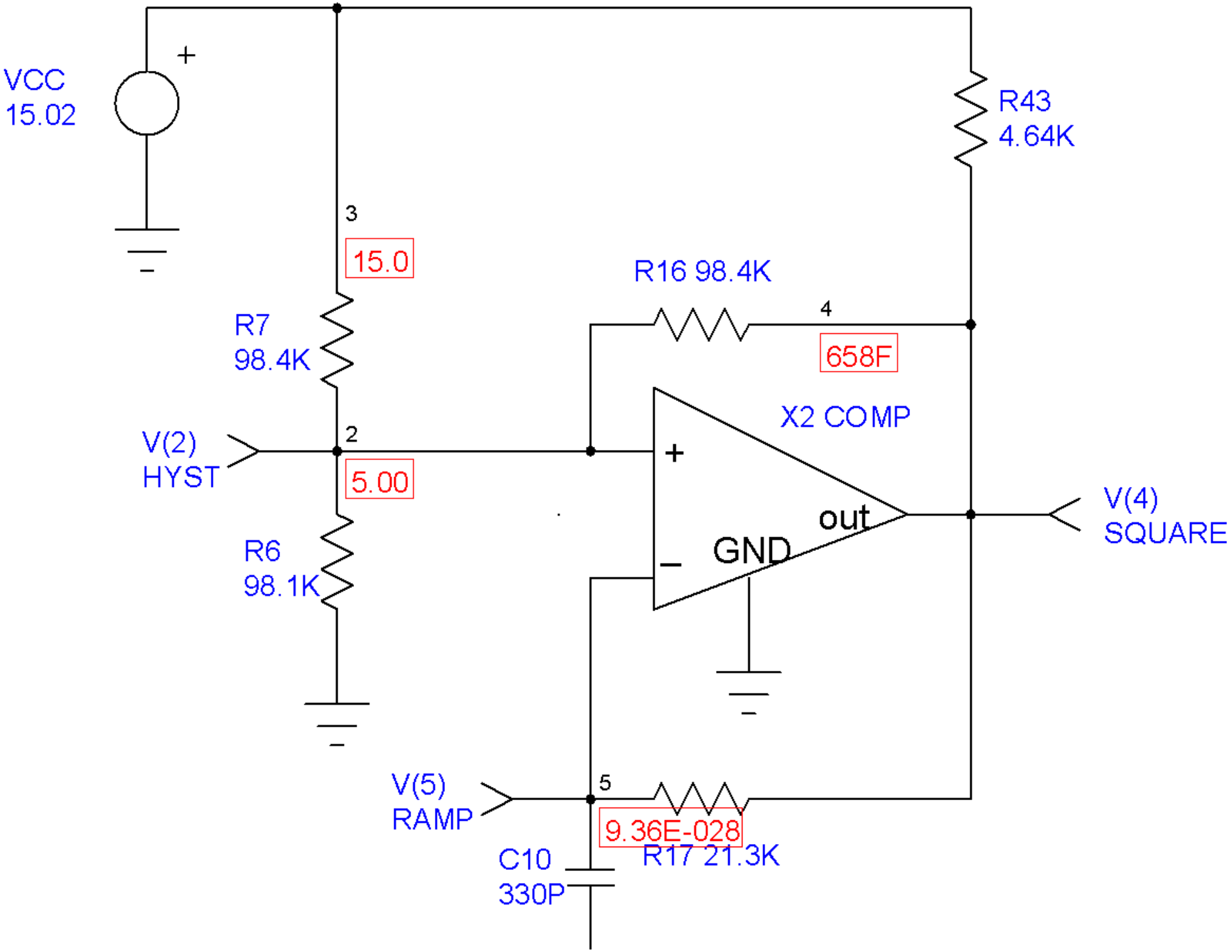

Tek Run: 5MS/s Average Trig'd
Ch1 Freq
66.58kHz
Low signal
amplitude
Ch1 Pk-Pk
260.6mV
2→
1→
Ch1 100mV Ch2 2 V M 10µs Ch1 2mV
12 Feb 1998
09:25:43

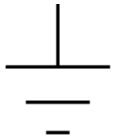
9
Gate Drive Circuits

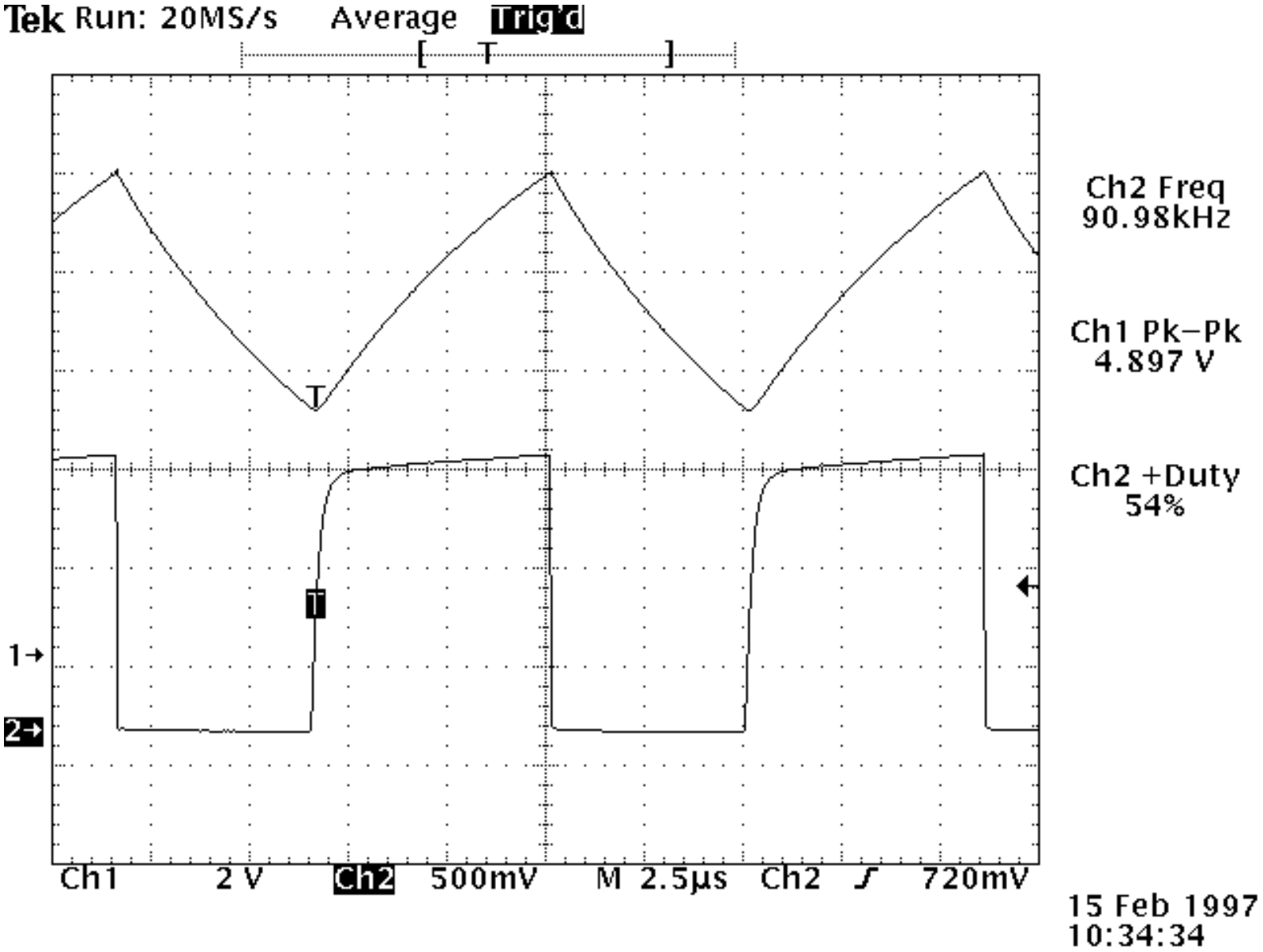
In the late 1970's, MOSFETs (Metal Oxide Semiconductor Field Effect Transistors) began replacing traditional bipolar transistors in many applications. Some of the improvements of the MOSFET over bipolar transistors include very fast switching, absence of secondary breakdown characteristics, wide safe operating area, and high gain [Application note 936A, International Rectifier]. Although MOSFETs are much easier to drive than bipolar transistors, attention must be paid to the drive circuitry to maximize the performance of these devices, as well as preventing outright device failure.

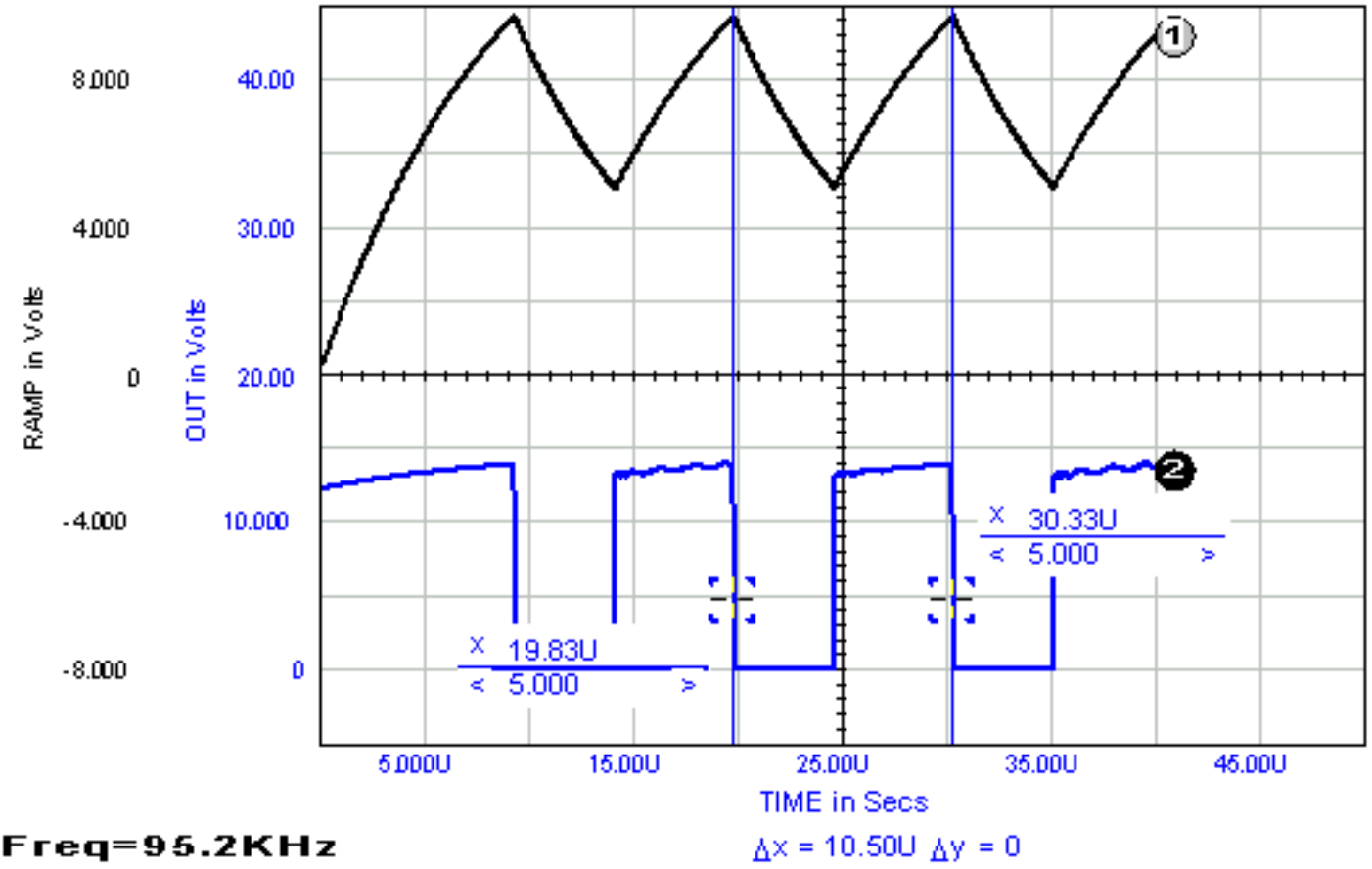
There are several behavioral characteristics of the MOSFET that require the designer to pay careful attention to the gate drive circuitry. The MOSFET is a voltage controlled device with theoretically no current draw on the gate. Realistically, there is a large non-linear gate charge that must be overcome before the MOSFET is able to turn fully on. In order to realize maximum performance from the MOSFET, large instantaneous currents are required to keep switching times and power losses low. Another characteristic that constrains the design of the gate drive is the typical 20 volt limit on the gate of the MOSFET. The silicon dioxide layer between the gate and the source regions can be easily penetrated, resulting in device failure, if the voltage between the gate and source exceeds $\pm$ 20 volts, even with low current [Application note 937B, International Rectifier].

The excellent performance characteristics of MOSFETs are conditional on the well designed gate drive circuitry. This chapter will aid the designer in modeling these circuits and utilizing MOSFETs to their fullest extent.


VCC
15.02
+
R43
4.64K
3
15.0
R16 98.4K
4
658F
R7
98.4K
X2 COMP
V(2)
HYST
2
5.00
+
out
V(4)
SQUARE
R6
98.1K
GND
V(5)
RAMP
5
9.36E-028
R17 21.3K
C10
330P

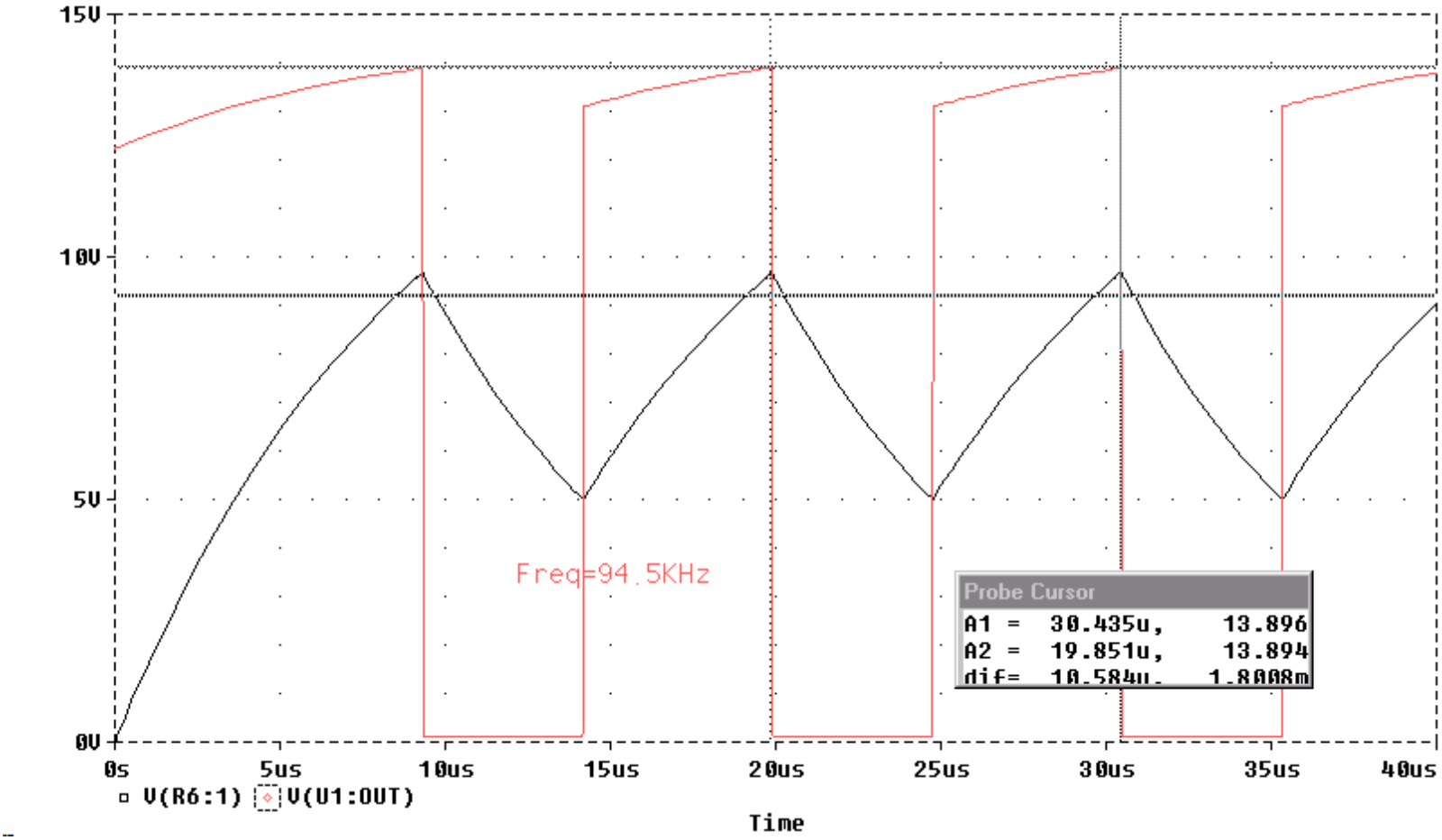


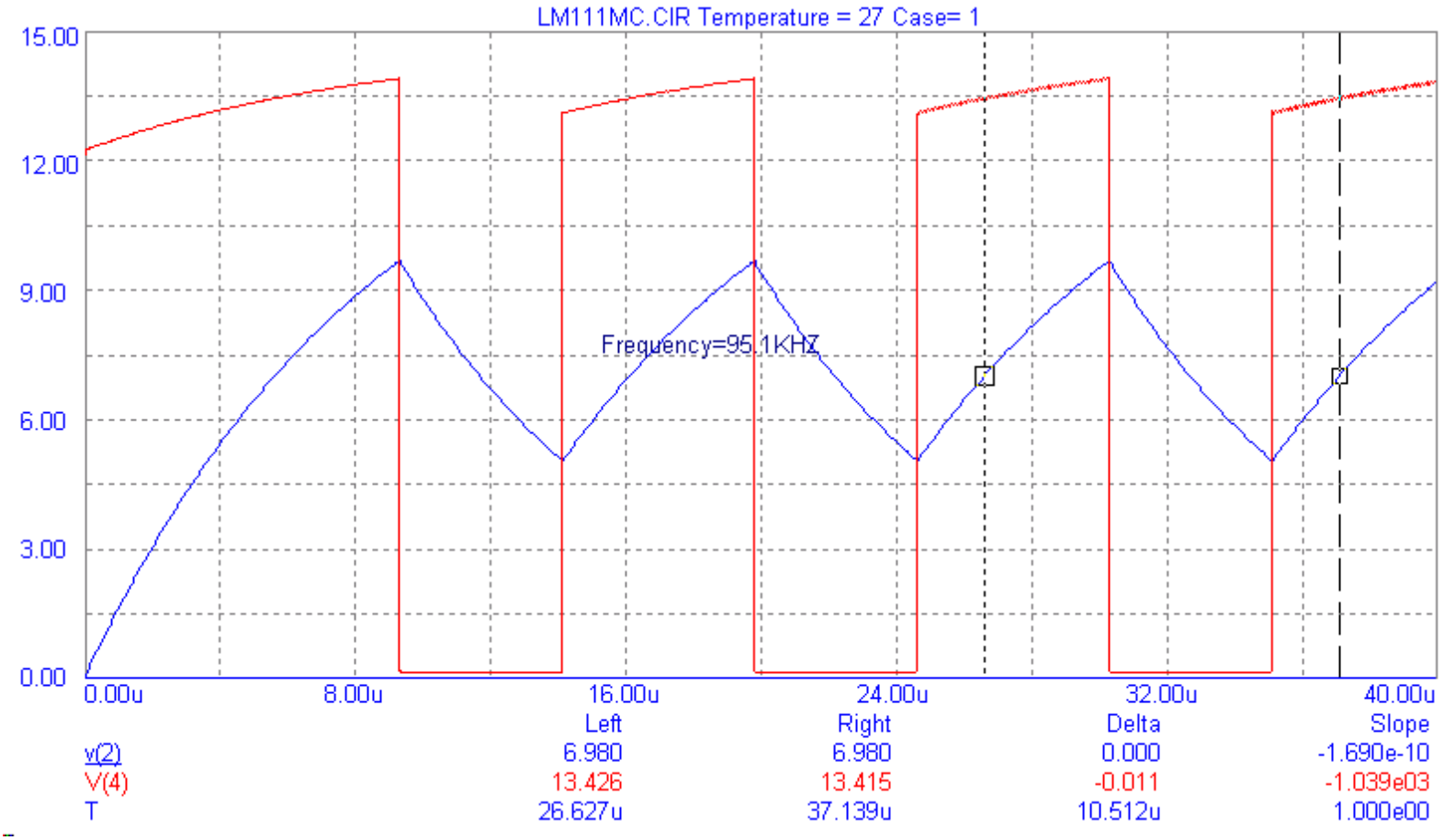

Tek Run: 20MS/s Average Trig'd
Ch2 Freq
90.98kHz
Ch1 Pk-Pk
4.897 V
Ch2 +Duty
54%
Ch1 2 V Ch2 500mV M 2.5µs Ch2 ∫ 720mV
15 Feb 1997
10:34:34



Freq=95.2KHz

Δx = 10.50U Δy = 0


15V
10V
5V
0V
Freq=94.5KHz
Probe Cursor
A1 = 30.435u, 13.896
A2 = 19.851u, 13.894
dif= 10.584u, 1.8888m
0s
5us
10us
15us
20us
25us
30us
35us
40us
V(R6:1)
V(U1:OUT)
Time


LM111MC.CIR Temperature = 27 Case= 1
15.00
12.00
9.00
6.00
3.00
0.00
Frequency=95.1KHZ
0.00u
8.00u
16.00u
24.00u
32.00u
40.00u
Left
Right
Delta
Slope
v(2)
6.980
6.980
0.000
-1.690e-10
V(4)
13.426
13.415
-0.011
-1.039e03
T
26.627u
37.139u
10.512u
1.000e00

#42: UC1846 50 % duty cycle gate drive circuit

This circuit was used in Chapter 12 as part of a high voltage, high current doubler. This circuit can provide a fixed frequency, fixed 50 % duty cycle square wave capable of driving the gate of a power Mosfet.

This circuit is shown in figure 42-1. The circuit is powered from a 15 volt supply connected to Vin and Vc (pins 15 and 13). A bypass capacitor is applied across the power of the IC to help minimize noise effects. The frequency of the output is set by resistor R5 and capacitor C3.

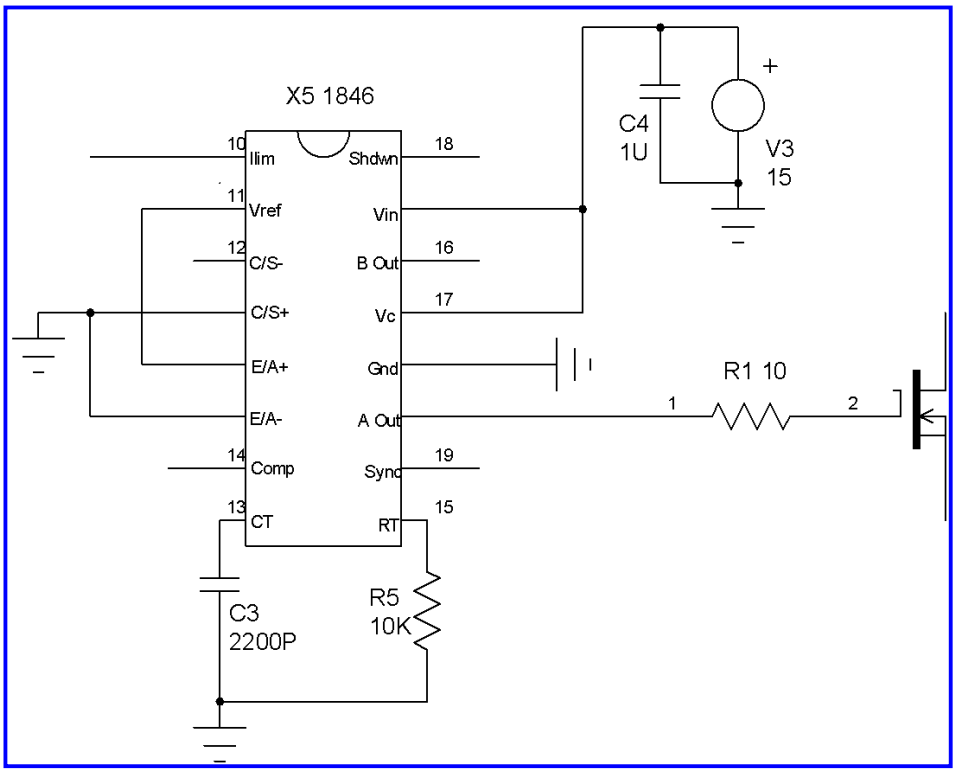


Figure 42-1: Schematic of UC1846 fixed duty cycle gate drive circuit

The frequency is fixed at 50 Khz, with a 50 % duty cycle. By tying the non-inverting terminal of the error amplifier to the reference voltage (5.1 volts) and tying the inverting terminal to ground, the oscillator controls the pulse termination. The output signal appears at A OUT (pin 11).

Our equivalent SPICE model of this circuit is shown in Figure 42-2. A 100 Meg resistor (R4) has been added from the inverting terminal of the current sense pin to ground in order to help convergence and prevent "singular matrix" errors.

- SPICE tip: The "trick" described above is a good way to prevent "singular matrix" errors. "Singular matrix" errors usually occur because the node does not have a direct path to ground. By adding the 100 Meg resistor, this node has a direct path to ground and does not effect the operation of the circuit.

- SPICE tip: In order to force convergence in this circuit, the UIC statement MUST be included in the .TRAN simulation. The SPICE engine has a difficult time determining the steady state operating point of the Flip-Flops internal to the UC1846. Also, the ABSTOL OPTIONS parameter has been changed from 1p to 1u to aid convergence.

A voltage and resistance (V2 and R3) was added to the drain of the Mosfet so the gate voltage characteristics will be accurate while the Mosfet is biased.

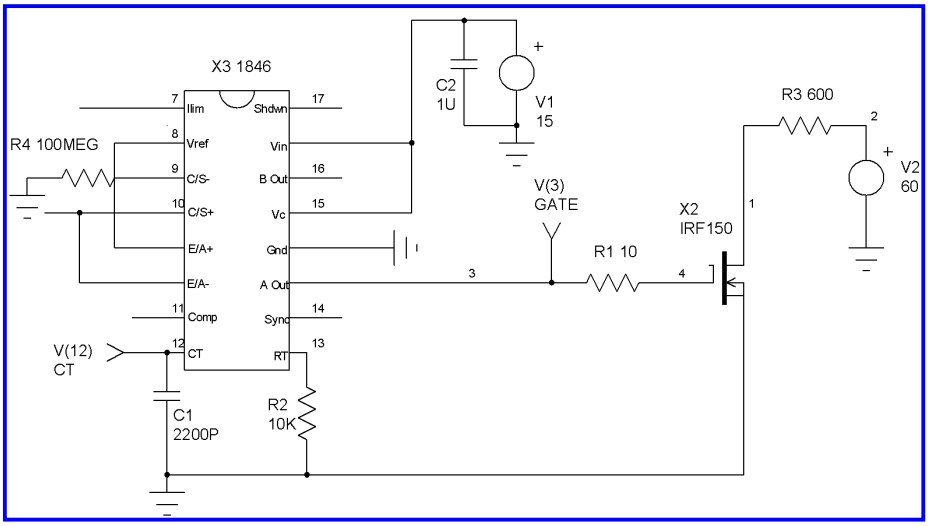


Figure 42-2: SPICE equivalent Schematic of UC1846 Mosfet Drive circuit

The Breadboard was constructed and two waveforms were measured. The waveforms are shown in Figure 42-3, the top trace is the output pulse, the bottom trace is the voltage on the Ct pin (pin 8).

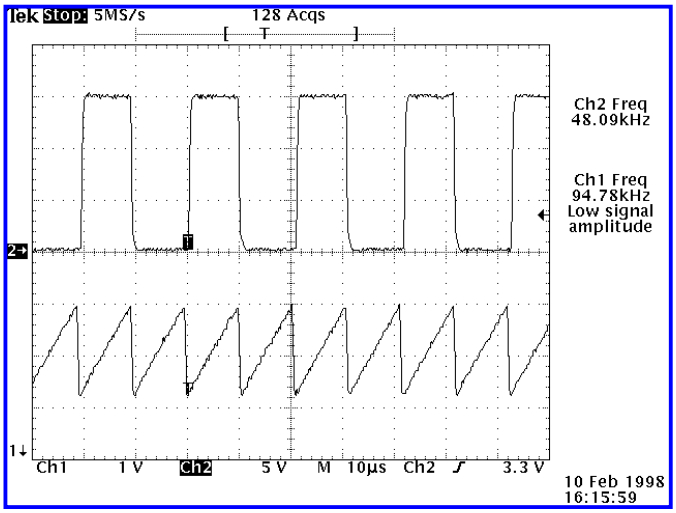


Figure 42-3: Breadboard waveforms

This circuit was also constructed in IsSpice. The resulting waveforms are shown in Figure 42-4. The top waveform in Figure 42-4 had a frequency of 44.05 Khz and the bottom waveform had a frequency of 87.86 Khz.

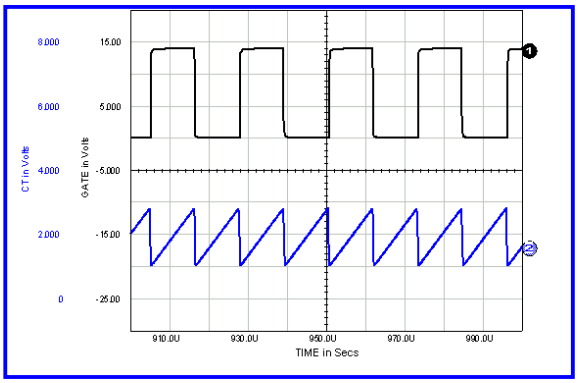


Figure 42-4: IsSpice waveform results

- Breadboard tip: You may notice the gate resistor (in this example, 10 ohms) is present in most of the Mosfet gate drives in circuits today. This resistor damps spurious oscillations that can occur in the gate voltage of power Mosfets. The value of this resistor is a trade off between reduced switching losses and suppressing these spurious oscillations. Another resistor that is usually included is a 10 Kohm resistor from the gate of the Mosfet to ground. Gate charge can be large on some power Mosfets, possibly causing the Mosfet to remain ON even if the gate drive has been removed. This 10 Kohm resistor to ground allows any excess charge to dissipate safely from the gate in the event of this occurrence. In this sample circuit, the low state of the UC1846 is a low impedance, which allows us to exclude this resistor.

The UC1846 model is not available in either the evaluation version of Pspice, nor Microcap.

Run Time Summary		
IsSpice v 7.6	PsPice v 6.3	Micro-Cap V v2
347.666 Sec	xxx Sec	xxx Sec

Advantages: Simple, high frequency capability, high output current, complementary outputs
Disadvantages: none

Filenames: 1846 (IsSpice)

References

1990 Linear Databook, Linear Technology.

1990 Linear Applications Handbook Volume I, Linear Technology.

Hexfet Power MOSFET Designer's Manual. International Rectifier. 1993.

Parker, Sybil, ed. 1984. Concise Encyclopedia of Science and Technology. New York: McGraw Hill

Van Valkenburg, M.E. 1982. Analog Filter Design. New York: Harcort Brace Jovanovich College Publishers.

#43: 555 Pulse shaped MOSFET driver

Proving once again the versatility of the 555 IC, this circuit utilizes the ability of the 555 to provide varying duty cycle shaped waveforms for MOSFETS. In certain applications of MOSFETs, when the device is turned on, current transfers from a freewheeling diode into the MOSFET. Parasitic inductances and high switching speeds can cause reverse recovery currents in the freewheeling diode that are high enough to destroy the device [AN-937B, International Rectifier]. For this reason, it is sometimes practical to delay the turn on edge of the MOSFET in order to limit the reverse recovery current in the freewheeling diode.

This circuit is shown in figure 43-1. The input waveform is generated at voltage source V1. The reset is pulled high through a 4.7 Kohm resistor and the trigger and threshold pins are tied together. This configuration causes the 555 to act as an inverter. The totem pole arrangement of the 2N2222A and 2N2907A transistors provides good current capability to drive the gate of the Mosfet. The gate of the Mosfet is modeled in this circuit by the 1000 pF capacitor. A bypass capacitor is applied across the power of the IC to help minimize noise effects (always a good idea when using switching IC's).

When the input transitions low, the output of the 555 transitions high. Capacitor C1 begins to charge through resistor R1. This action provides for the delayed pulse. On turn off, the voltage is discharged through diode D3 to ground, allowing for a fast switching time (which minimizes switching losses).

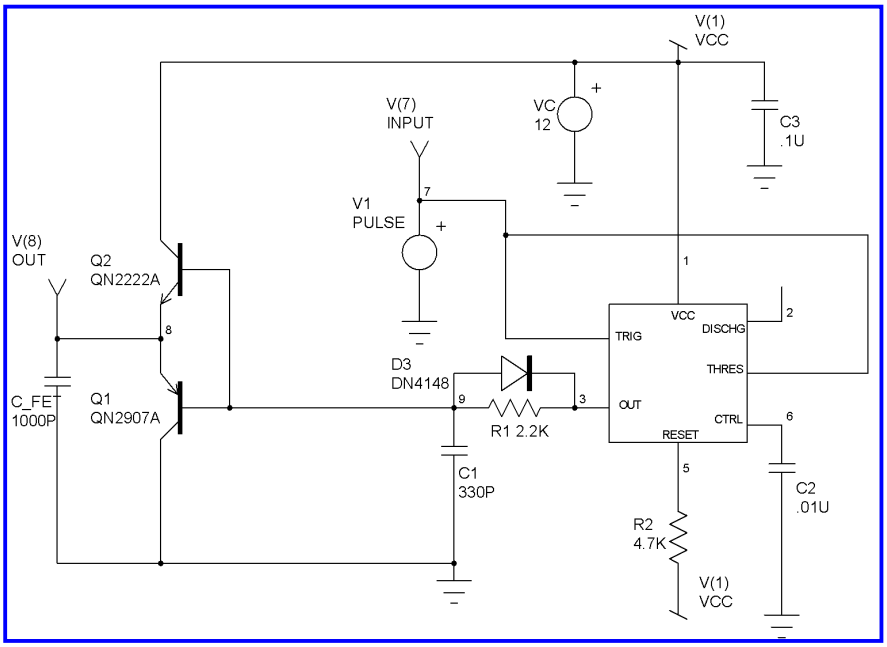


Figure 43-1: Schematic of pulse shaping gate drive circuit

- Breadboard tip: If there is no input signal to this circuit, the default output is high. Also note that this circuit operates as an inverter.

- SPICE tip: In order to assist convergence in this circuit, the UIC statement was included in the .TRAN simulation. This statement helps in circuits where a steady state operating point may not exist or is difficult for SPICE to determine.

The Breadboard was constructed and two waveforms were measured. The waveforms are shown in Figure 43-2, the top trace is the output gate drive pulse, the bottom trace is the input voltage to the 555.

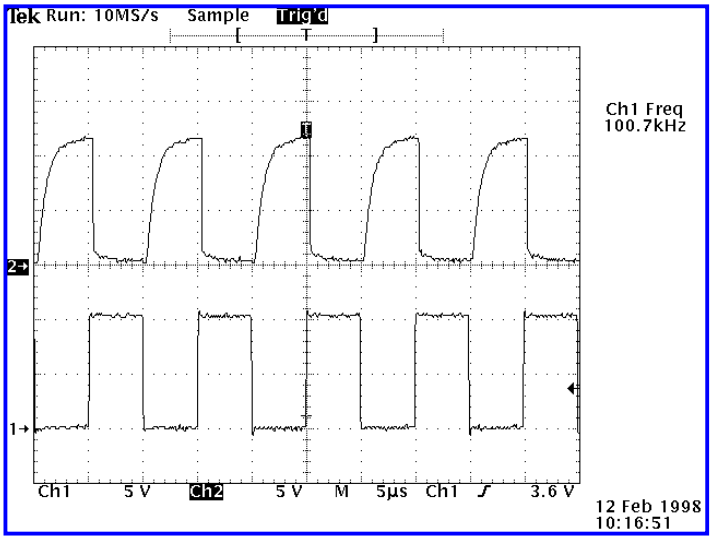


Figure 43-2: Breadboard waveforms

This circuit was also constructed in IsSpice, Pspice, and Microcap. The resulting waveforms are shown in Figure 43-3 through 43-5.

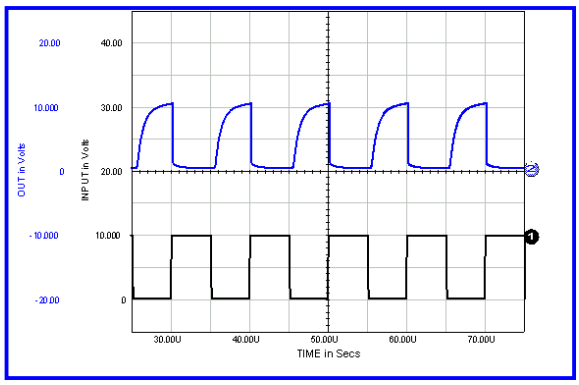


Figure 43-3: IsSpice waveform results

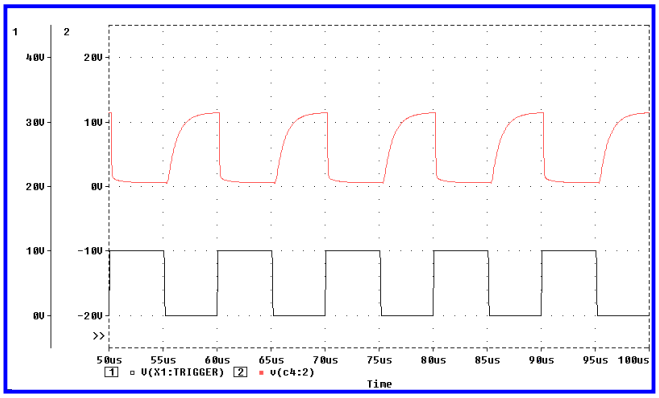


Figure 43-4: Pspice waveform results

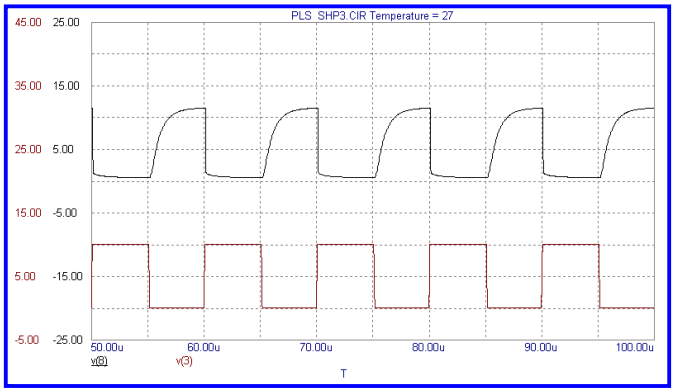


Figure 43-5: Microcap waveform results

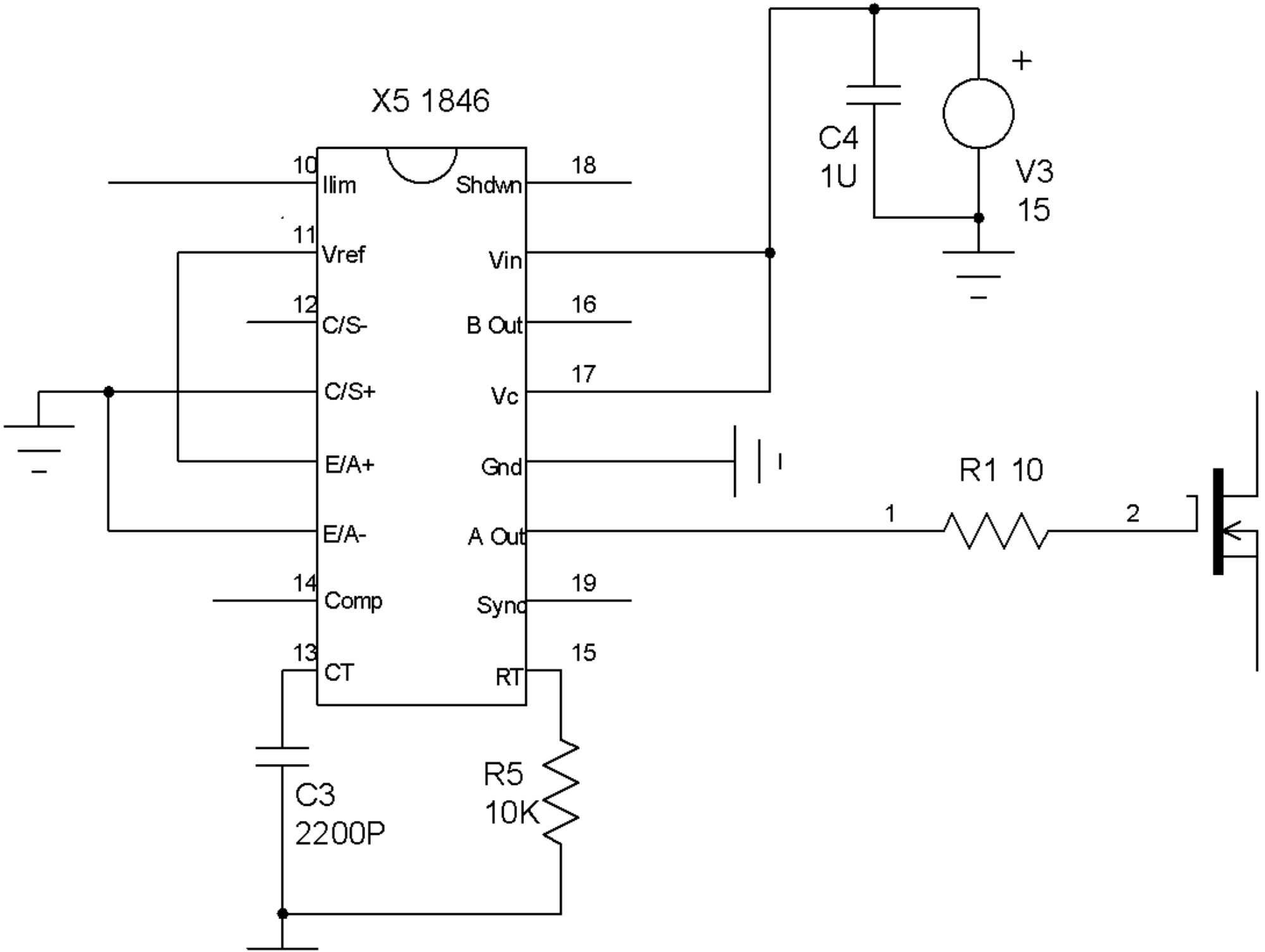
- SPICE tip: In order to run this schematic on the Pspice evaluation version, the DISCH pin of the 555 model needed to be connected to a .01 uF capacitor. Leaving this pin floating produced an error. When this capacitor was added, the simulation results matched the other two simulators.

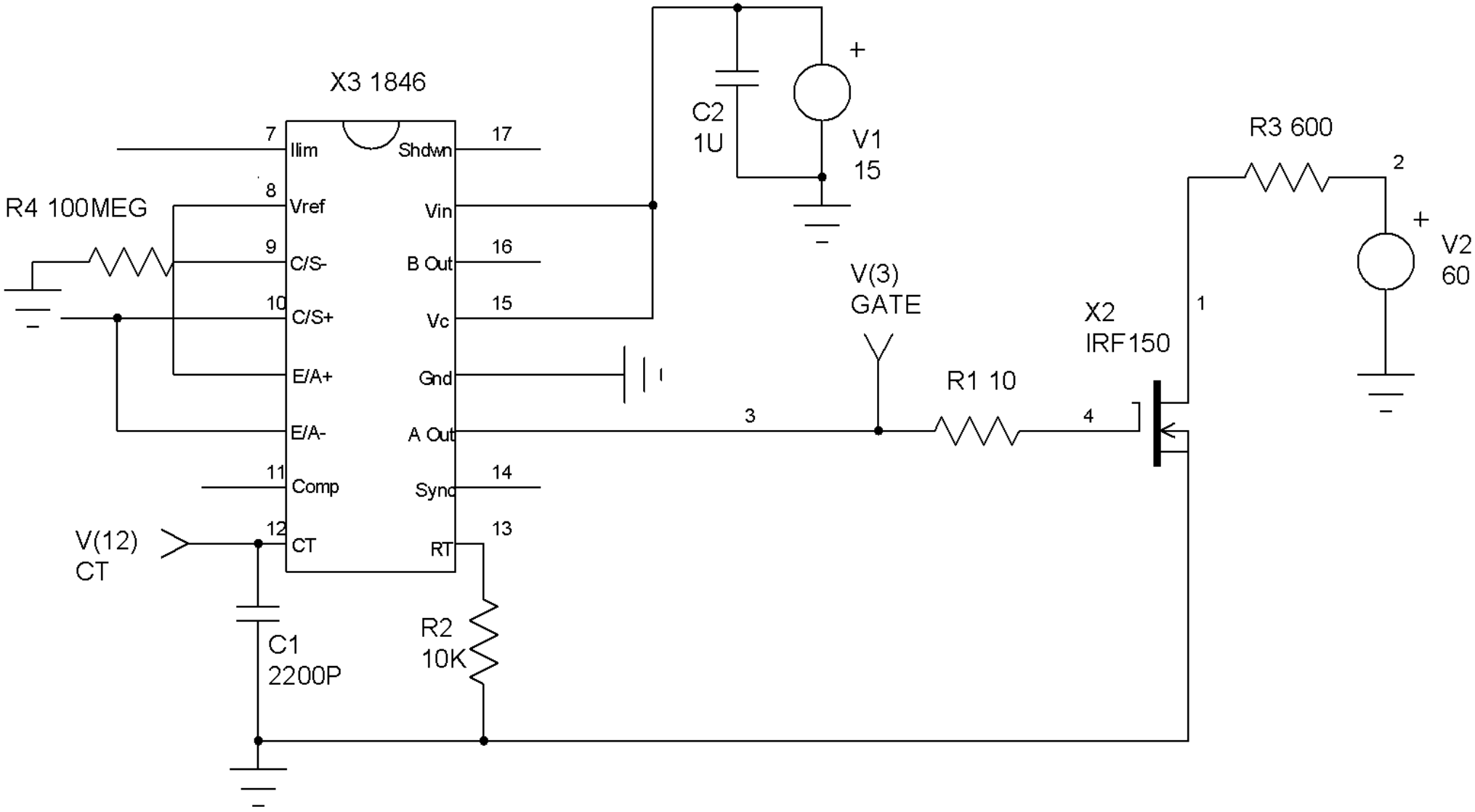
Generally, a SPICE primitive capacitor is not the best way to model the non-linear capacitance of a MOSFET. The capacitance of the gate of the MOSFET is dependent on the gate to source voltage, and to a lesser extent, the drain to source voltage. However, the fixed capacitance used in this simulation is adequate for our purposes.

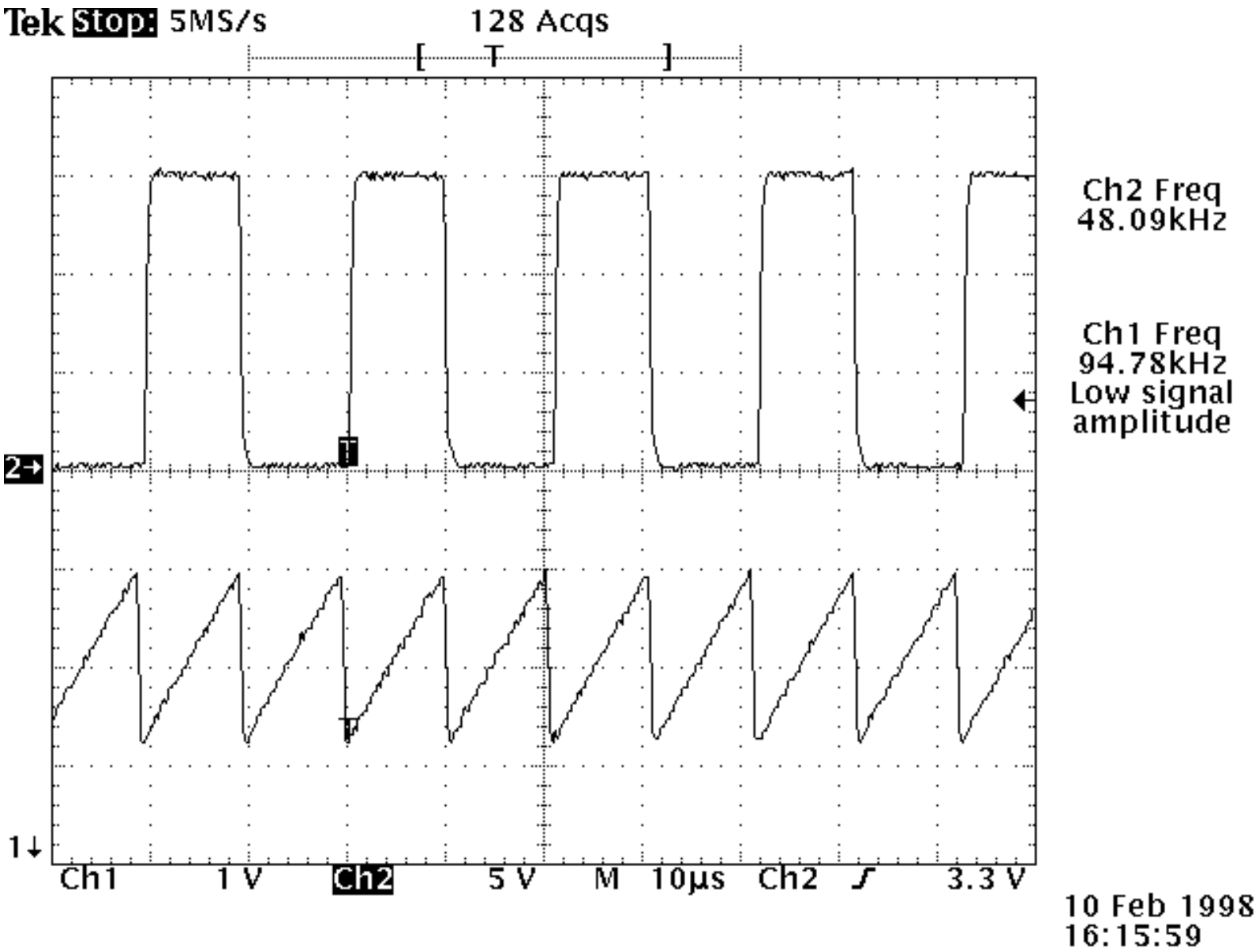
Run Time Summary		
IsSpice v 7.6	PsPice v 6.3	Micro-Cap V v2
40.85 Sec	11.45 Sec	70.528 Sec
Advantages: good drive current capability, reduced turn on switch transient currents		
Disadvantages: Higher parts count than other solutions. Slower turn on creates higher power dissipation in the MOSFET.		

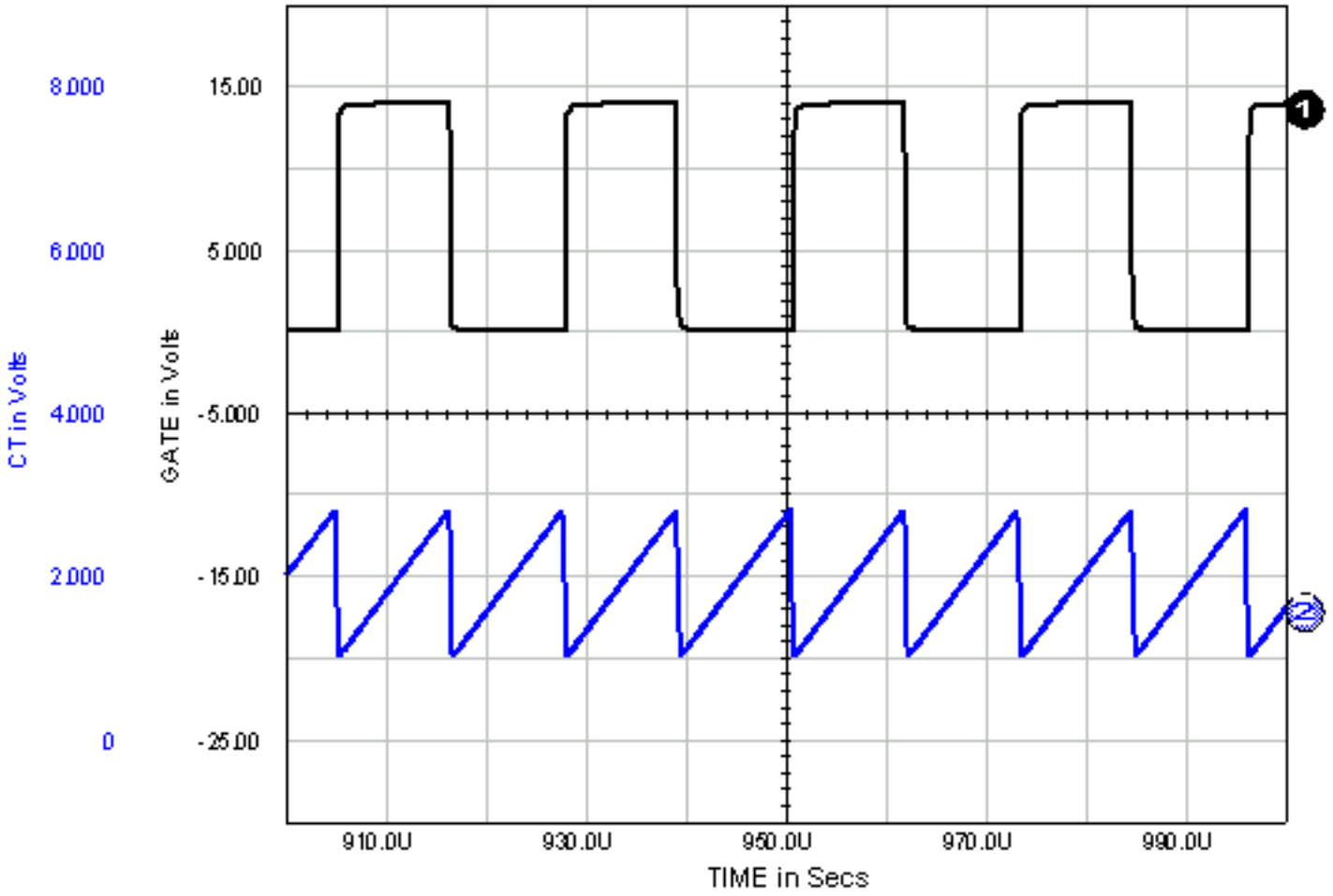
Filenames: puls_sh (IsSpice) pls_shp2 (Pspice) pls_shp3 (Microcap)

555 Pulse shaped MOSFET driver


X5 1846
10
Ilim
11
Vref
12
C/S-
C/S+
E/A+
E/A-
14
Comp
13
CT
18
Shdwn
Vin
16
B Out
17
Vc
Gnd
A Out
19
Sync
15
RT
C4
1U
+
V3
15
I
R1 10
1
2
C3
2200P
R5
10K


X3 1846
7
Ilim
8
Vref
9
C/S-
10
C/S+
E/A+
E/A-
11
Comp
12
CT
Shdwn
17
Vin
B Out
16
Vc
15
Gnd
A Out
3
Sync
14
RT
13
R4 100MEG
V(12)
CT
C1
2200P
R2
10K
C2
1U
V1
15
V(3)
GATE
R1 10
X2
IRF150
1
4
R3 600
2
V2
60


Tek Stop: 5MS/s
128 Acqs
Ch2 Freq
48.09kHz
Ch1 Freq
94.78kHz
Low signal
amplitude
2→
1↓
Ch1 1 V
Ch2 5 V
M 10µs
Ch2 ∫ 3.3 V
10 Feb 1998
16:15:59


8.000
6.000
4.000
2.000
0
CT in Volts
15.00
5.000
-5.000
-15.00
-25.00
GATE in Volts
910.0U
930.0U
950.0U
970.0U
990.0U
TIME in Secs
1
2

#44: Zero to 100% Duty Cycle Driver

When the requirements for isolated gate drive circuits require operation at nearly full duty cycle or nearly zero duty cycle, these circuits can be difficult to design. The transformer that provides isolation can easily saturate at full duty cycles. The circuit featured here uses a unique idea in order to circumvent this difficulty.

This circuit is shown in figure 44-1. The input waveform is generated at voltage source VIN. The center tapped transformer X2 saturates at turn on, which provides turn on charge to the output MOSFET through diode D2 and resistor R2. When the input waveform turns off, D2 is reversed biased and turn off charge is provided to MOSFET X3, allowing for a fast turn off. Capacitor C1 provides the energy bank of the circuit. The transformer is wound on a 41005 toroid using F material. There are three turns for each winding (this example used 26 AWG trifilar twisted). The MOSFET load being driven is approximated as a 2000 pF capacitor.

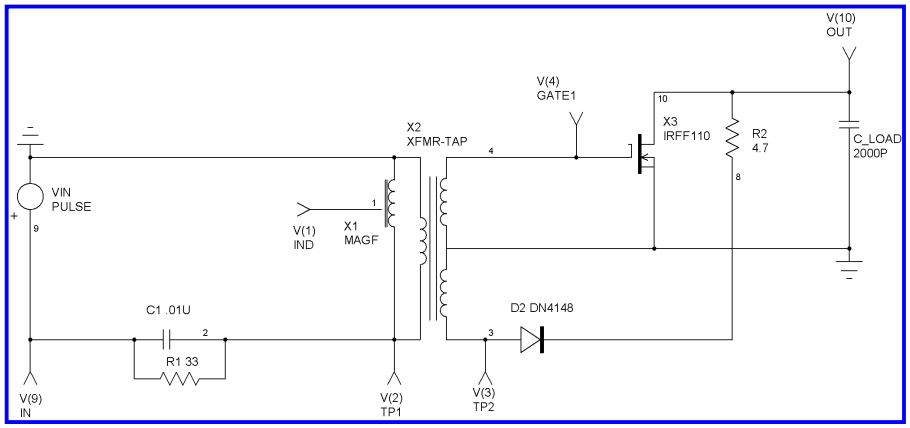


Figure 44-1: Schematic of zero to 100% duty cycle gate drive circuit

- Breadboard tip: If operating this circuit at wide duty cycles, the 33 ohm resistor will dissipate high power. Choose an adequately sized resistor.

- SPICE tip: To model the transformer, an ideal center tapped transformer is combined with a non-linear core model for the F material. As this circuit counts on the saturation of the core, a SPICE primitive inductor will not work. By adding this non-linear core model across the input of the center tapped transformer, the

magnetizing inductance and saturation characteristics of the core is realized.

In order to fully test the capabilities of this circuit, the input pulse was varied in duty cycle from 5 % to 95 %. The voltage source VIN used the following two statements:

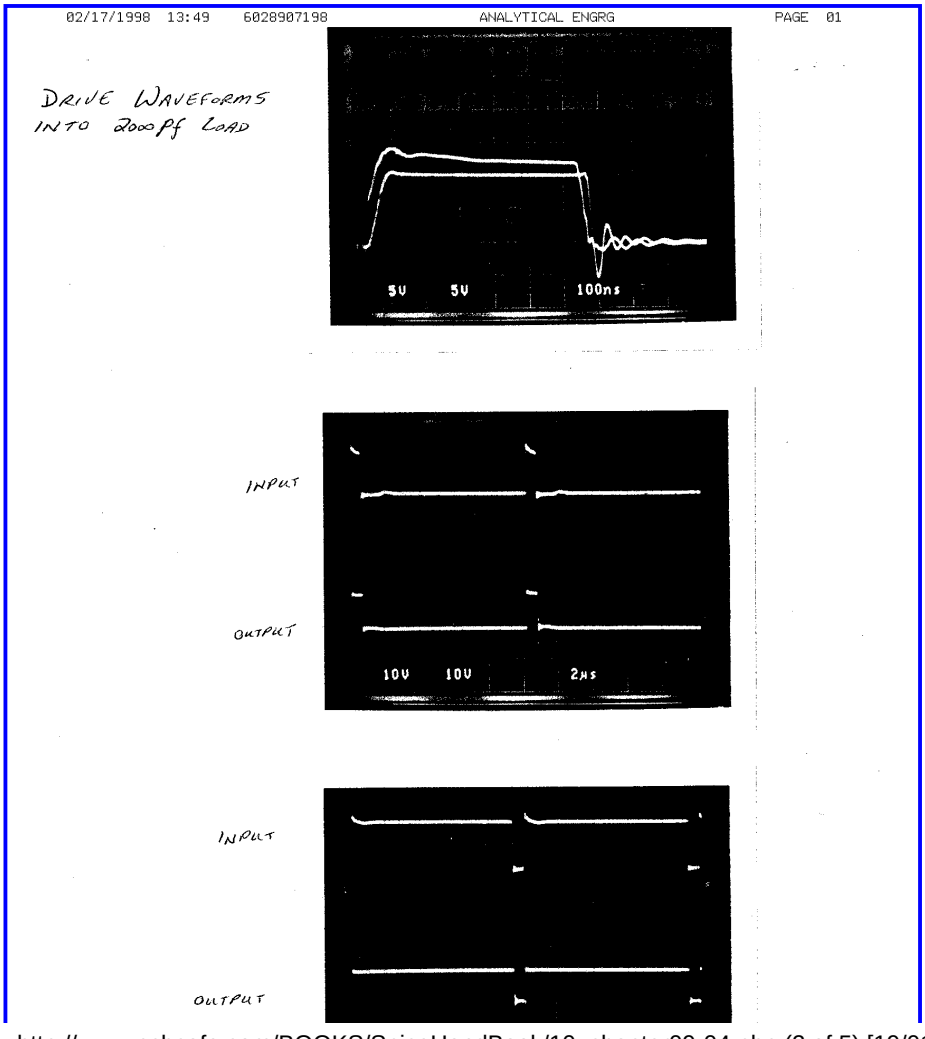
```
PULSE 0 15 0 20N 20N .5U 10U ; 5% duty cycle

PULSE 0 15 0 20N 20N 9.5U 10U ; 95% duty cycle
```

Fast switching circuits like this one can cause simulation problems. Discontinuities can create "Time Step Too Small" errors. In order to aid in convergence, the following statement was added to each of the simulators.

```
.OPTIONS
ITL4=100 ;
```

This increases the number of transient iterations at each time point.

Figure 44-2 shows the waveform results of the breadboard at three different test conditions. The top picture shows the input pulse and the output pulse overlapped so the delay and turn off ring can be examined. The middle picture shows the input (top) and output (bottom) waveforms when the duty cycle is 5 %. The bottom picture shows the input (top) and output (bottom) waveforms when the duty cycle is 95 %.



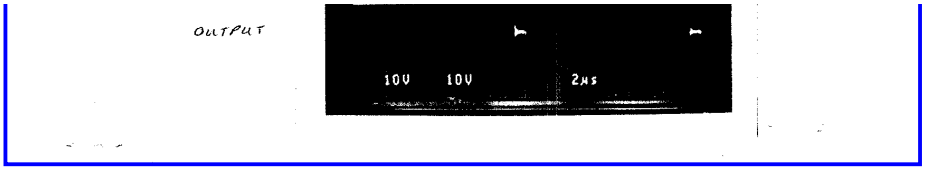
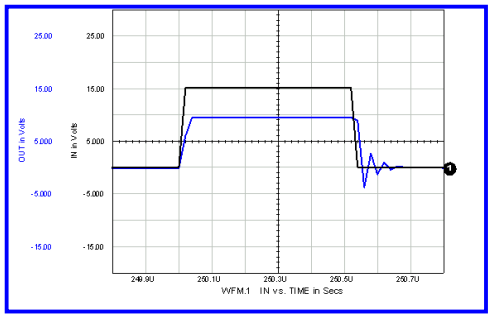
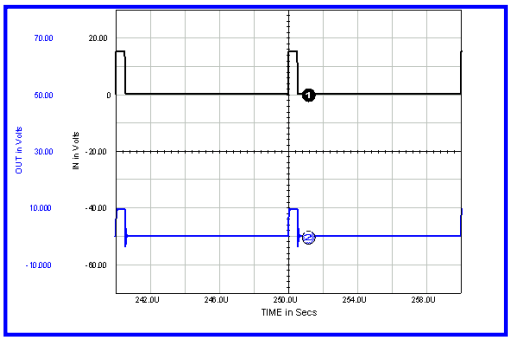


Figure 44-2: Breadboard waveforms

This circuit was also constructed in IsSpice, Pspice, and Microcap. The resulting waveforms are shown in Figure 44-3 through 44-5.





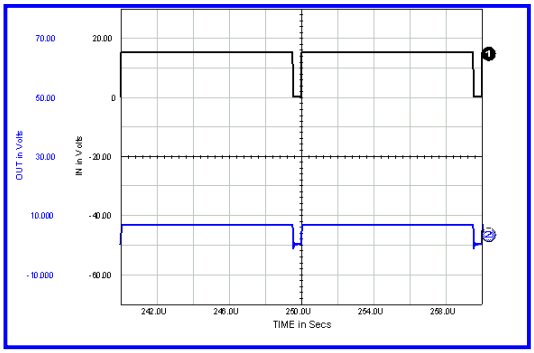
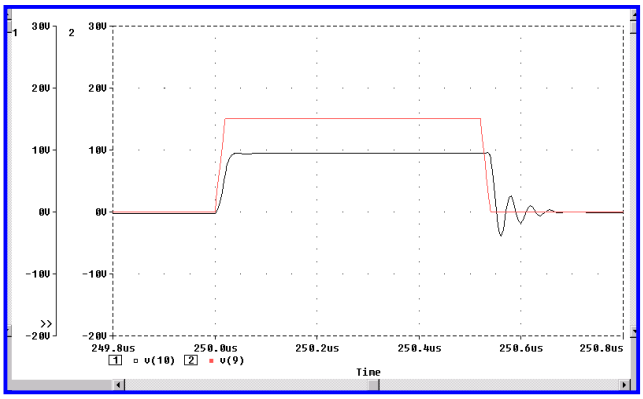
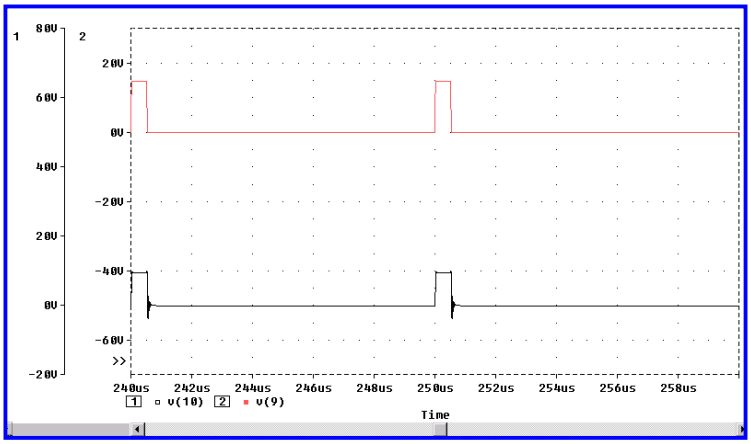


Figure 44-3: IsSpice correlation waveform results





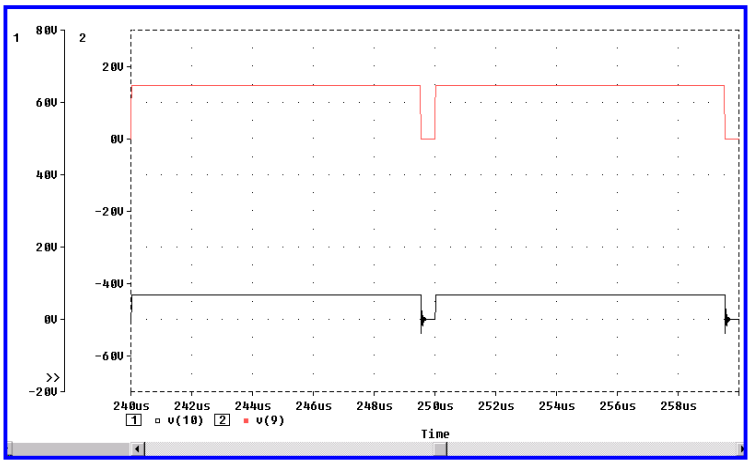
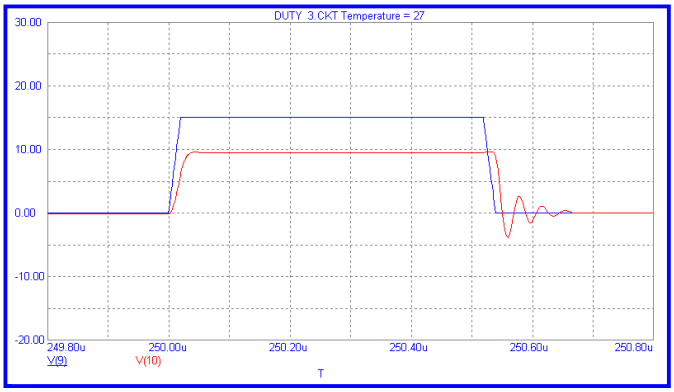
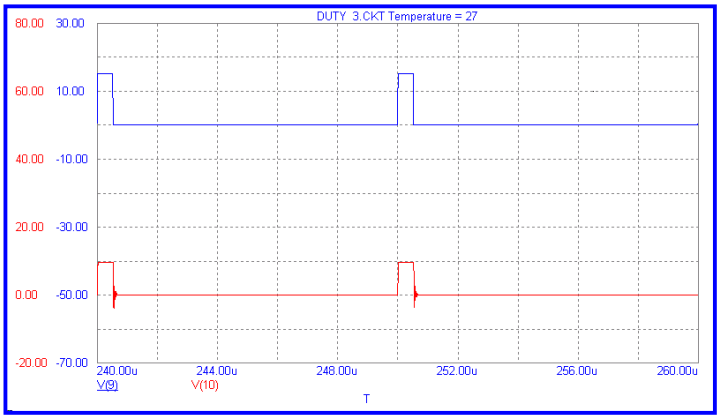


Figure 44-4: Pspice waveform results





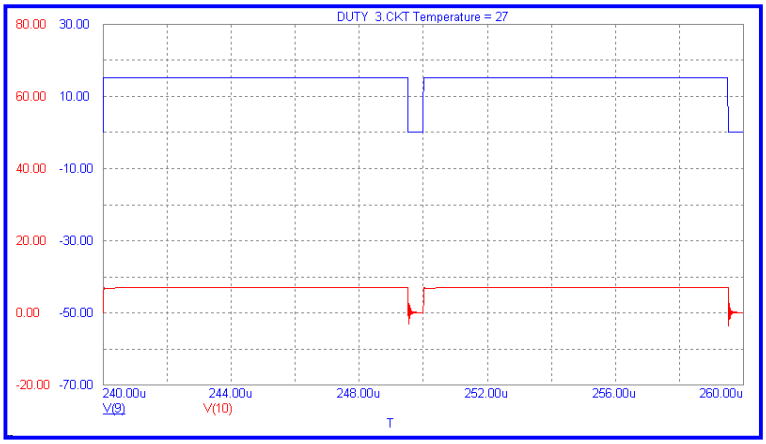


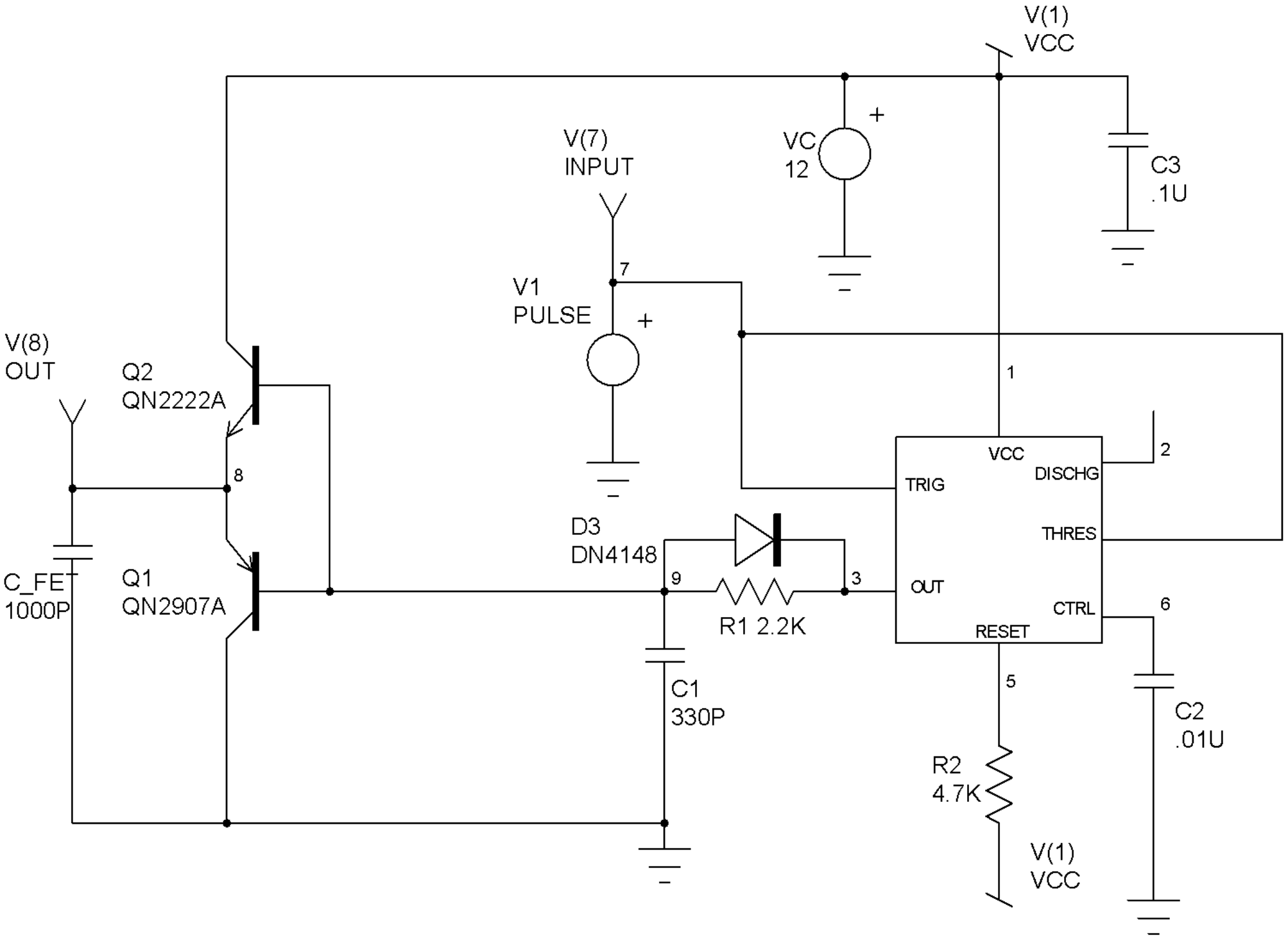
Figure 44-5: Microcap waveform results

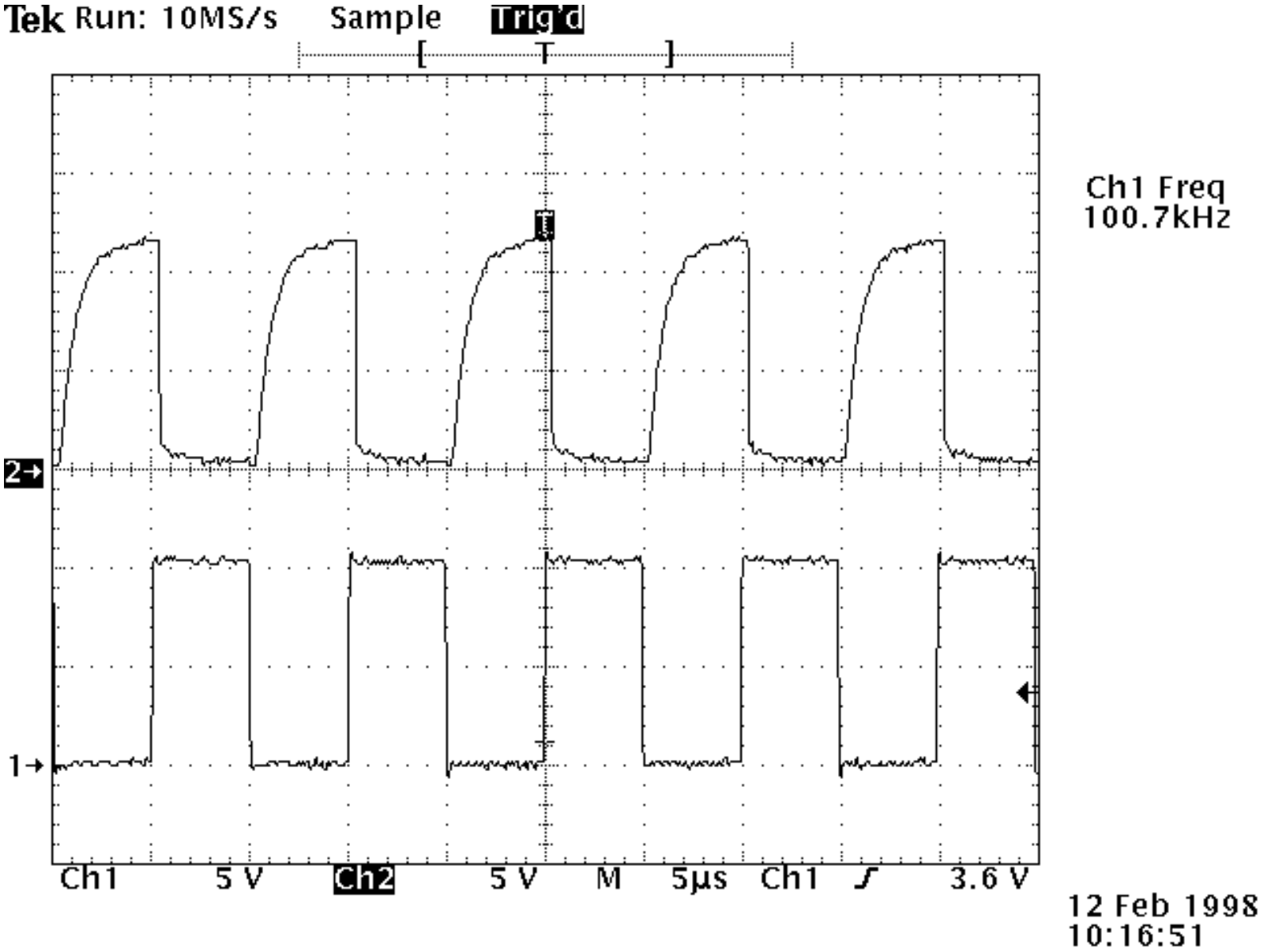
Generally, a SPICE primitive capacitor is not the best way to model the non-linear capacitance of a MOSFET. The capacitance of the gate of the MOSFET is dependent on the gate to source voltage, and to a lesser extent, the drain to source voltage. However, the fixed capacitance used in this simulation is adequate for our purposes.

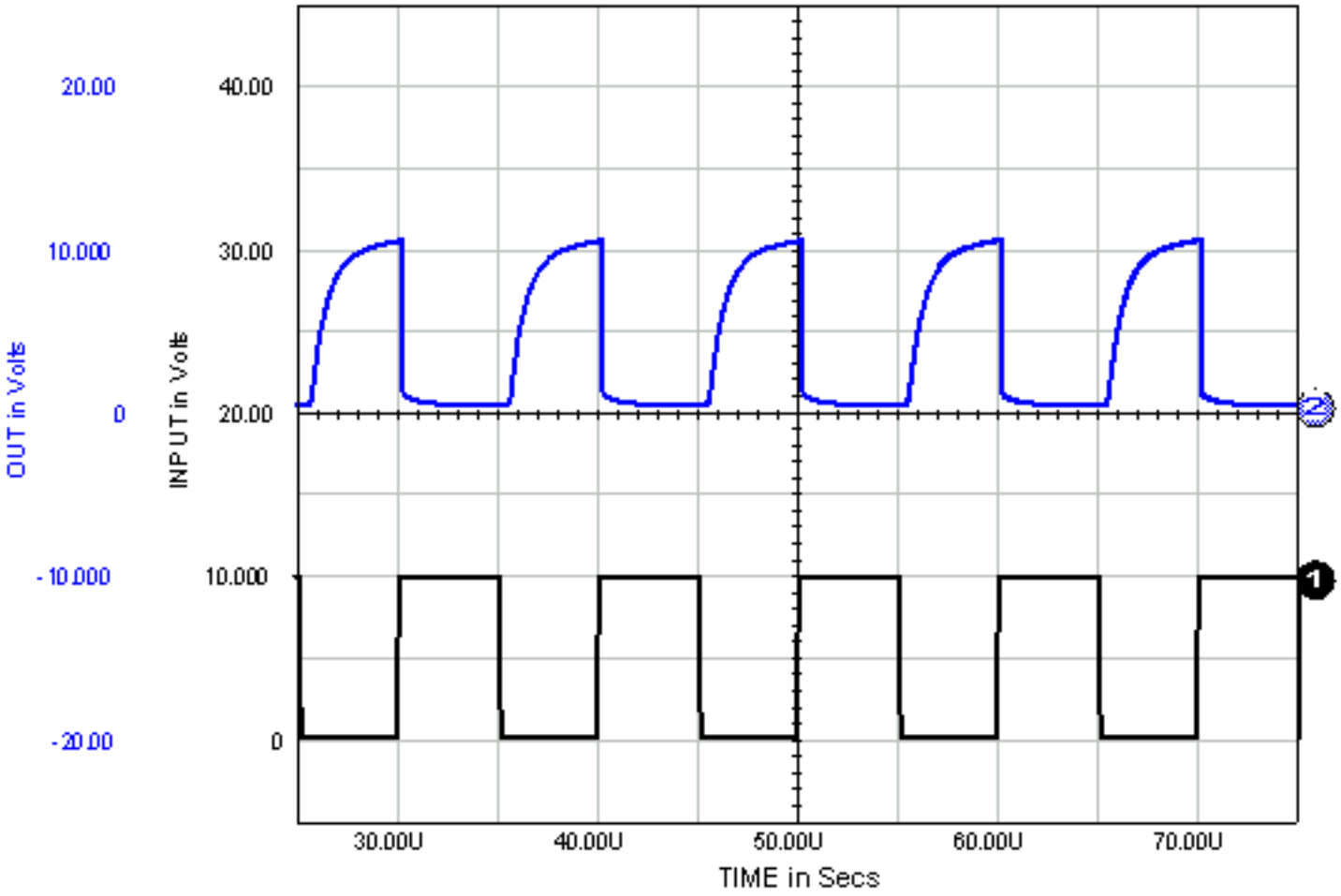
- Microcap tip: While attempting to run this simulation in Microcap the following error was generated "Floating point 'Pow (0,-1.1376) Domain Error'". This was traced to the use of the SPICE compatible VALUE statement in an E element. The value statement is used to model equations dependent on other nodes or currents. The statement in question used the form X ^ - Y. This was acceptable to IsSpice and Pspice, but not to Microcap. This statement was rewritten in the equivalent form 1 / (X ^ Y) which was accepted without error.

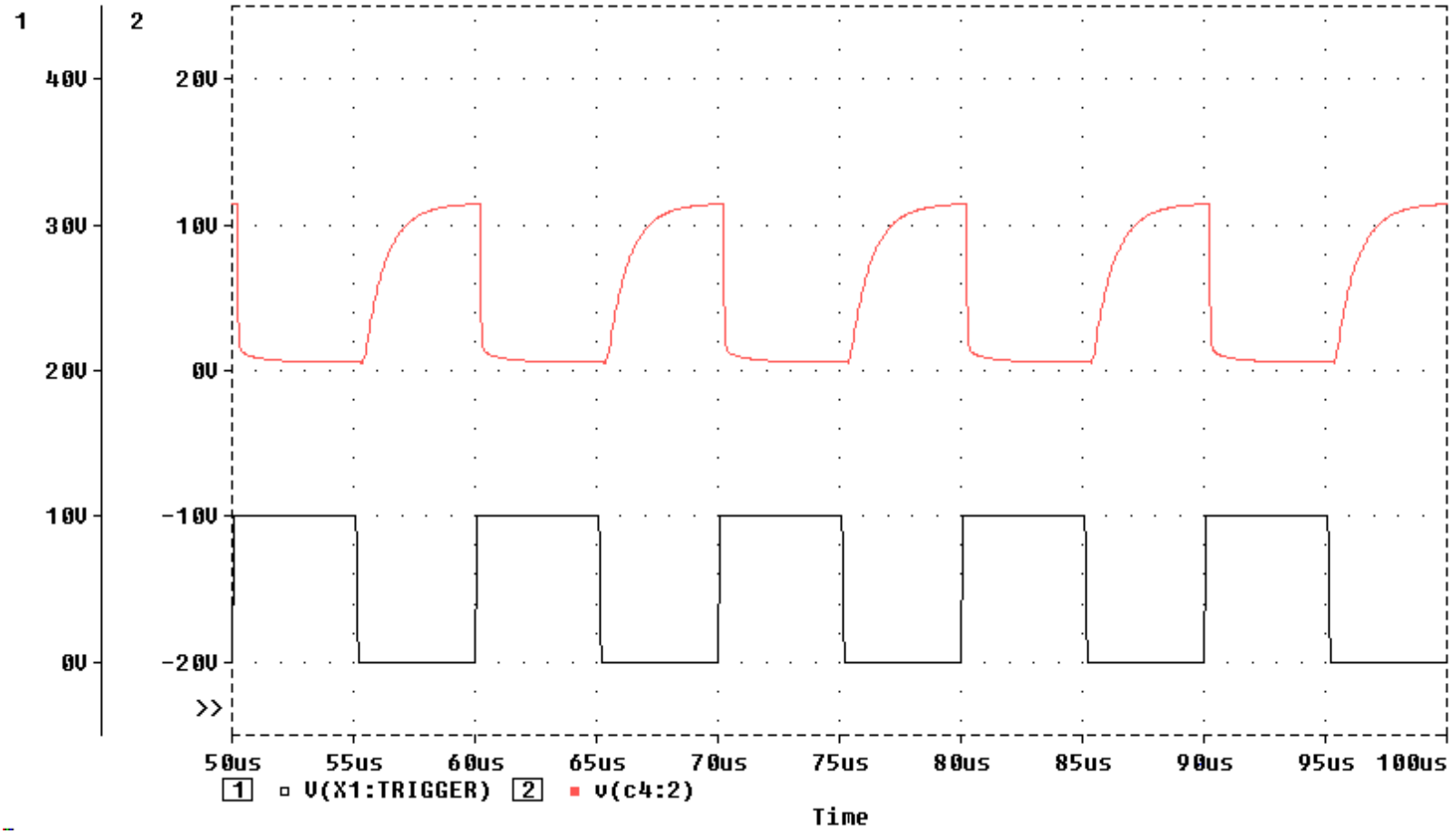
Run Time Summary		
IsSpice v 7.6	Pspice v 6.3	Micro-Cap V v2
61.633 Sec	58.42 Sec	184.89 Sec
Advantages: Isolated Driver, nearly infinite duty cycle range, very low delay, not frequency limited		
Disadvantages: high power dissipation in the 33 ohm resistor at wide duty cycles, ringing on trailing edge		

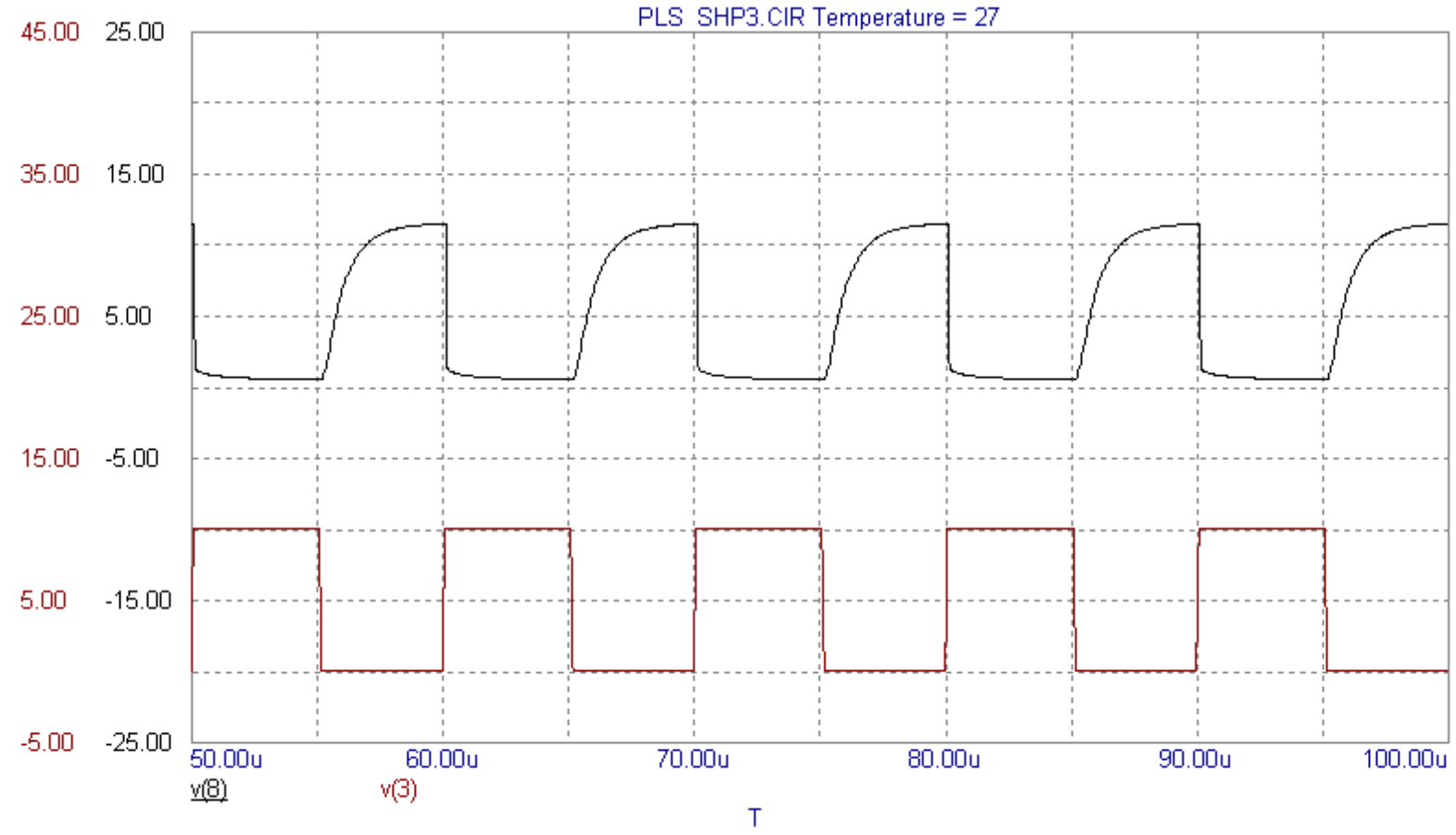
Filenames: ful_duty (IsSpice) duty2 (Pspice) duty_3 (Microcap)


V(1)
VCC
VC
12
+
C3
.1U
V(7)
INPUT
V1
PULSE
+
7
V(8)
OUT
Q2
QN2222A
8
C_FE
1000P
Q1
QN2907A
D3
DN4148
9
3
R1 2.2K
C1
330P
1
VCC
DISCHG
2
TRIG
THRES
OUT
CTRL
6
RESET
5
R2
4.7K
V(1)
VCC
C2
.01U


Tek Run: 10MS/s Sample Trig'd
Ch1 Freq
100.7kHz
2→
1→
Ch1 5 V Ch2 5 V M 5µs Ch1 ƒ 3.6 V
12 Feb 1998
10:16:51


20.00
10.000
0
-10.000
-20.00
OUT in Volts
40.00
30.00
20.00
10.000
0
INPUT in Volts
30.00U
40.00U
50.00U
60.00U
70.00U
TIME in Secs
2
1


1
2
40V
30V
20V
10V
0V
20V
10V
0V
-10V
-20V
>>
50us
55us
60us
65us
70us
75us
80us
85us
90us
95us
100us
1 V(X1:TRIGGER) 2 v(c4:2)
Time


PLS SHP3.CIR Temperature = 27
45.00
25.00
35.00
15.00
25.00
5.00
15.00
-5.00
5.00
-15.00
-5.00
-25.00
50.00u
60.00u
70.00u
80.00u
90.00u
100.00u
v(8)
v(3)
T

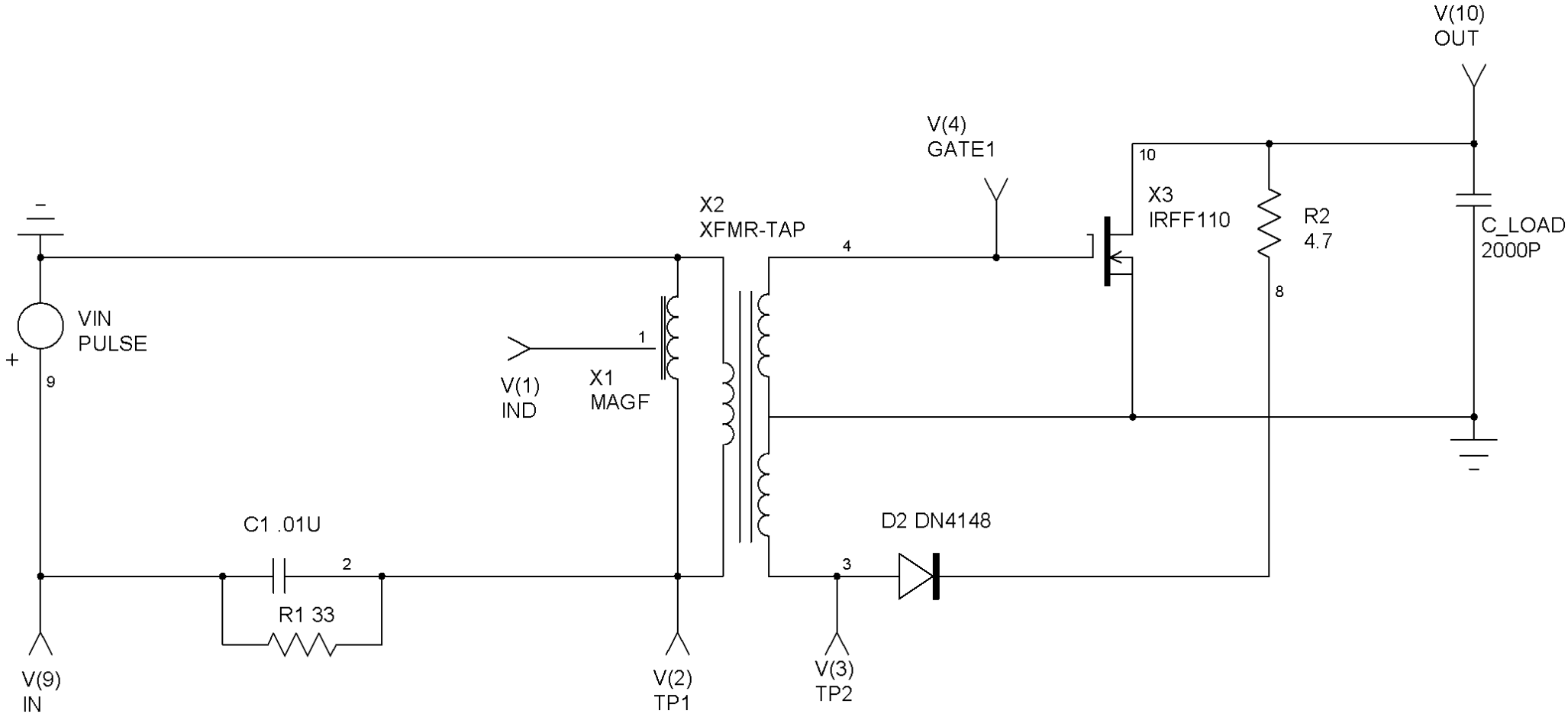
10
Voltage Multiplier Circuits

As more and more electrical designs utilize the benefits in performance, cost, and size of Integrated Circuits, demand for DC power in the system has been increasing.

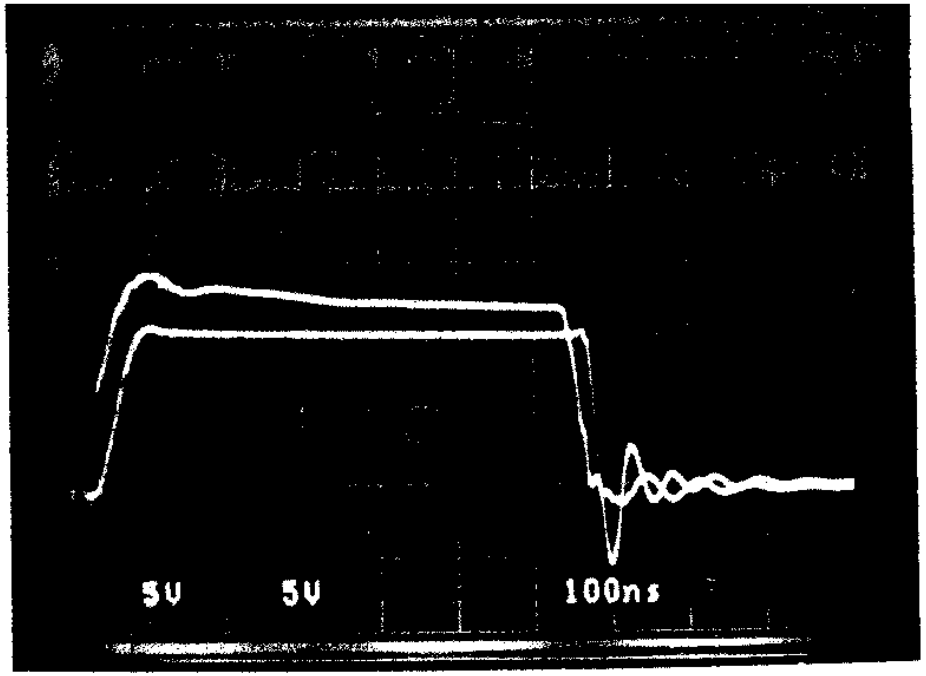
Unfortunately, sometimes the only power input of these circuits is an AC waveform, with a spare winding from a transformer that must power the housekeeping supplies of the system. Other times, the designer is trying to avoid adding a DC housekeeping power supply to the system, which while adding power capability to the IC's, also adds complexity and cost.

One simple and inexpensive solution to powering Integrated Circuits and other circuits that require DC levels, are the voltage multiplier circuits.

Using these circuits requires few parts, and provides a good design choice when circumstances permit their use. The information in this chapter will aid the designer in predicting the performance of these circuits and maximizing their capability and usefulness in the system.

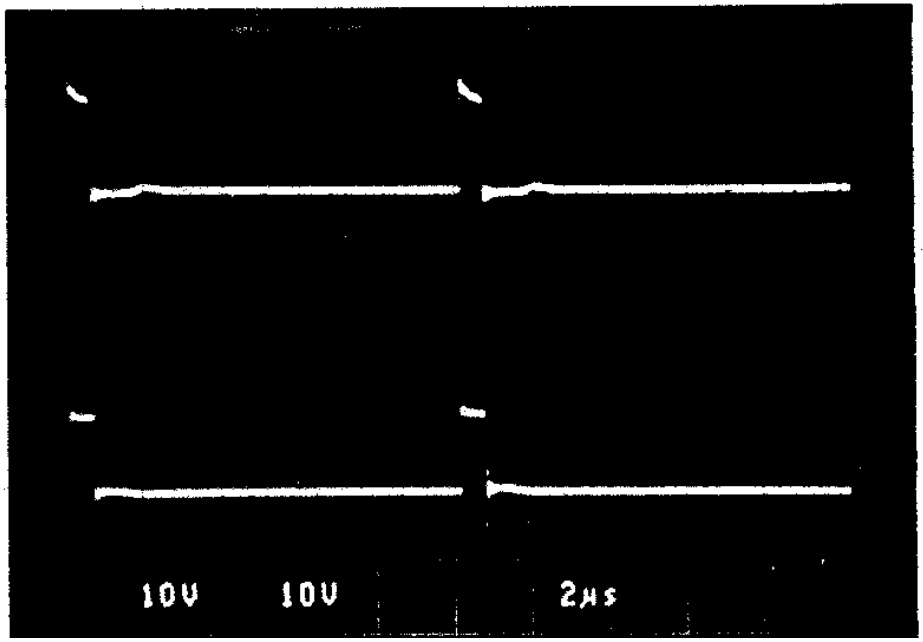

V(10)
OUT
V(4)
GATE1
10
X3
IRFF110
R2
4.7
C_LOAD
2000P
X2
XFMR-TAP
4
8
VIN
PULSE
9
1
V(1)
IND
X1
MAGF
C1 .01U
2
R1 33
D2 DN4148
3
V(9)
IN
V(2)
TP1
V(3)
TP2

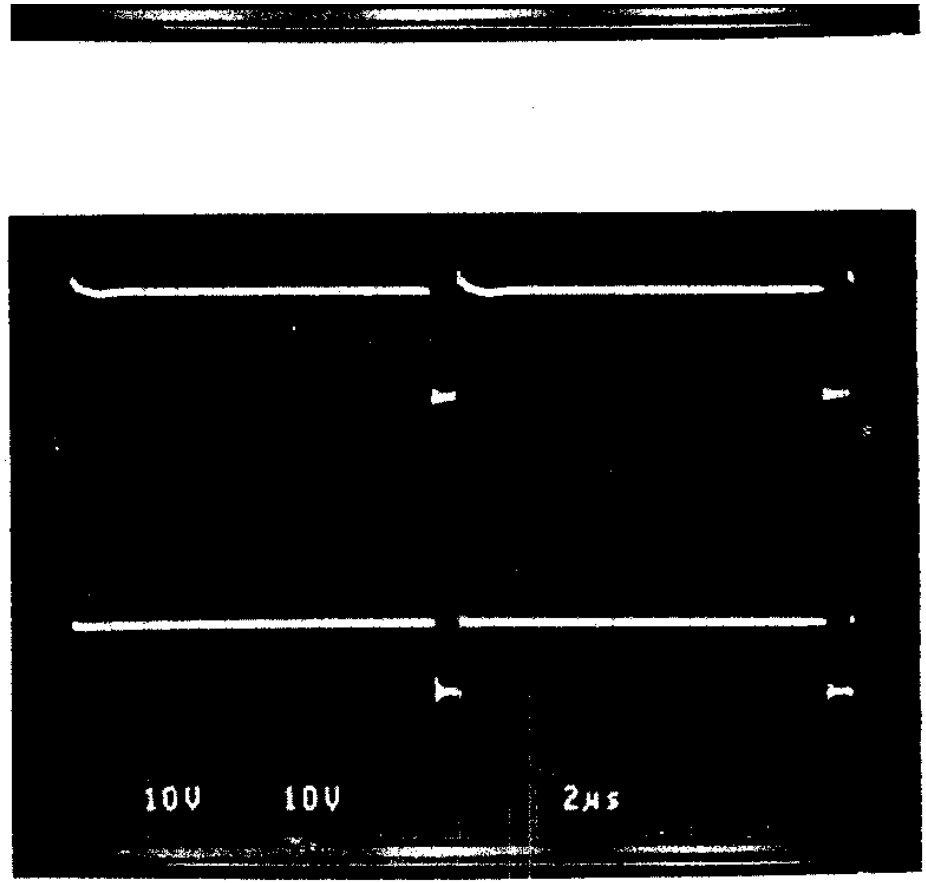
DRIVE WAVEFORMS
INTO 2000pf LOAD

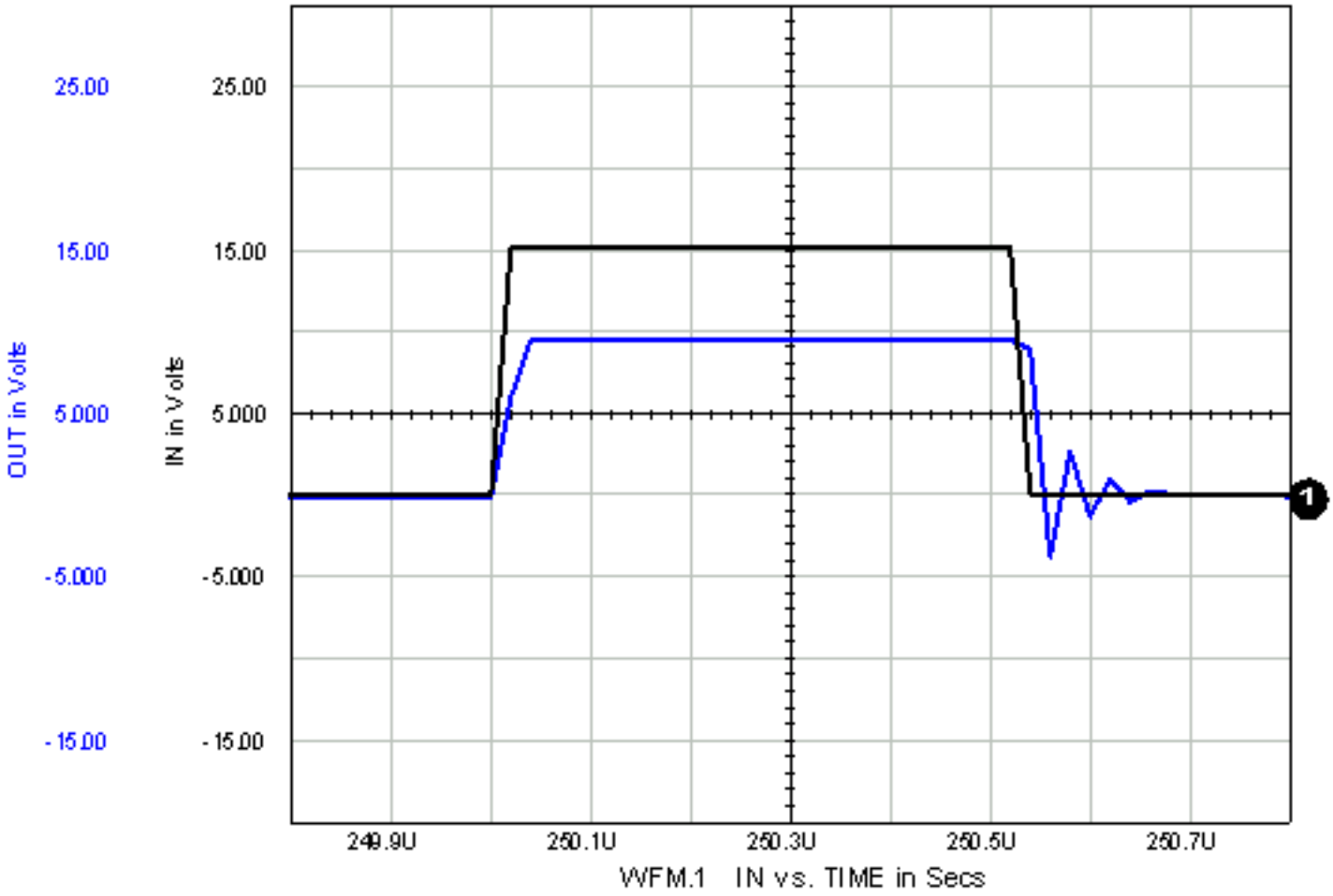


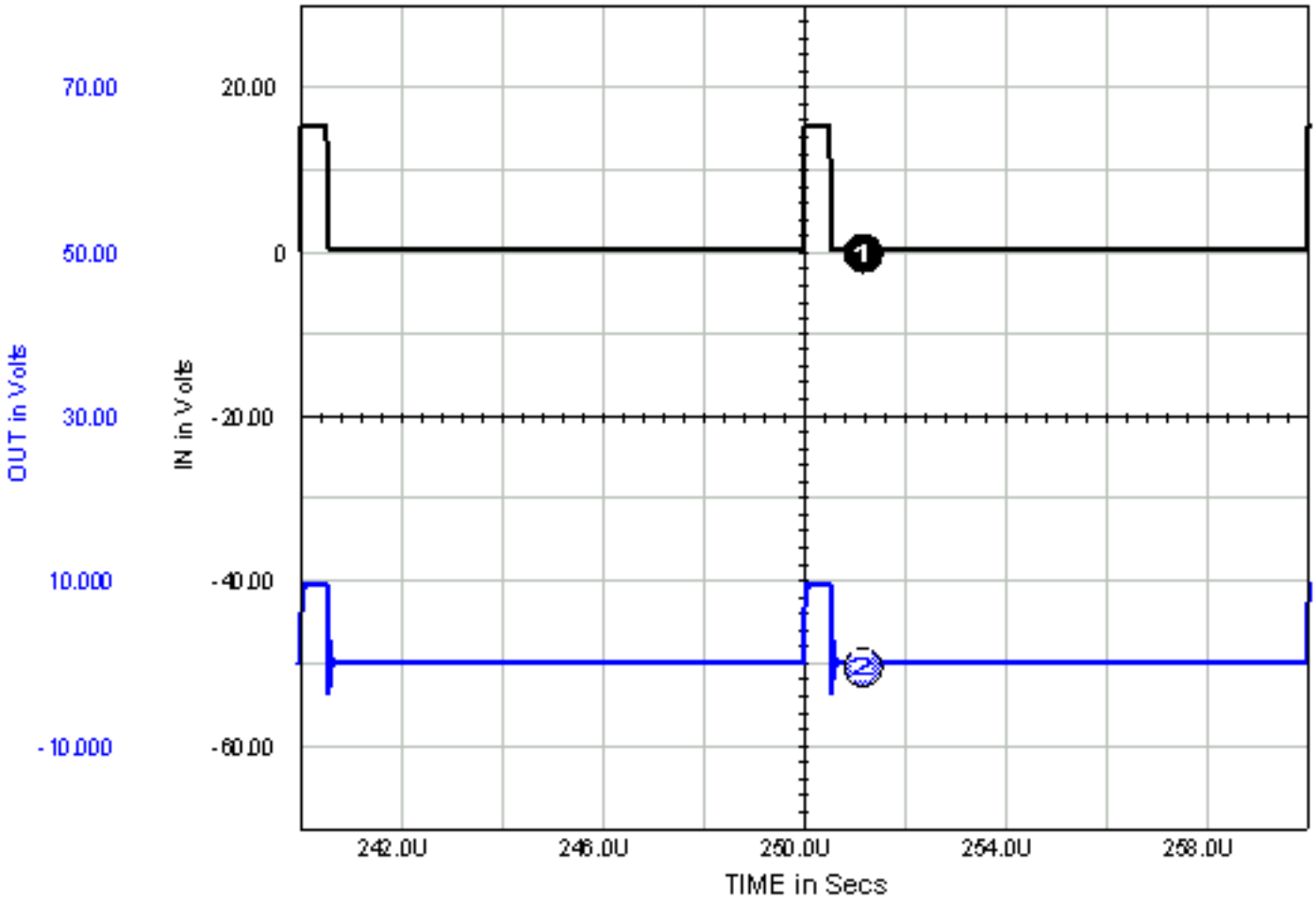
INPUT

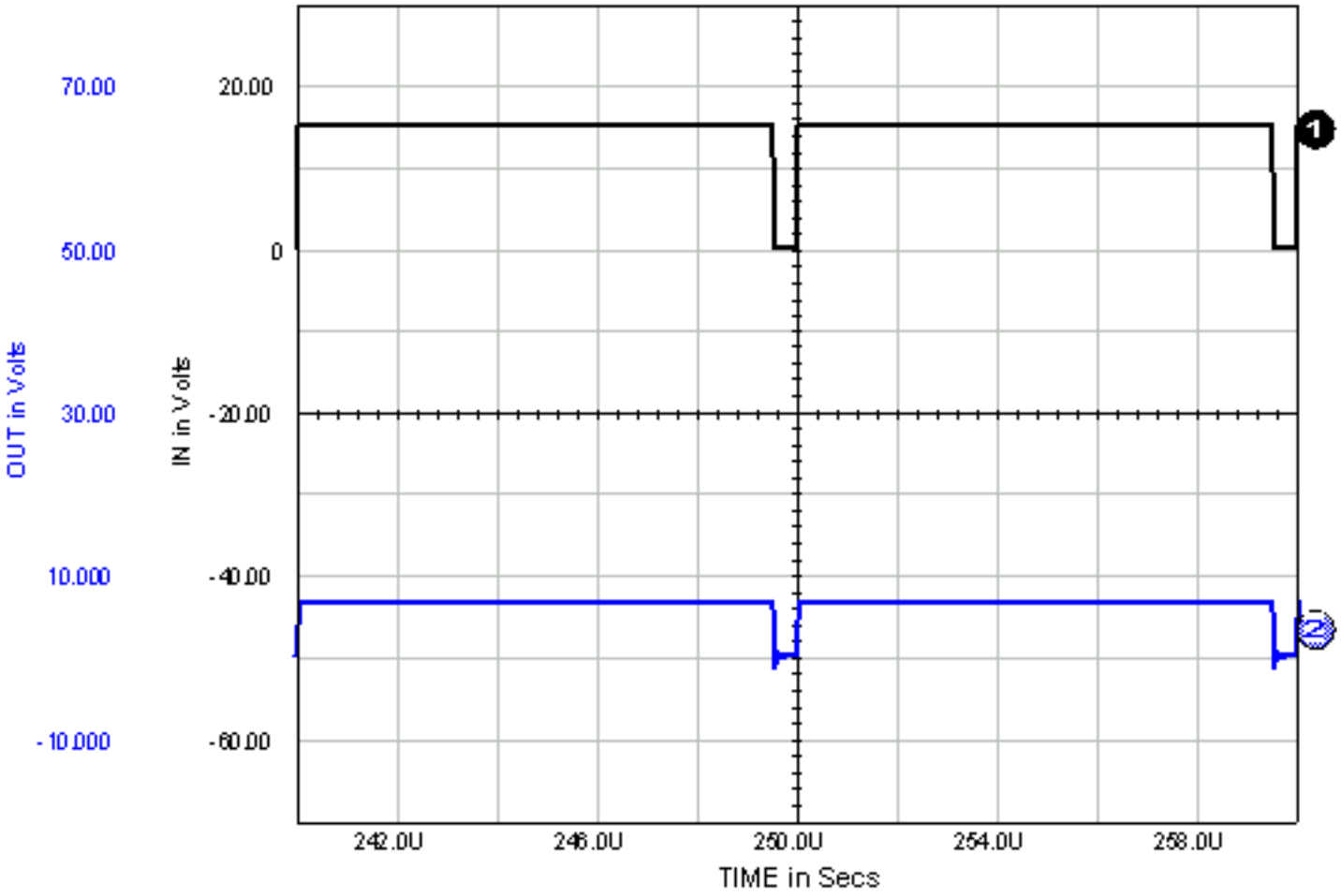
OUTPUT

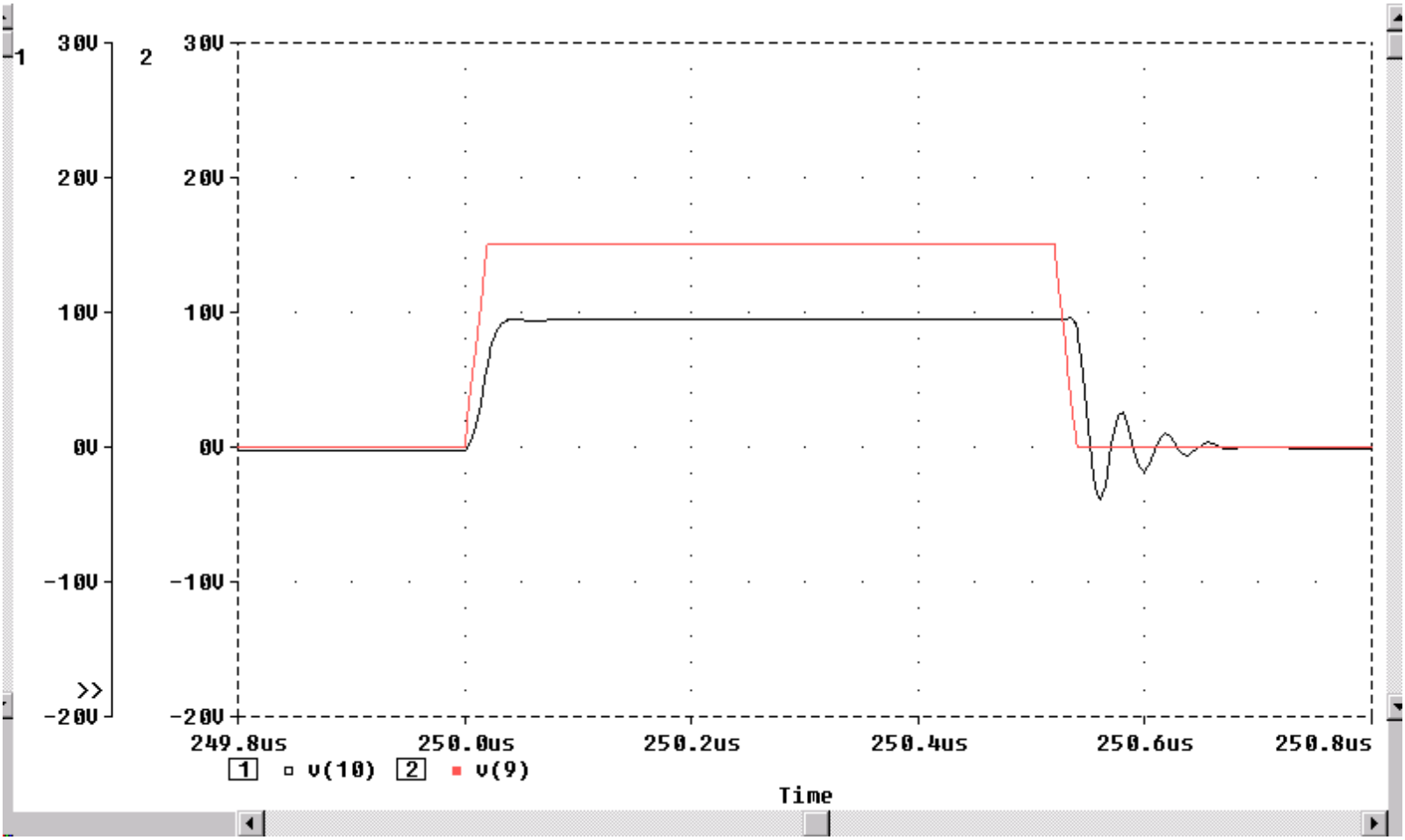


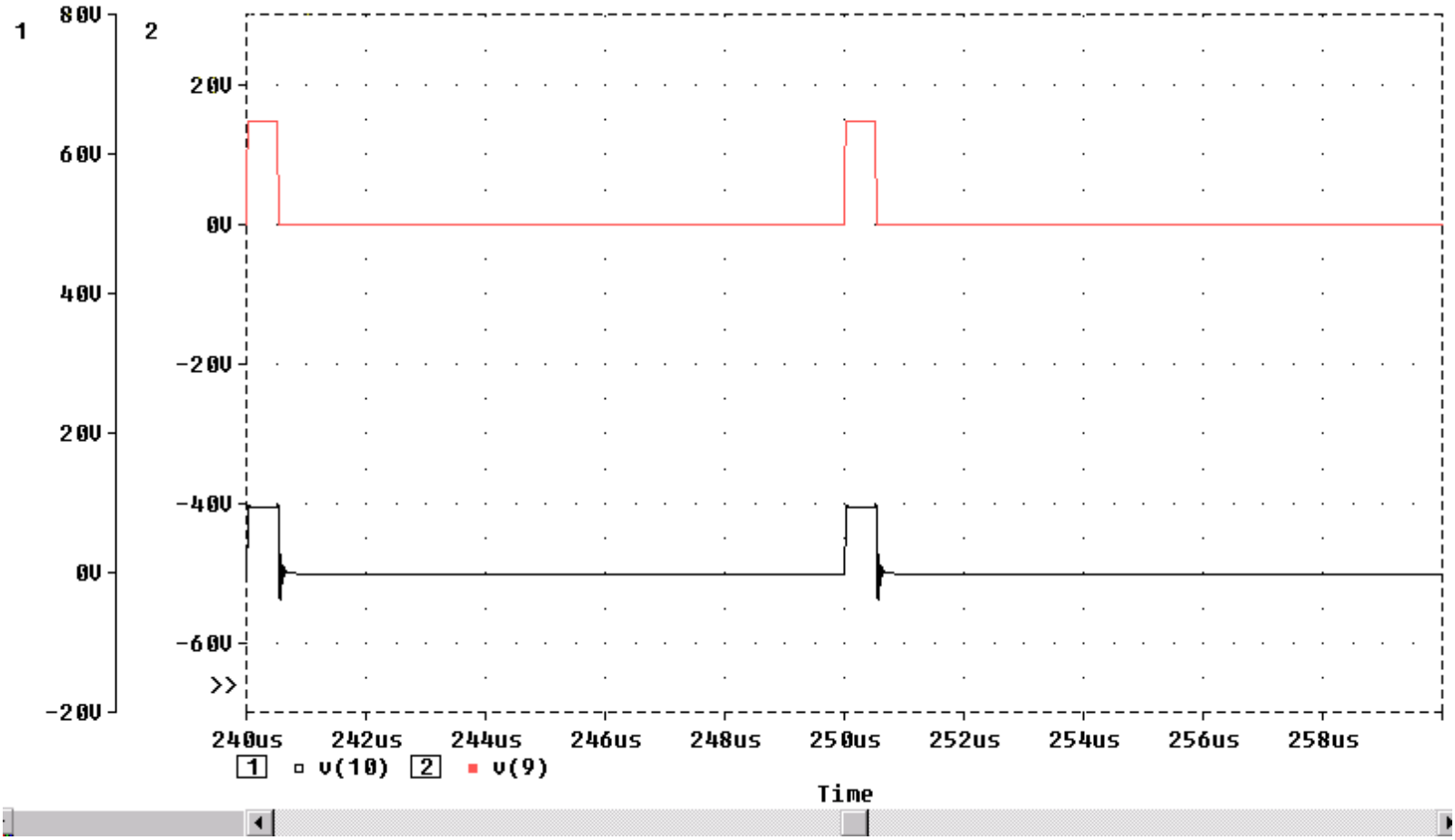

INPUT
OUTPUT
10V
10V
2μs

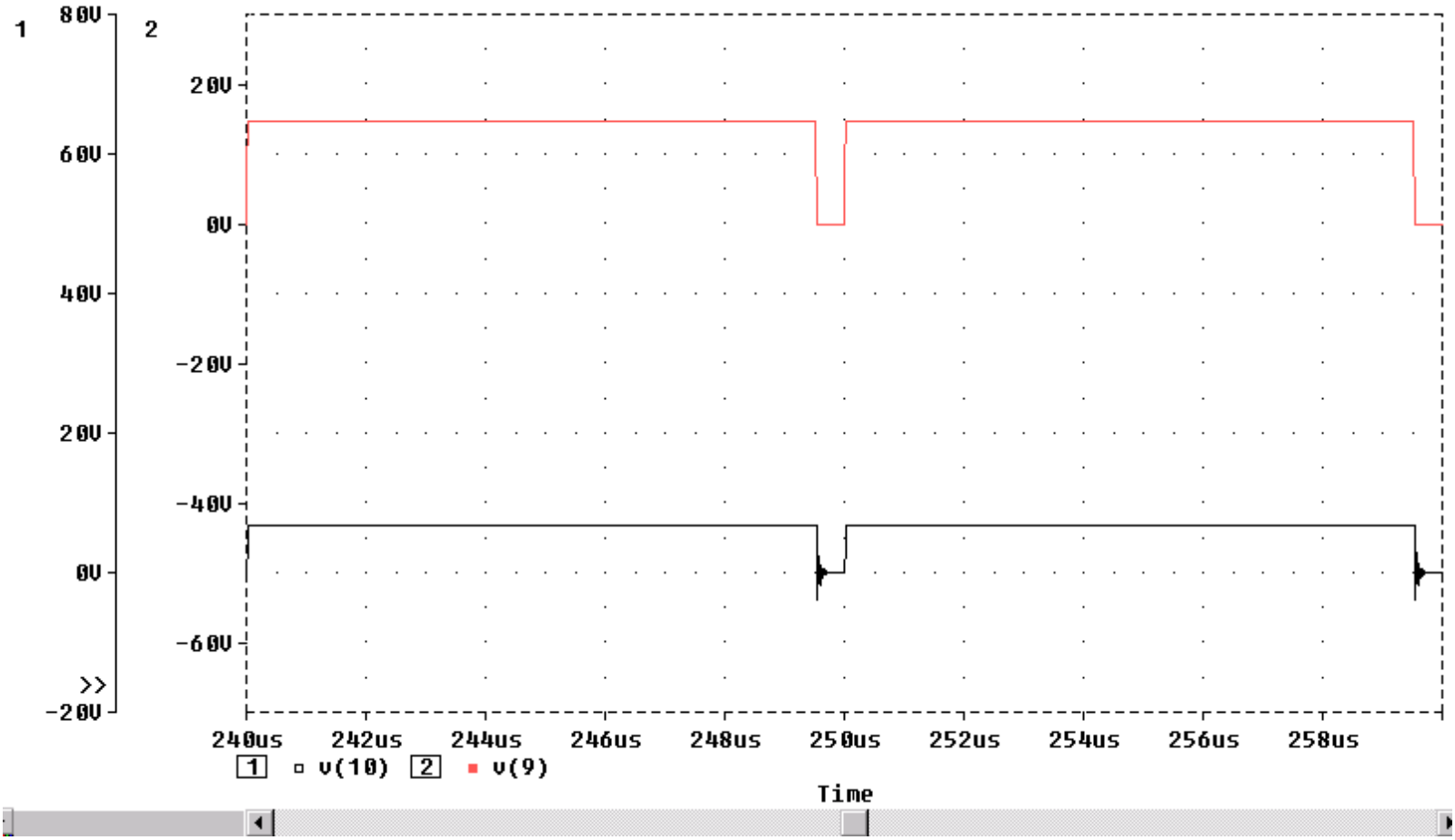

25.00
15.00
5.000
-5.000
-15.00
OUT in Volts
25.00
15.00
5.000
-5.000
-15.00
IN in Volts
249.9U
250.1U
250.3U
250.5U
250.7U
WFM.1 IN vs. TIME in Secs
1

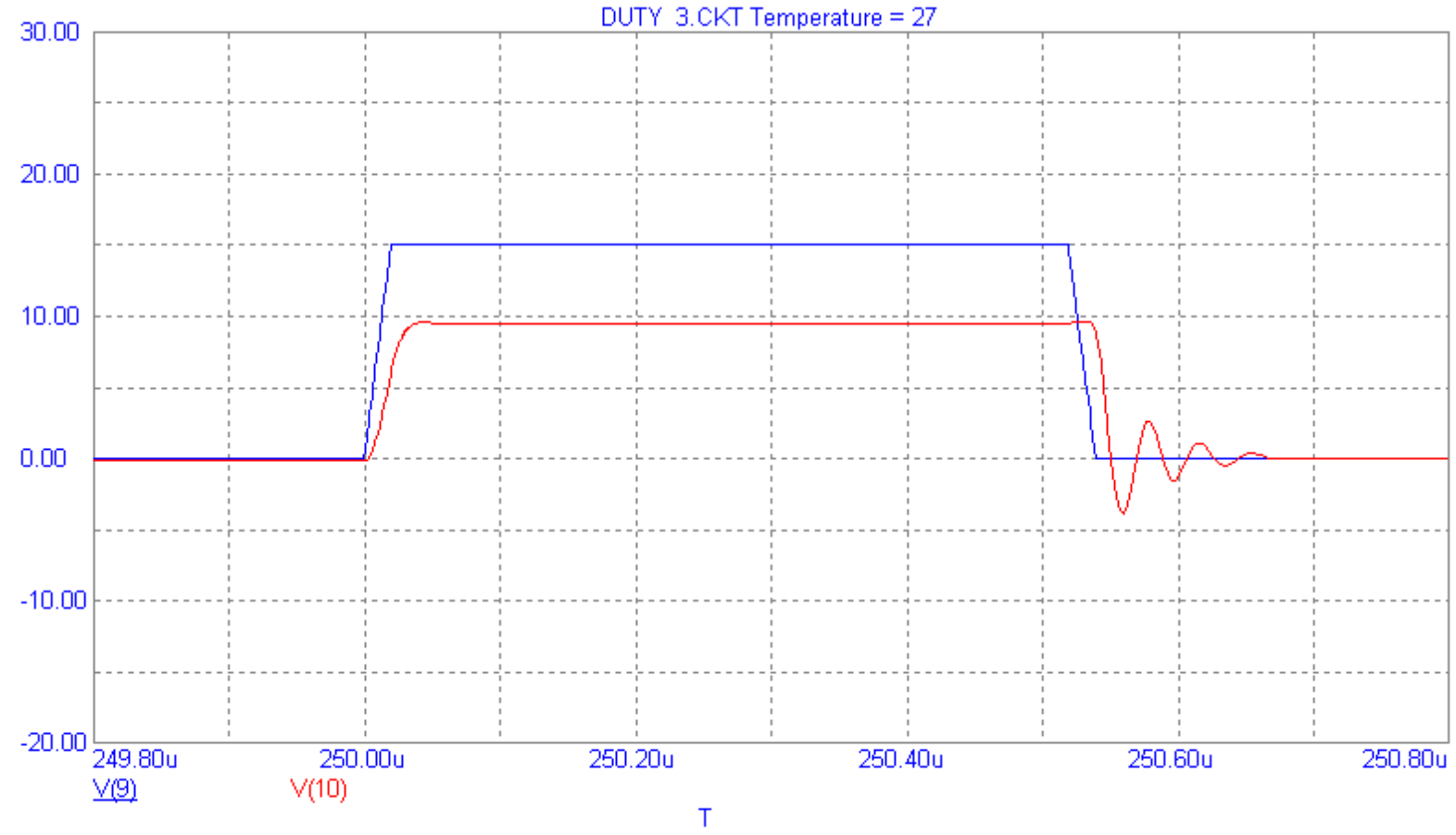

70.00
50.00
30.00
10.000
-10.000
OUT in Volts
20.00
0
-20.00
-40.00
-60.00
IN in Volts
242.0U
246.0U
250.0U
254.0U
258.0U
TIME in Secs
1
2

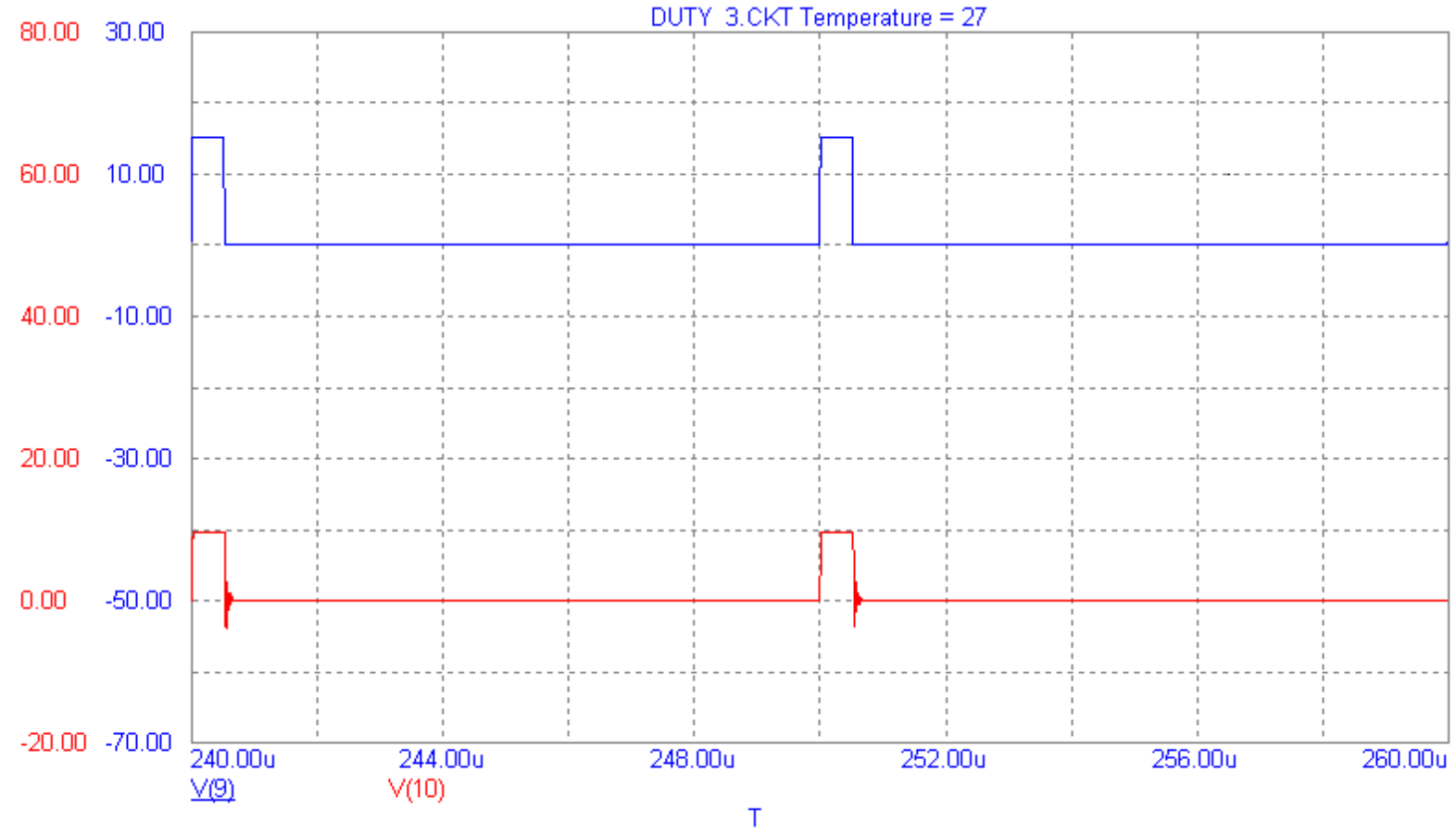

70.00
50.00
30.00
10.000
-10.000
OUT in Volts
20.00
0
-20.00
-40.00
-60.00
IN in Volts
242.0U
246.0U
250.0U
254.0U
258.0U
TIME in Secs
1
2

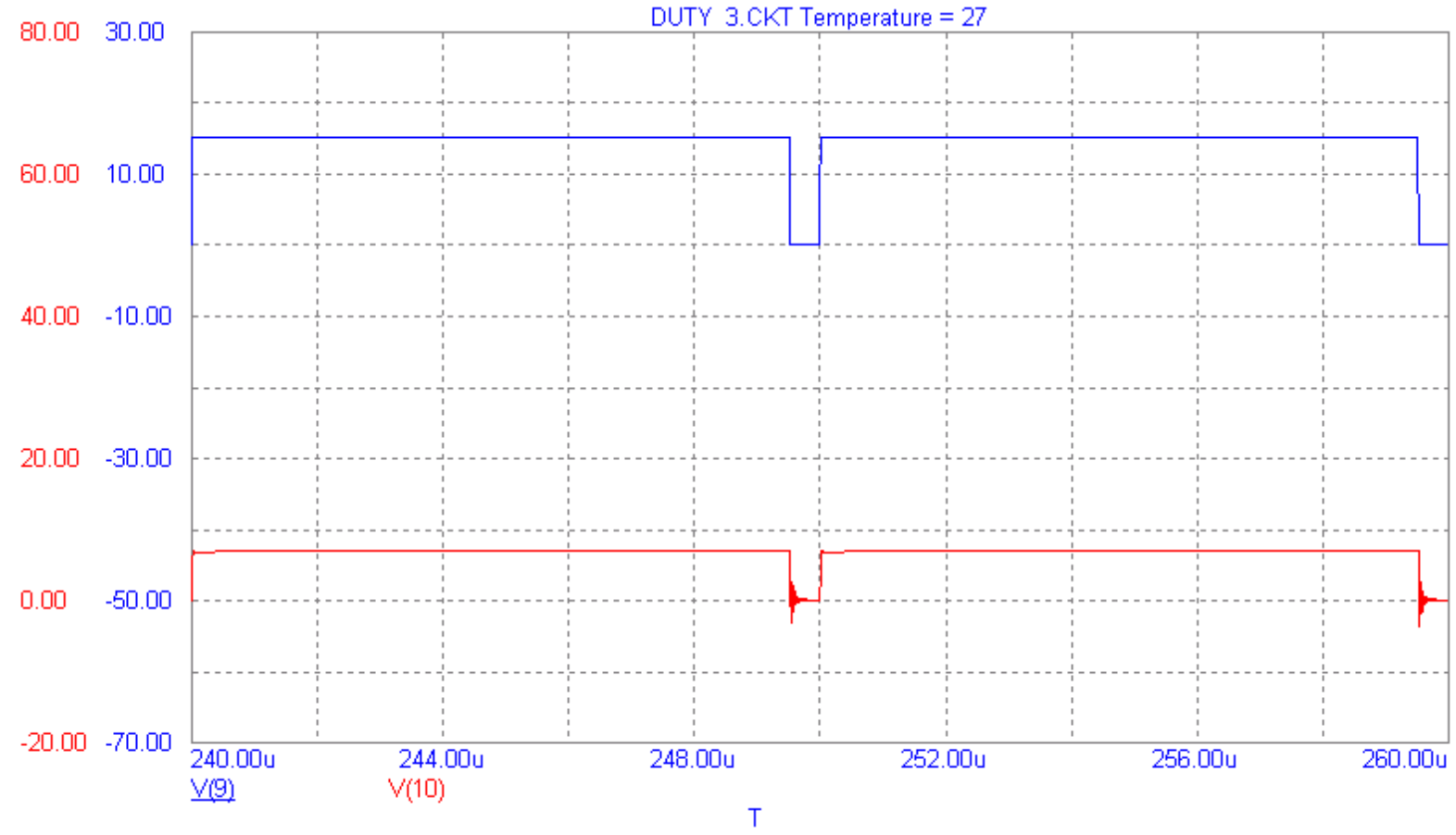

1
2
30V
20V
10V
0V
-10V
>>
-20V
249.8us
250.0us
250.2us
250.4us
250.6us
250.8us
1 v(10) 2 v(9)
Time


1
2
80V
60V
40V
20V
0V
-20V
20V
0V
-20V
-40V
-60V
>>
240us
242us
244us
246us
248us
250us
252us
254us
256us
258us
1 v(10) 2 v(9)
Time


1
2
80V
60V
40V
20V
>>
-20V
20V
0V
-20V
-40V
-60V
240us
242us
244us
246us
248us
250us
252us
254us
256us
258us
1 v(10) 2 v(9)
Time


DUTY 3.CKT Temperature = 27
30.00
20.00
10.00
0.00
-10.00
-20.00
249.80u
250.00u
250.20u
250.40u
250.60u
250.80u
V(9)
V(10)
T


DUTY 3.CKT Temperature = 27
80.00
30.00
60.00
10.00
40.00
-10.00
20.00
-30.00
0.00
-50.00
-20.00
-70.00
240.00u
244.00u
248.00u
252.00u
256.00u
260.00u
V(9)
V(10)
T


DUTY 3.CKT Temperature = 27
80.00
30.00
60.00
10.00
40.00
-10.00
20.00
-30.00
0.00
-50.00
-20.00
-70.00
240.00u
244.00u
248.00u
252.00u
256.00u
260.00u
V(9)
V(10)
T

#45: AC to DC voltage doubler

The conventional voltage doubler is a very simple, yet effective method of creating a DC voltage from an AC voltage [Mimms, 1991]. The schematic for the conventional voltage doubler is shown in Figure 45-1. The input is an AC waveform. This particular circuit was measured using both a square wave and a sine wave, with the circuit working using both input types. During the positive cycle of the AC waveform, the waveform is rectified by diode D1 and capacitor C1. During the negative cycle, the waveform is rectified by diode D2 and C2. This creates an effective DC voltage at the output terminals that is roughly 2 times the AC voltage minus the forward drop of the diode. The resistor R3 was added as a slight load.

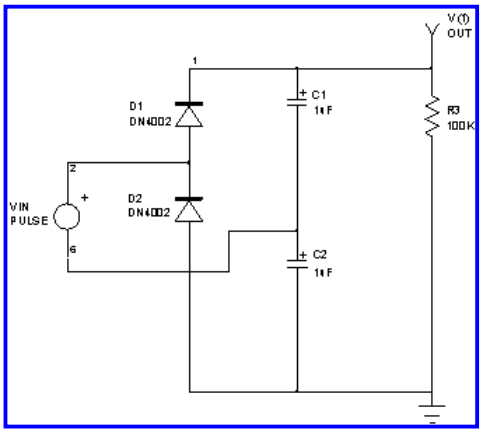


Figure 45-1: Schematic of Conventional Doubler

The actual SPICE model of this circuit is shown in Figure 45-2. Notice there are two resistors in series with each of the capacitors, R1 and R2. These resistors are modeling the approximate Equivalent Series Resistance (ESR) of the tantalum capacitors in the circuit at the switching frequency.

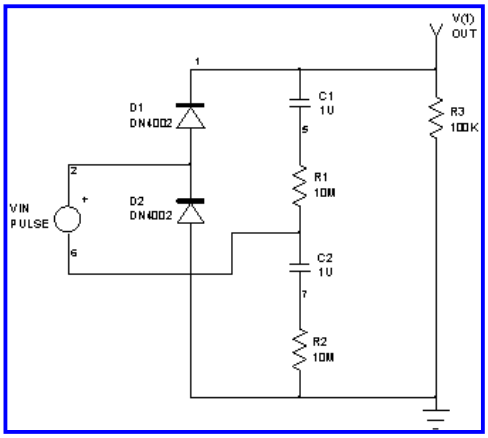


Figure 45-2: SPICE equivalent Schematic of Conventional Doubler

This circuit was built in the lab using 1N4002 1A 100V rated diodes with 1 uF tantalum capacitors. The input pulse was a square wave from -3 volts to +3 volts. The input pulse had a frequency of 5 Khz at a 50% duty cycle. The PULSE statement in the SPICE model is shown below:

PULSE -3 3 .1U .1U 100U 200U

The input pulse and the output DC voltage was measured using the Oscilloscope. The result picture is shown in Figure 45-3A. Unfortunately, the ripple on the breadboard was small enough to be swamped by the noise in the lab, and we were not able to make an accurate measurement. The IsSpice model result is shown in Figure 45-3B. The top waveform is the output voltage and the bottom waveform is the input pulse.

- Breadboard tip: It is not necessary to use the 1N4002 rectifier for this circuit. When choosing a rectifier, remember, the diode reverse characteristics must be rated for 2 times the input voltage.

- Simulation tip: In order to allow the simulation to find the DC voltage, the simulation was run for 10 mSec. Each of the simulations used Initial Conditions (IC) in order to shorten the simulation time. In this simulation, the capacitors were biased at an initial voltage of 2.75 volts. In Pspice, this is accomplished by double clicking the capacitor and changing the attribute for IC. In Microcap, this is accomplished by clicking the TEXT toolbutton and entering the command .IC v(2)=2.25 v(4)=2.25. In IsSpice, this is accomplished by double clicking the capacitor and entering IC=2.5 after the capacitance value.

- Spice tip: The only real error source for the output voltage is the forward drop characteristics of this diode . Each of the three SPICE simulators have a model for the 1N4002 diode, with all of the simulators within about 100 mV of each other. The question becomes which model is correct? The answer is they are all probably correct. The forward drop tolerance of a diode varies from lot to lot, from manufacturer to manufacturer, and from device to device. Table 45-1 shows the results of each of the three simulators along with the breadboard results.

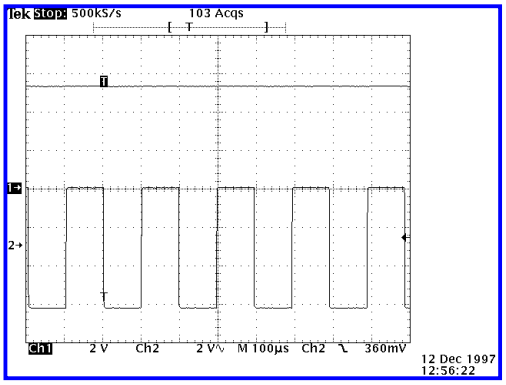


Figure 45-3A: Breadboard waveforms of input and output

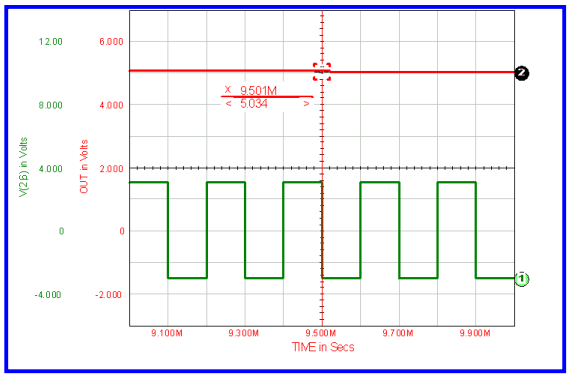


Figure 45-3B: IsSpice waveforms of input and output

Output Voltage Results Summary			
IsSpice v 7.6	Pspice v 6.3	Micro-Cap V v2	Breadboard
5.034 Volts	5.078 Volts	4.998 Volts	5.21 Volts

Table 45-1: Output voltage comparison between SPICE and breadboard

The results of the Microcap simulation are shown in Figure 45-4, while the Pspice results are shown in Figure 45-5.

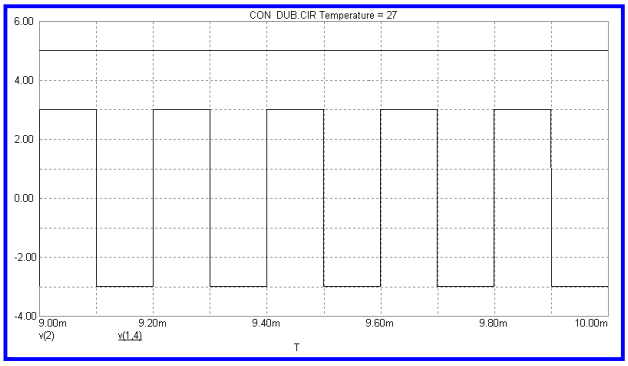


Figure 45-4: Microcap input and output waveforms

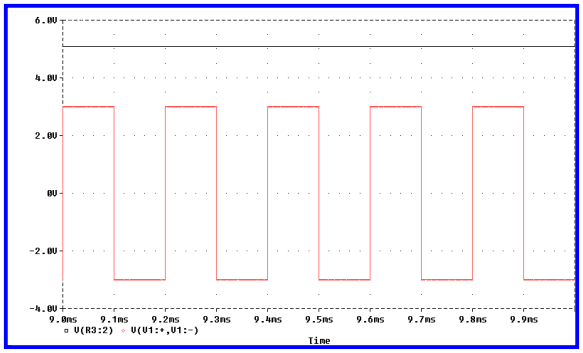


Figure 45-5: Pspice input and output waveforms

Run Time Summary		
IsSpice v 7.6	PsPice v 6.3	Micro-Cap V v2
32.21 Sec	52.03 Sec	49.34 Sec
Advantages: Low parts count		
Disadvantages: Current capability limited by source, ripple not as controlled as other topologies, no AC/DC isolation, no regulation.		

Filenames: con_dou (IsSpice) con_dub (Micro-cap) con_doub (Pspice)

#46: Cascade Doubler

By slightly altering the circuit in Figure 45-1, we can attain the cascade doubler, which has the output characteristics as the Conventional doubler. This circuit is shown in Figure 46-1A. The SPICE equivalent circuit is shown in Figure 46-1B.

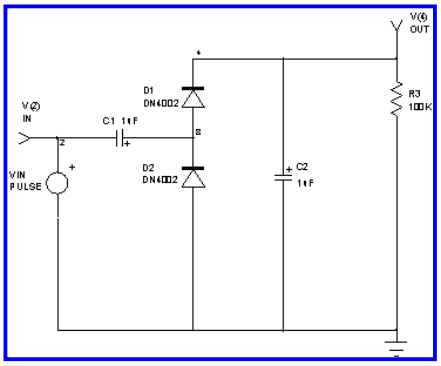


Figure 46-1A: Schematic of Cascade Doubler

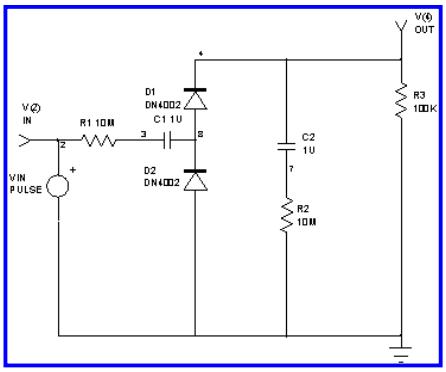


Figure 46-1B: SPICE Schematic of Cascade Doubler

This circuit used the same 1N4002 diodes as circuit #45, the same 1uF capacitors, and the same 5Khz ± 3 volt input pulse. A 100 Kohm resistor acts as a load for the circuit. The breadboard results are shown in Figure 46-2A, with the IsSpice results in Figure 46-2B. The top waveform is the DC output voltage and the bottom waveform is the AC input waveform.

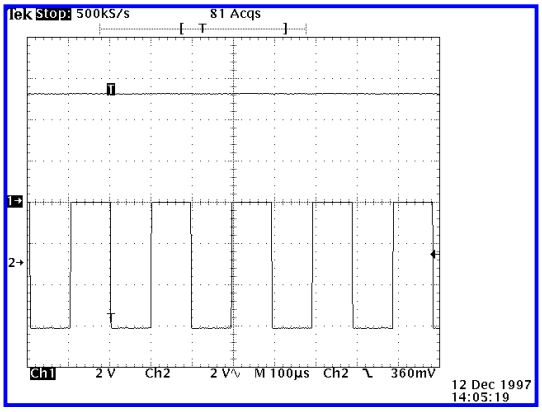


Figure 46-2A: Breadboard input and output waveforms

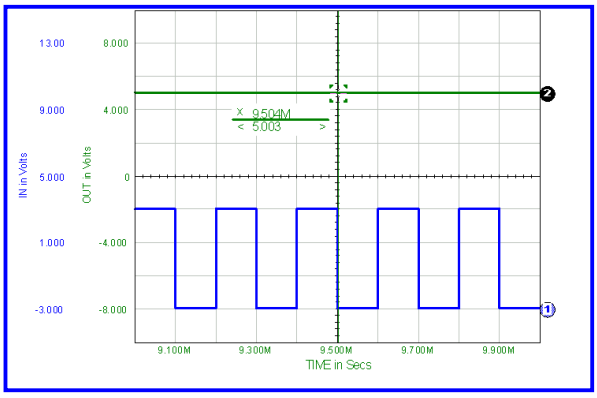


Figure 46-2B: IsSpice input and output waveforms

- Breadboard tip: Notice in Figure 46-1A, the capacitors are shown polarized. SPICE will not care one way or the other, but your breadboard tantalum or electrolytic capacitors will! Negative voltages on polarized capacitors will damage them just as easily as exceeding their rated voltage.

The results of the Microcap and Pspice simulators are shown in Figures 46-3 and 46-4. The results are tabulated and compared in Table 46-1.

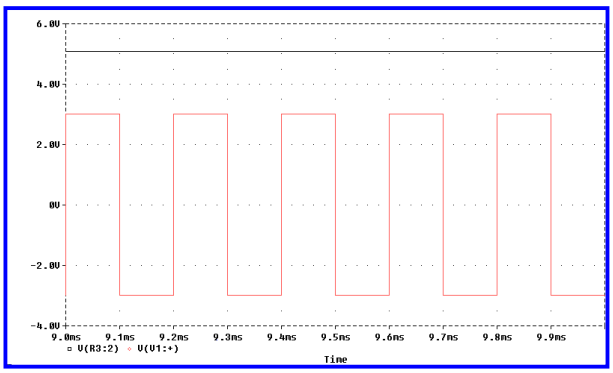


Figure 46-3: Pspice input and output waveforms

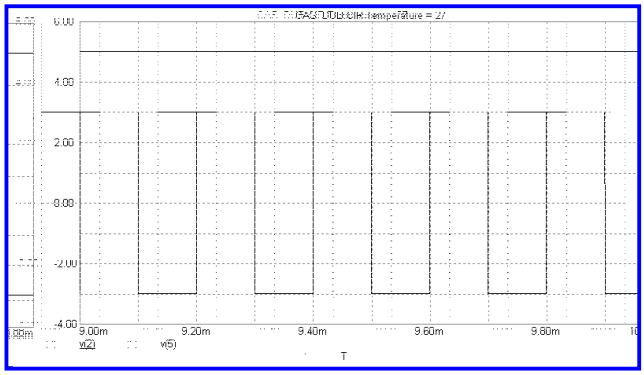


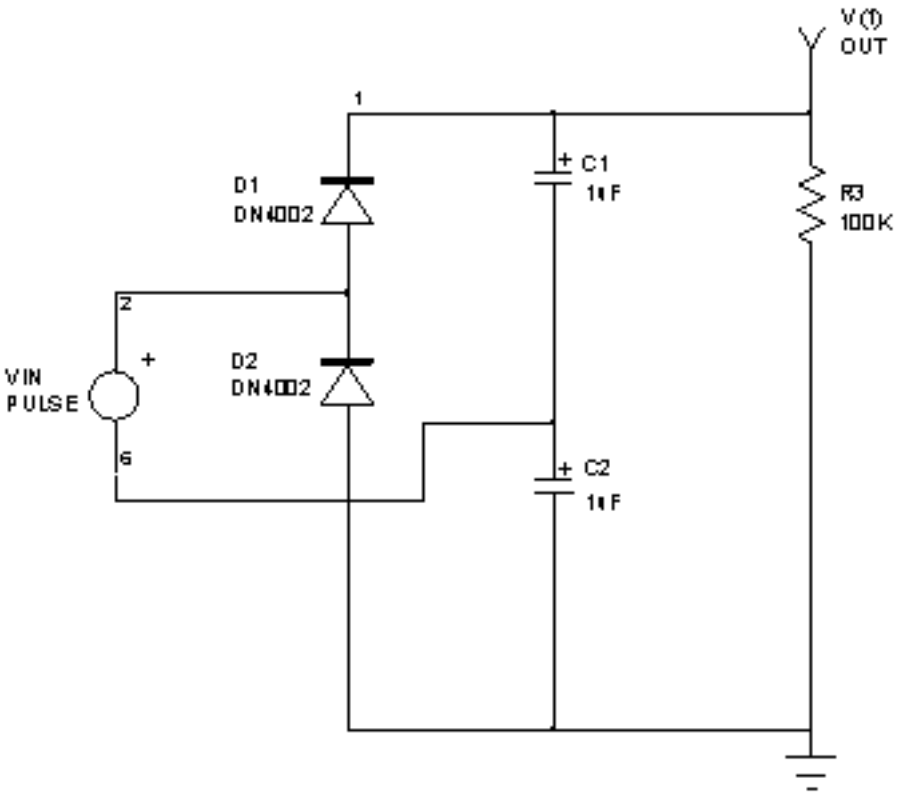
Figure 46-3: Microcap input and output waveforms

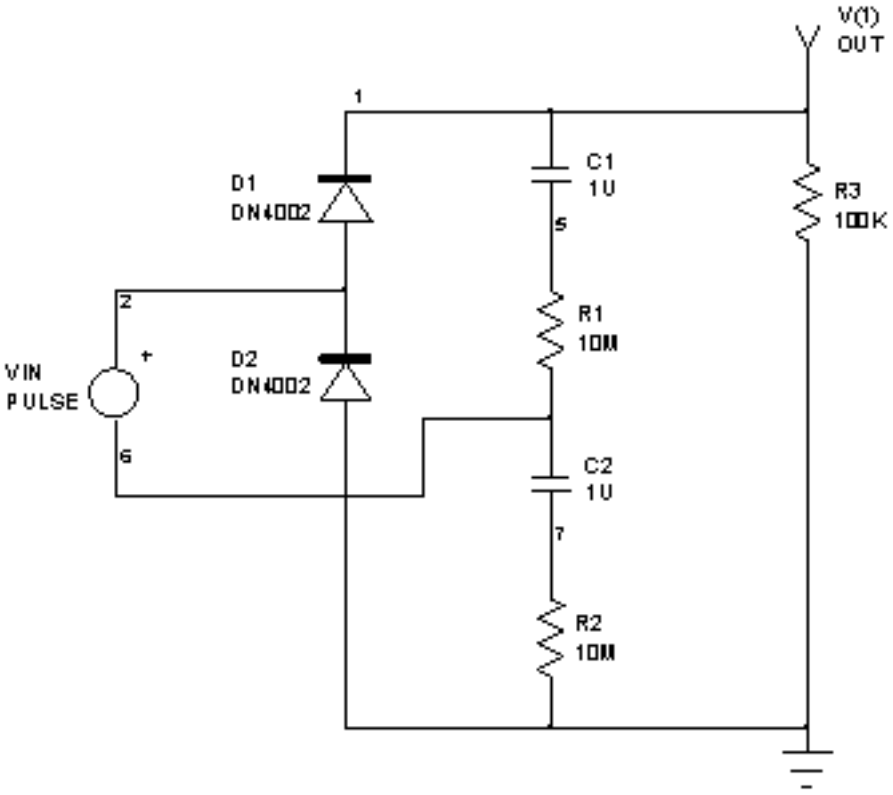
Output Voltage Results Summary			
IsSpice v 7.6	Pspice v 6.3	Micro-Cap V v2	Breadboard
5.003 Volts	5.081 Volts	4.995 Volts	5.15 Volts

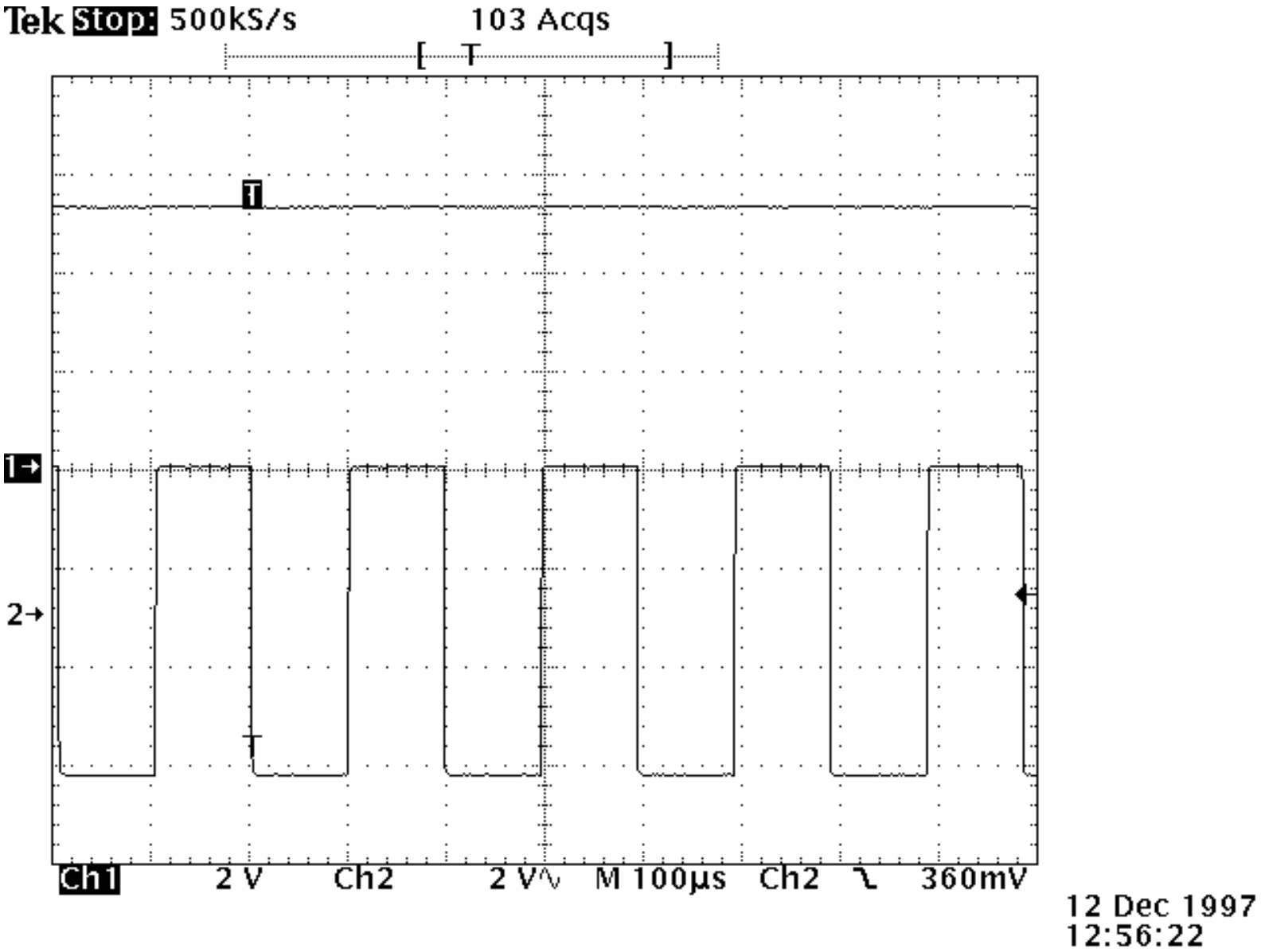
Table 46-1: Output voltage comparison between SPICE and breadboard

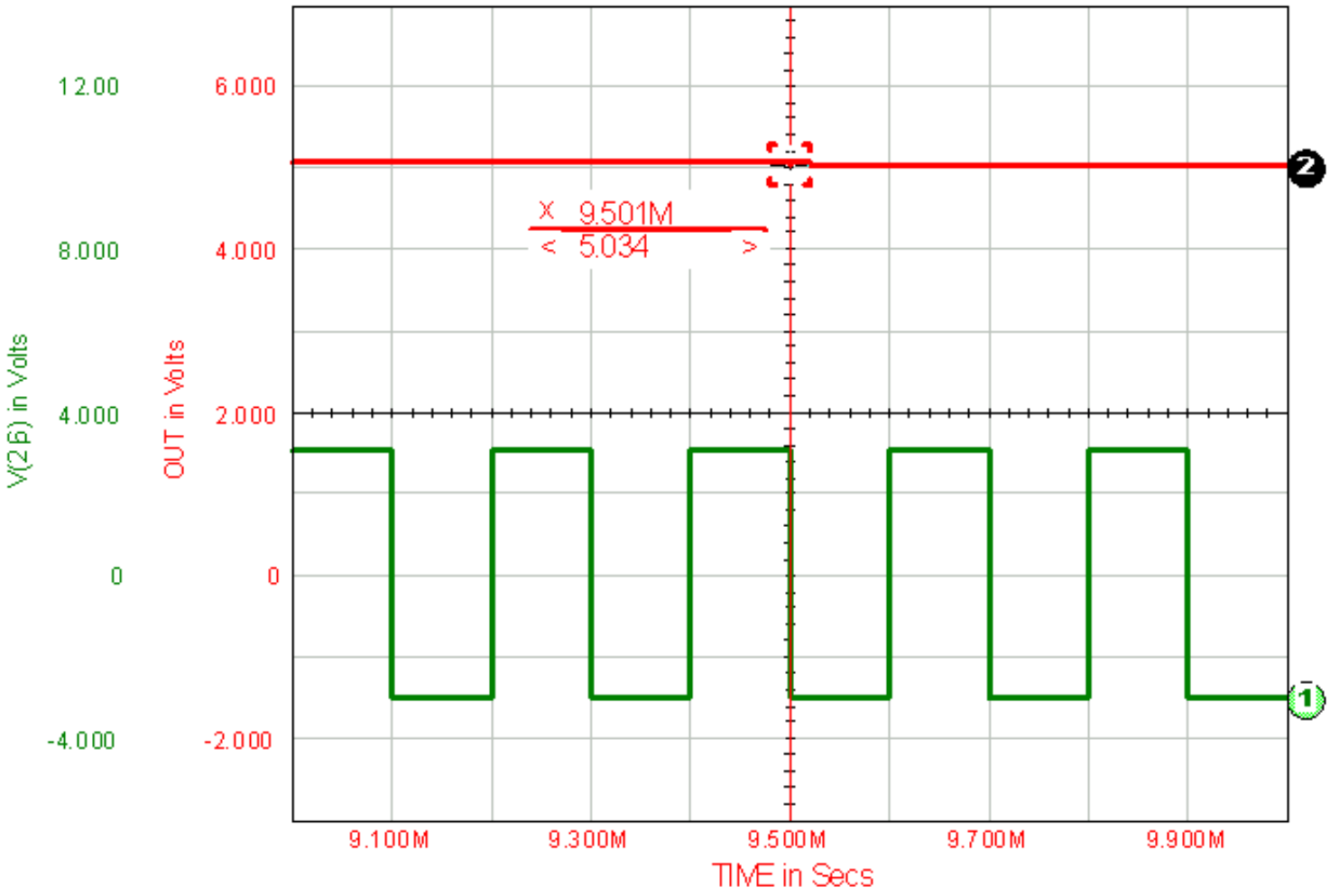
Run Time Summary		
IsSpice v 7.6	PsPice v 6.3	Micro-Cap V v2
22.18 Sec	49.08 Sec	48.064 Sec
Advantages: Low parts count		
Disadvantages: Current capability limited by source, ripple not as controlled as other topologies, no AC/DC isolation, no regulation.		

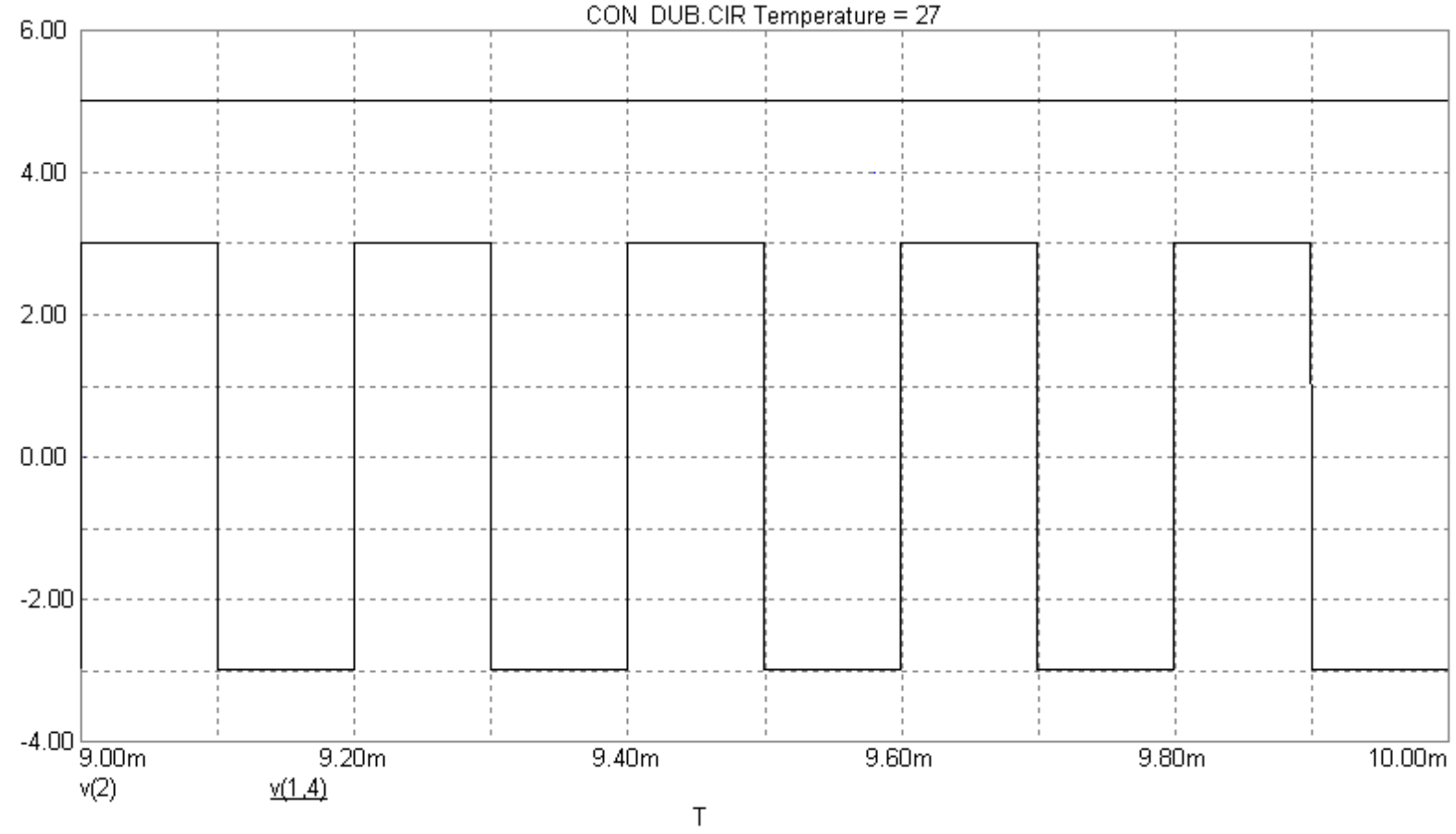
Filenames: cas_dou (IsSpice) cas_dub (Micro-cap) cas_doub (Pspice)

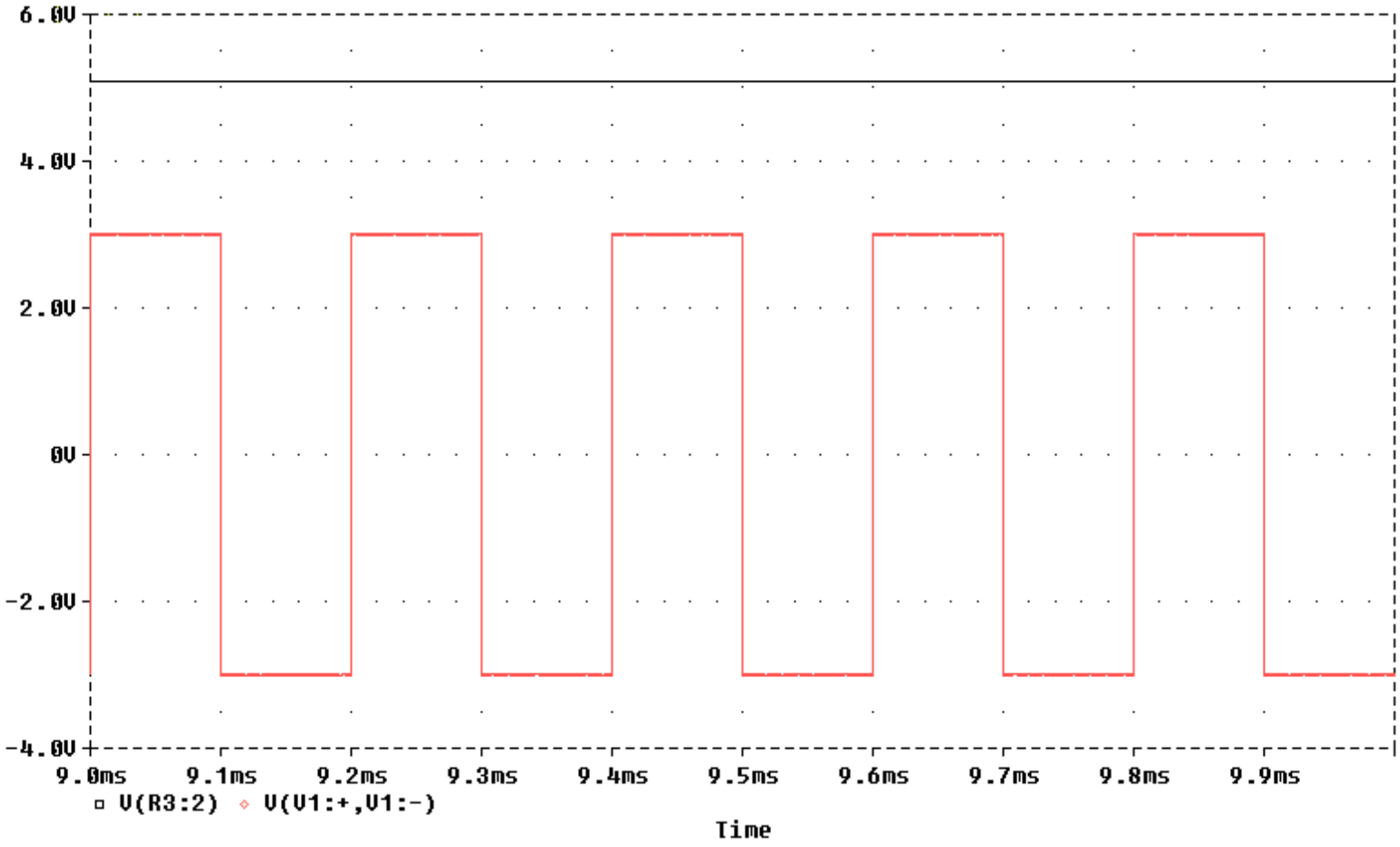

V(1)
OUT
1
D1
DN4002
C1
1uF
R3
100K
2
VIN
PULSE
+
D2
DN4002
6
C2
1uF


V(1)
OUT
1
D1
DN4002
C1
1U
R3
100K
5
2
R1
10M
VIN
PULSE
+
D2
DN4002
6
C2
1U
7
R2
10M


Tek Stop: 500kS/s
103 Acqs
1→
2→
Ch1 2 V Ch2 2 V M 100µs Ch2 360mV
12 Dec 1997
12:56:22


12.00
8.000
4.000
0
-4.000
V(2,0) in Volts
6.000
4.000
2.000
0
-2.000
OUT in Volts
X 9.501M
< 5.034 >
2
1
9.100M
9.300M
9.500M
9.700M
9.900M
TIME in Secs


CON DUB.CIR Temperature = 27
6.00
4.00
2.00
0.00
-2.00
-4.00
9.00m
9.20m
9.40m
9.60m
9.80m
10.00m
v(2)
v(1,4)
T


6.0V
4.0V
2.0V
0V
-2.0V
-4.0V
9.0ms
9.1ms
9.2ms
9.3ms
9.4ms
9.5ms
9.6ms
9.7ms
9.8ms
9.9ms
V(R3:2)
V(V1:+,V1:-)
Time

#47: Bridge AC to DC Doubler

An improvement to the conventional and cascade doublers shown above is the bridge rectifying doubler. Instead of half wave rectification, the bridge doubler provides full wave rectification. The advantages to full wave rectification include less input impedance and a ripple voltage at twice the input frequency, which improves ripple filtering capability. The schematic for the bridge doubler is shown in figure 47-1. The IsSpice equivalent schematic is shown in figure 47-2.

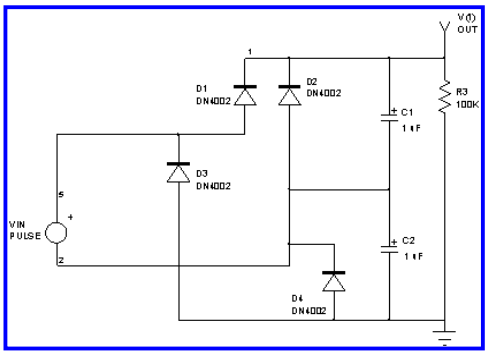


Figure 47-1: Schematic of Bridge Rectifying Doubler

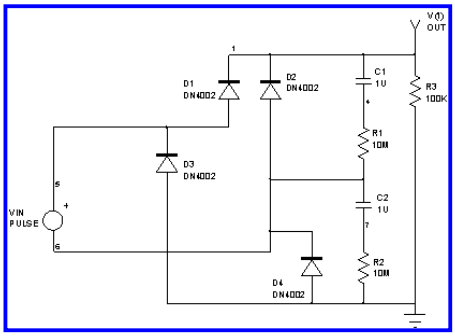


Figure 47-2: SPICE Schematic of Bridge Rectifying Doubler (with ESR shown)

This circuit used the same 1N4002 diodes as circuit #45, the same 1uF capacitors, and the same 5Khz ± 3 volt input pulse. Again, a 100 Kohm resistor acts as a load for the circuit. The breadboard results are shown in Figure 47-3A, with the IsSpice results in Figure 47-3B. The top waveform is the DC output voltage and the bottom waveform is the AC input waveform.

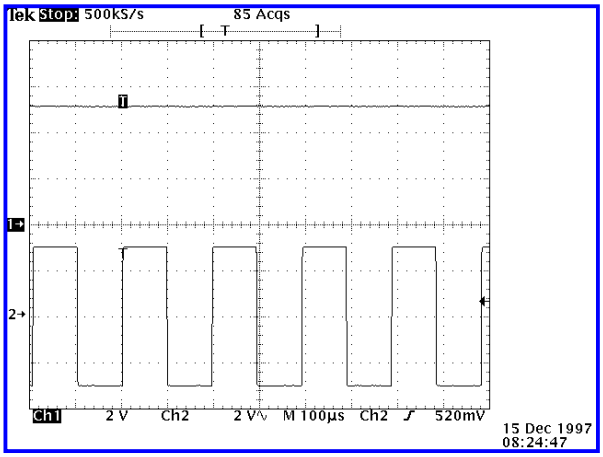


Figure 47-3A: Breadboard input and output waveforms

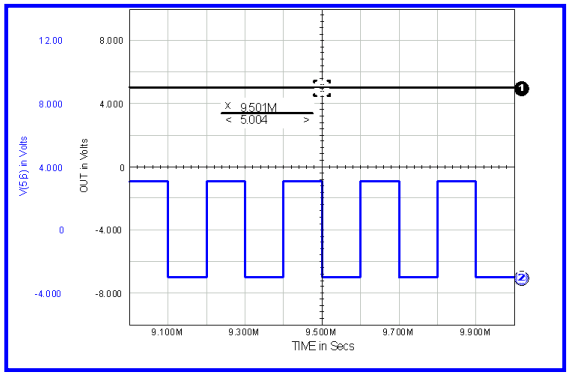


Figure 47-3B: IsSpice input and output waveforms

The results of the Microcap and Pspice simulators are shown in Figures 47-4 and 47-5. The results are tabulated and compared in Table 47-1.

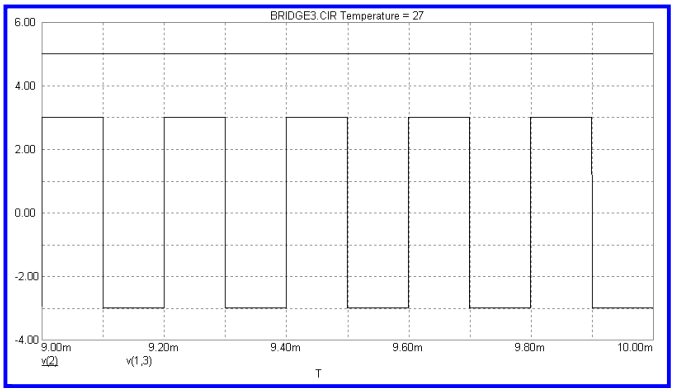


Figure 47-4: Microcap input and output waveforms

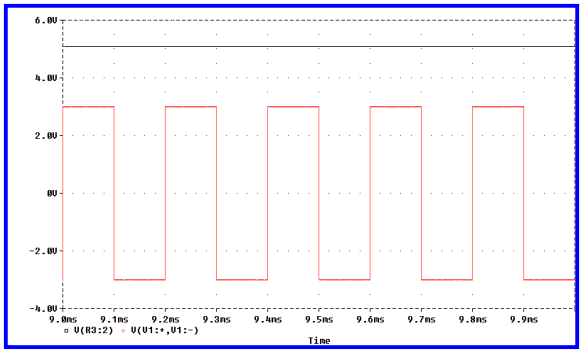


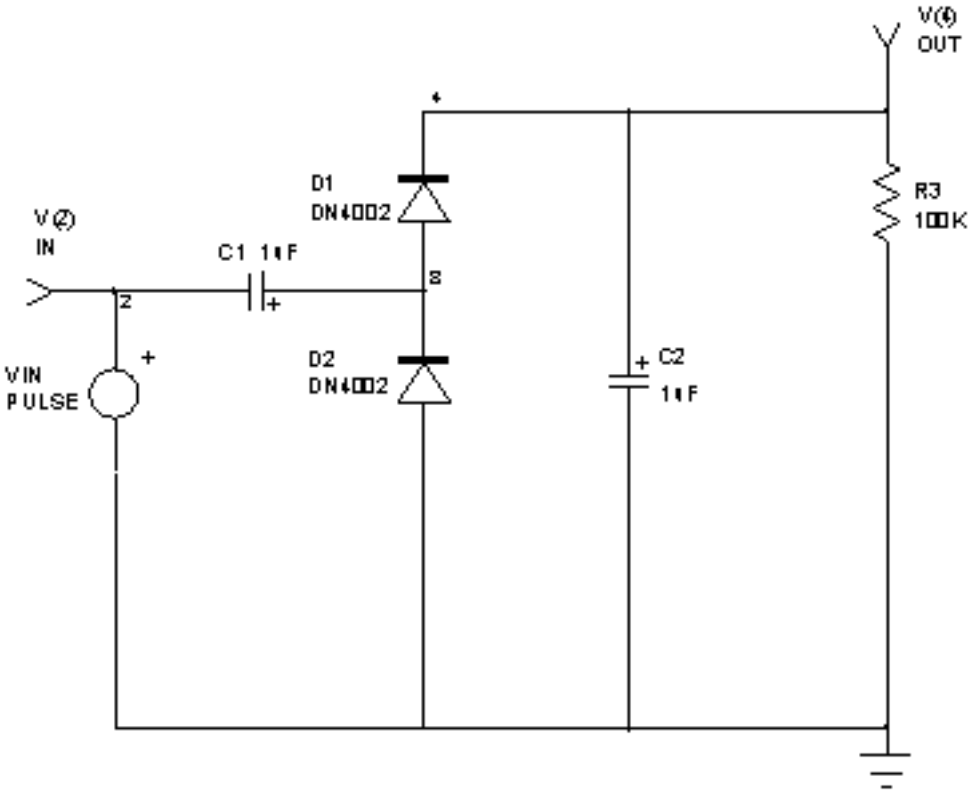
Figure 47-5: Pspice input and output waveforms

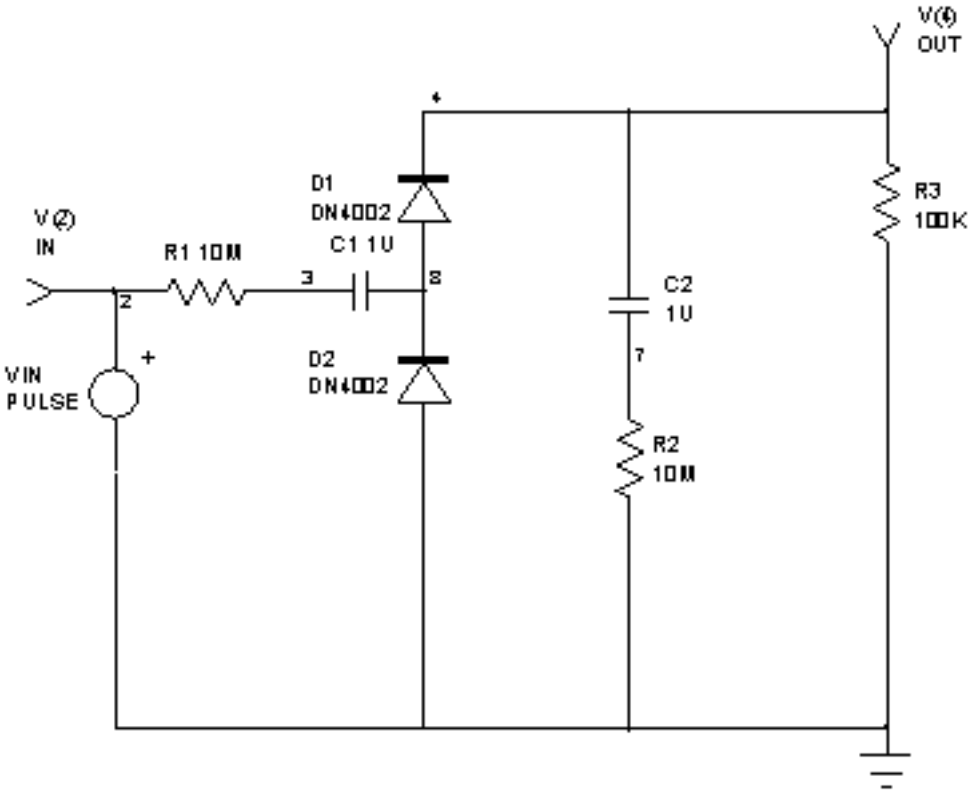
Output Voltage Results Summary			
IsSpice v 7.6	Pspice v 6.3	Micro-Cap V v2	Breadboard
5.004 Volts	5.087 Volts	4.998 Volts	4.95 Volts

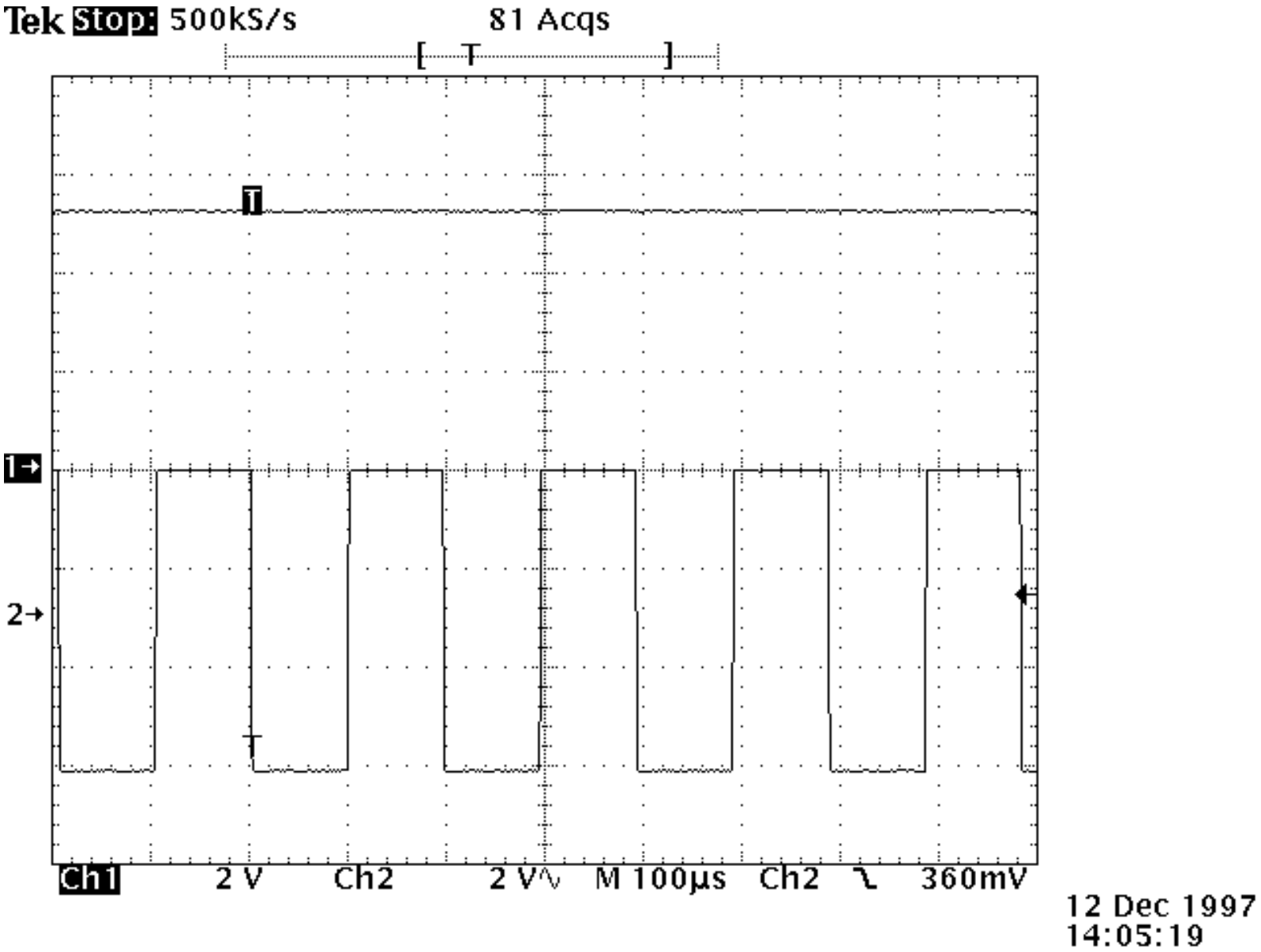
Table 47-1: Output voltage comparison between SPICE and breadboard

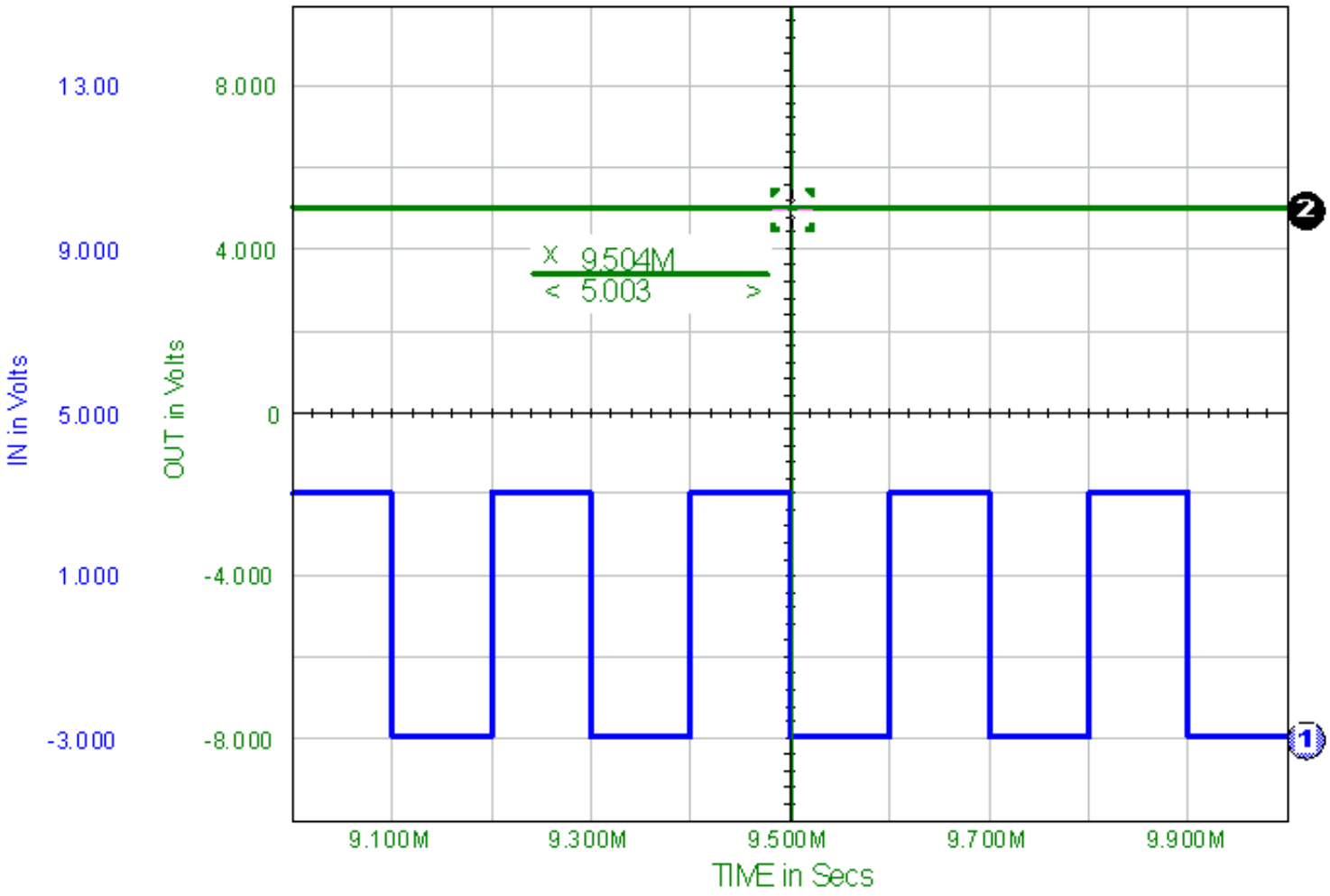
Run Time Summary		
IsSpice v 7.6	PsPice v 6.3	Micro-Cap V v2
27.73 Sec	55.03 Sec	65.92 Sec
Advantages: medium parts count, lower impedance than conventional doublers, full wave rectification allows for less filtering (ripple now at twice the switching frequency).		
Disadvantages: Current capability limited by source, ripple not as controlled as other topologies, no AC/DC isolation, no regulation.		

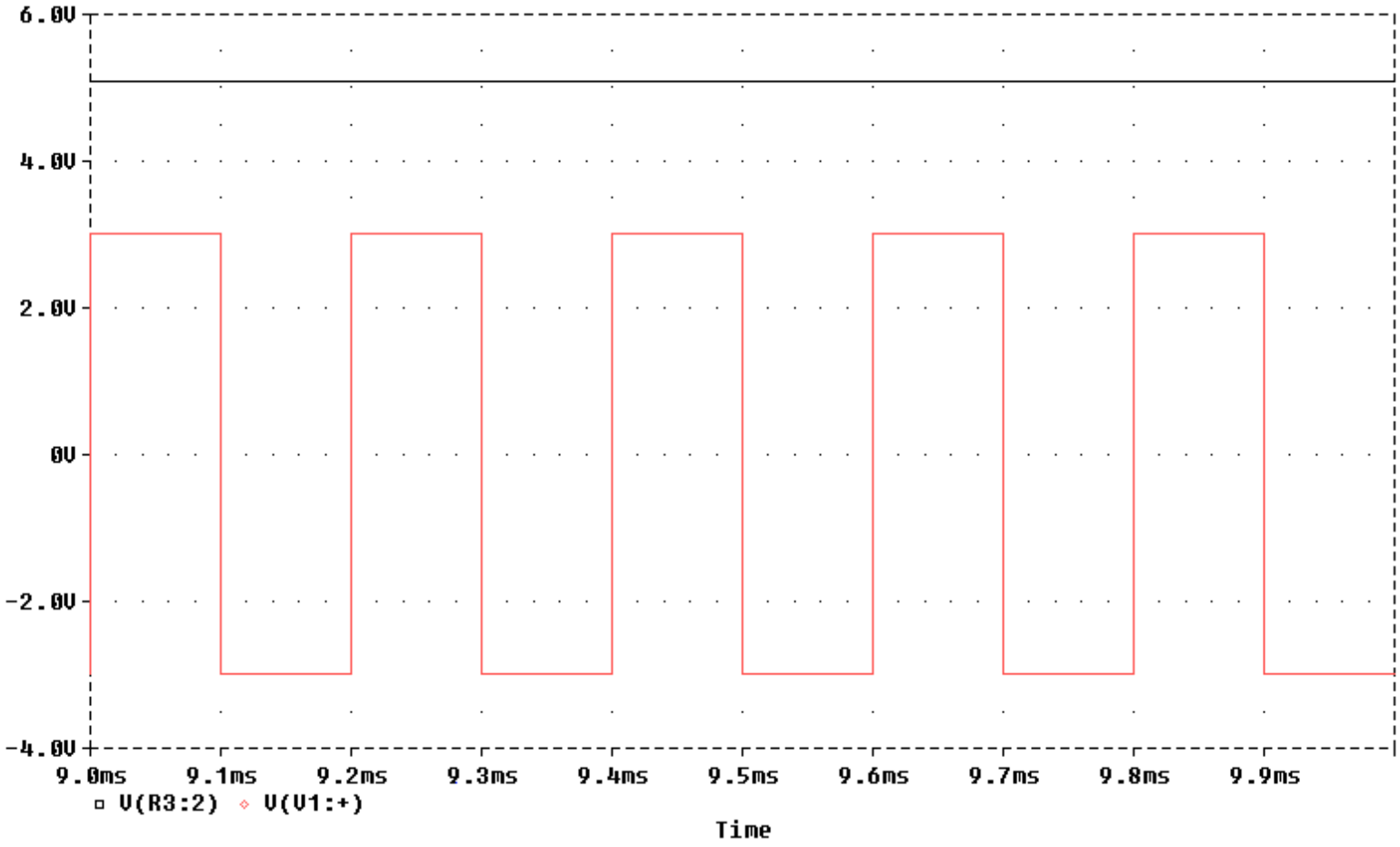
Filenames: bridge1 (IsSpice) bridge3 (Micro-cap) bridge2 (Pspice)

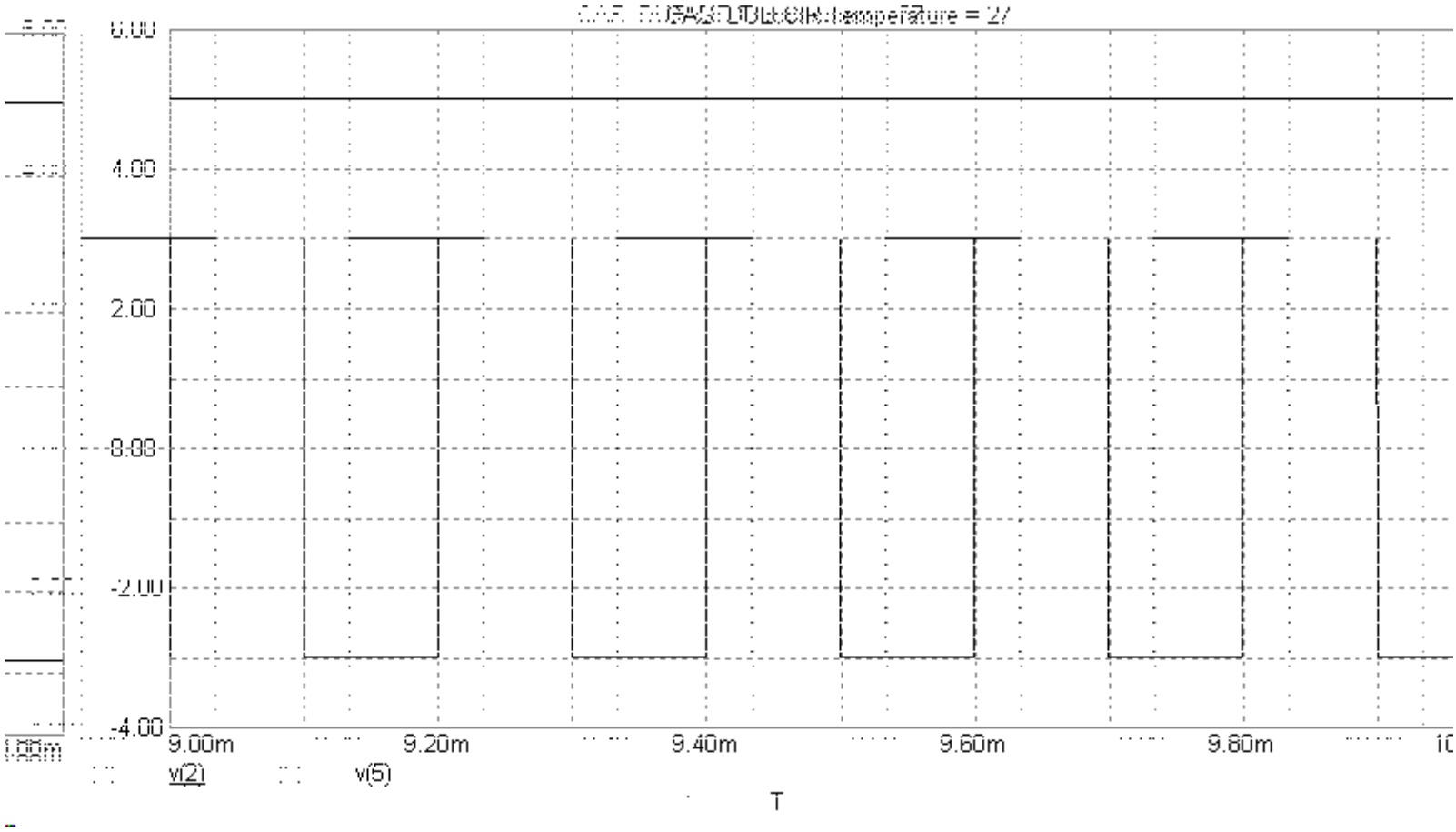

V(4)
OUT
D1
DN4002
R3
100K
V(2)
IN
C1 1uF
2
3
VIN
PULSE
D2
DN4002
C2
1uF


V(4)
OUT
4
D1
DN4002
R3
100K
V(2)
IN
R1 10M
C1 1U
3
8
C2
1U
2
7
VIN
PULSE
+
D2
DN4002
R2
10M


Tek Stop: 500kS/s
81 Acqs
1→
2→
Ch1 2 V Ch2 2 V∿ M 100µs Ch2 ⌊ 360mV
12 Dec 1997
14:05:19


13.00
9.000
5.000
1.000
-3.000
IN in Volts
8.000
4.000
0
-4.000
-8.000
OUT in Volts
X 9.504M
< 5.003 >
2
1
9.100M
9.300M
9.500M
9.700M
9.900M
TIME in Secs


6.0V
4.0V
2.0V
0V
-2.0V
-4.0V
9.0ms
9.1ms
9.2ms
9.3ms
9.4ms
9.5ms
9.6ms
9.7ms
9.8ms
9.9ms
V(R3:2)
V(V1:+)
Time


Temperature = 27
6.00
4.00
2.00
-0.00
-2.00
-4.00
9.00m
9.20m
9.40m
9.60m
9.80m
v(2)
v(5)
T

#48: AC to DC Quadrupler

By connecting two cascade doublers, we can generate a circuit that provides approximately 4 times the AC input voltage as a DC output voltage. The schematic for this circuit is shown in Figure 48-1. The SPICE equivalent circuit is shown in Figure 48-2.

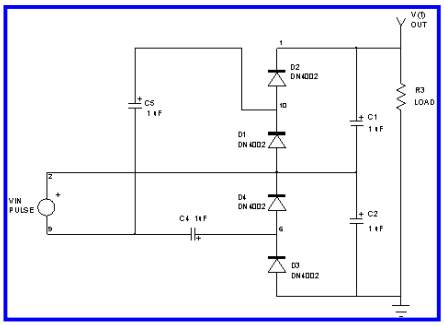


Figure 48-1: Schematic of AC to DC Quadrupler

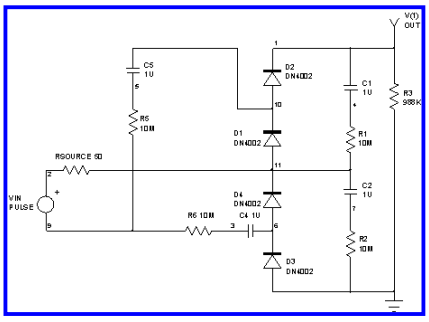


Figure 48-2: SPICE Schematic of AC to DC Quadrupler

Notice in the SPICE circuit (Figure 48-2), the 50 ohm source impedance of the square wave generator is modeled as resistor RSOURCE. The output voltage is dependant on the conduction angle through this resistor, therefore, for the measurements we will make on this circuit, it is important to include this resistance.

The breadboard was constructed and the output voltage was measured using five different loads. The results of the breadboard and the results of each of the three simulators was noted. The result of these measurements is Table 48-1.

Output Voltage Results Summary				
Load [ohms]	Breadboard [volts]	IsSpice [volts]	Pspice [volts]	Microcap [volts]
9.88E+05	10.300	10.130	10.289	10.119
4.00E+05	10.140	10.050	10.210	10.044
2.18E+05	10.020	9.963	10.120	9.962
9.80E+04	9.840	9.795	9.939	9.809
5.49E+04	9.660	9.632	9.760	9.661

Table 48-1: Output voltage comparison between SPICE and breadboard for varying loading

- Breadboard tip: Using an oscilloscope to measure this circuit is tricky. The input signal and output voltage do not share a common ground. A characteristic of most oscilloscopes is that the grounds for each of the probes are tied together internally at the oscilloscope. This prevents plotting real time waveforms on the same screen. If the grounds are tied together, through the oscilloscope probes or otherwise, this circuit will malfunction.

All of the data was collected into Excel and plotted. The resulting plot is shown in Figure 48-3.

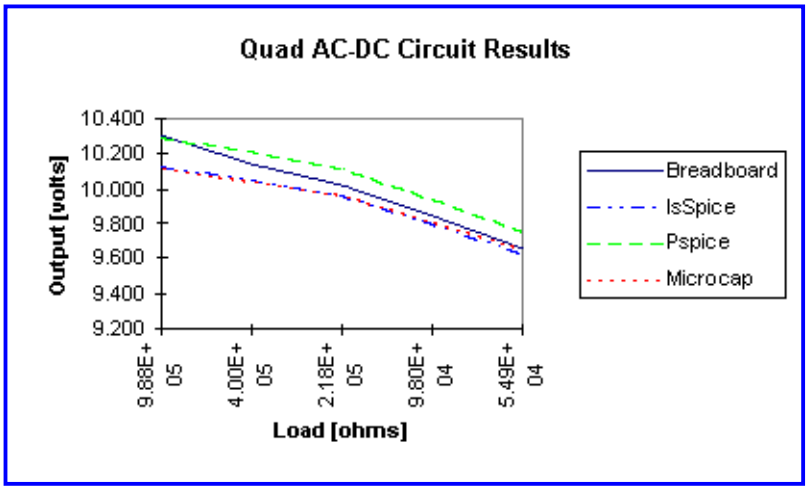


Figure 48-3: DC output voltage results of breadboard and three simulators

Examining Figure 48-3, it is interesting to note the Microcap and IsSpice results are very similar, the Pspice results are slightly higher, and the breadboard data falls in between the simulations. Suspecting the culprit to be the diode models, these were examined more closely. A simple curve tracer circuit was created in each of the simulators. The IsSpice circuit is shown in Figure 48-4. The diode on the left is the IsSpice model, the one on the right is the model Kielkowski created using measurements in his book on component modeling in SPICE [Kielkowski, 1995]. This identical test circuit was also constructed in Pspice and Microcap in order to test the characteristics of the 1N4002 diode in the 10uA to 200uA region. In order to run the DC analysis, the current source was stepped from 10 uA to 200 uA in 10 uA increments. Also, a diode from the actual breadboard circuit was measured at the same points as the SPICE models and added to this graph. The plot of all five results are shown in Figure 48-5.

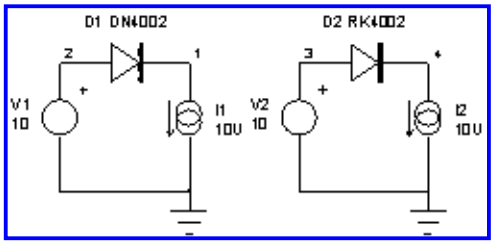


Figure 48-4: IsSpice diode forward characteristics test circuit schematic

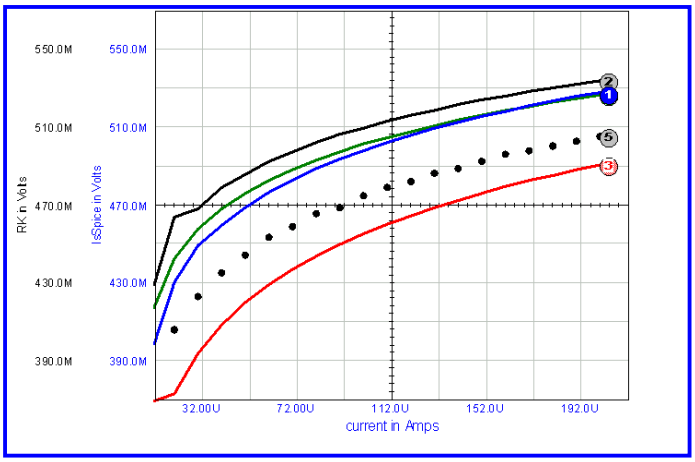


Figure 48-5: Comparison of 1N4002 diode characteristics

In figure 48-5, the traces, from top to bottom, are Ron Kielkowski's model, the Mircocap model, the IsSpice model, the measured data from a 1N4002 from the quadrupler circuit, and the Pspice model. The measured data is the dotted line. All of the diode data is similar. The differences from the breadboard diode, as explained above, are largely due to manufacturing tolerances, different manufacturers, and lot to lot variations. Ron Kielkowski's model was taken from data from an actual 1N4002 diode as well. Figure 48-5 is a good example of how differences in a model does not necessarily mean the model is not correct. It is easy to construct a SPICE compatible diode model that will exactly trace the curve of the breadboard 1N4002, however it would still only be valid for the exact breadboard modeled with that diode.

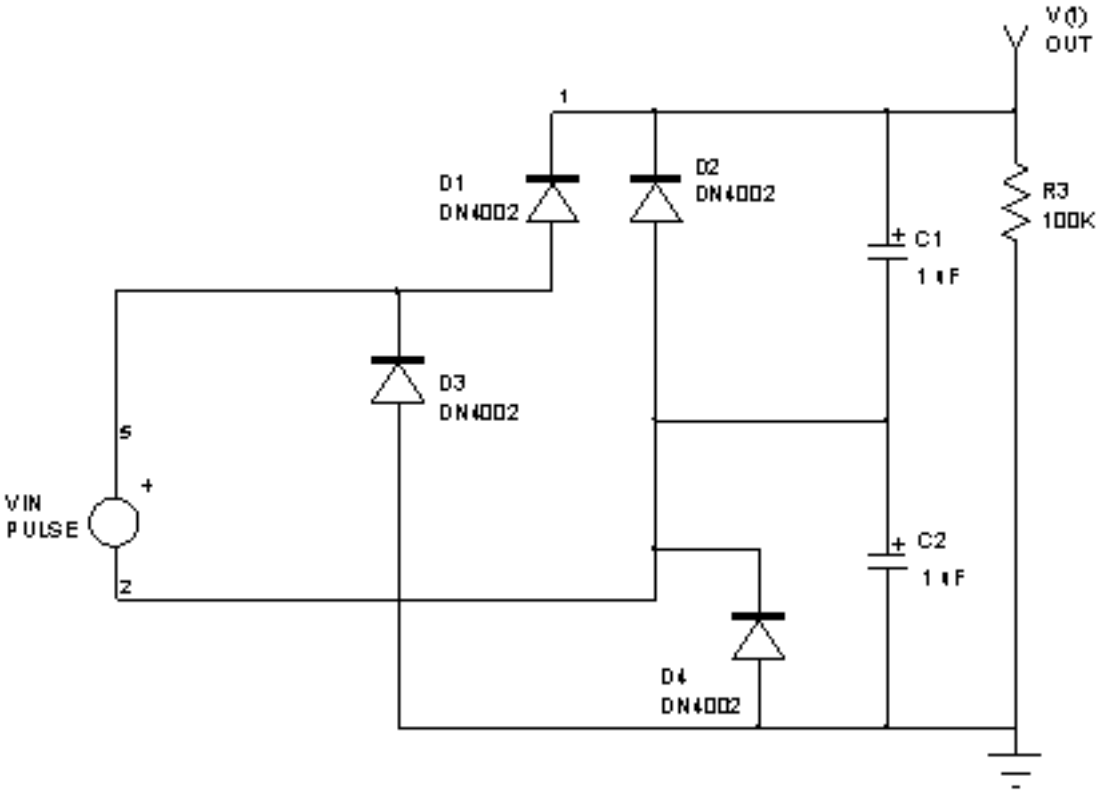
- SPICE tip: To duplicate the ability of plotting the results from three simulators and measured data on one Intuscope plot can be tricky. Each of the three simulators is capable of writing output data directly to a text file. The IsSpice default is in text (*.OUT). To send Pspice data to an output file, use the .PRINT statement in the circuit netlist file. The results will be printed to an *.OUT file which is directly readable by Intuscope (just use the 'Select Source Data...' command under the WAVEFORMS menu)! In Microcap, in the ANALYSIS LIMITS Pop up box, click on the button that enables placing the waveform in the numeric output file (*.TNO). This data can be read by any simple text editor and manipulated such that Intuscope can read it. By the same fashion, lab data can be entered into a text file and read by Intuscope.

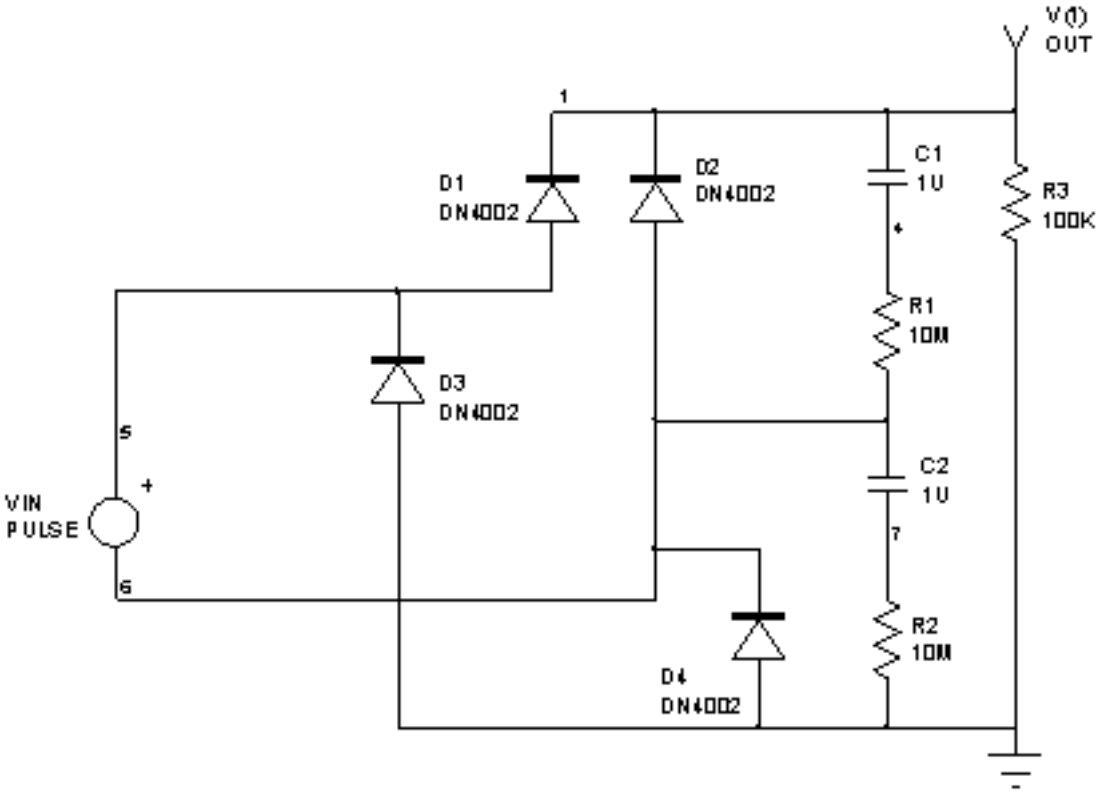
Run Time Summary		
IsSpice v 7.6	PsPice v 6.3	Micro-Cap V v2
40.81 Sec	69.68 Sec	80.12 Sec
Advantages: Low parts count		

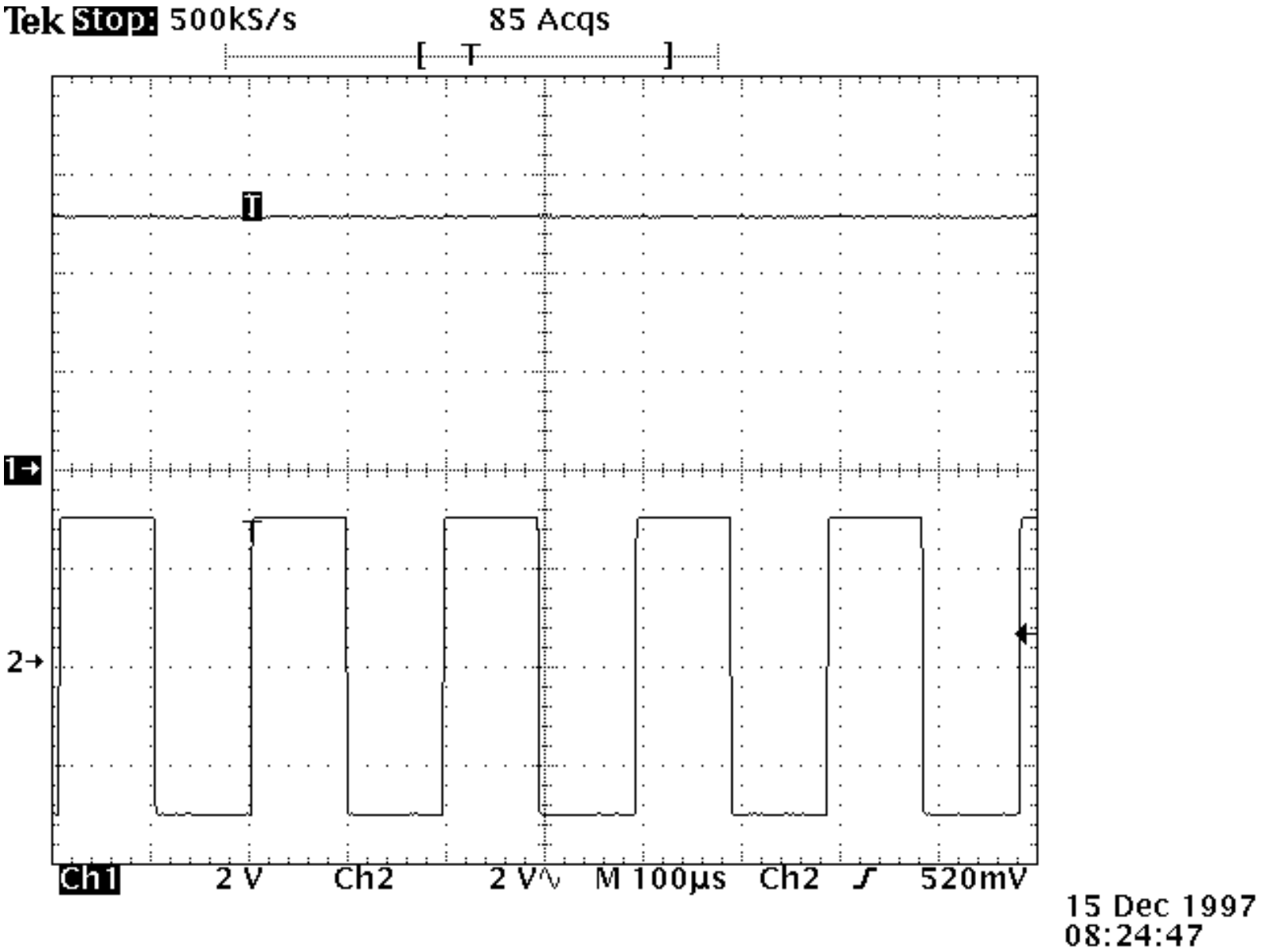
Disadvantages: Current capability limited by source, ripple not as controlled as other topologies, no AC/DC isolation, no regulation.

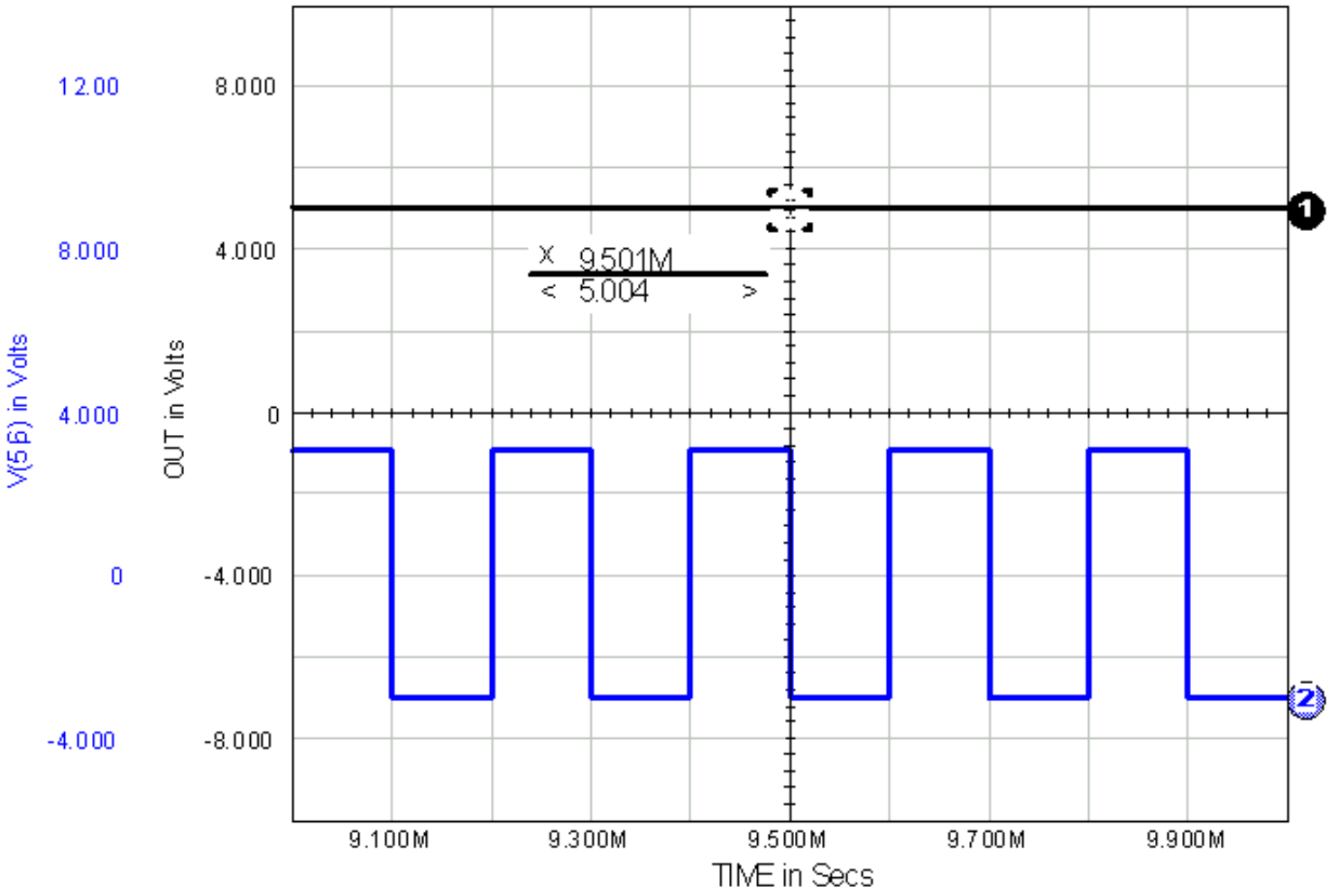
Filenames: quad1 (IsSpice) quad2 (Micro-cap) quad3 (Pspice)

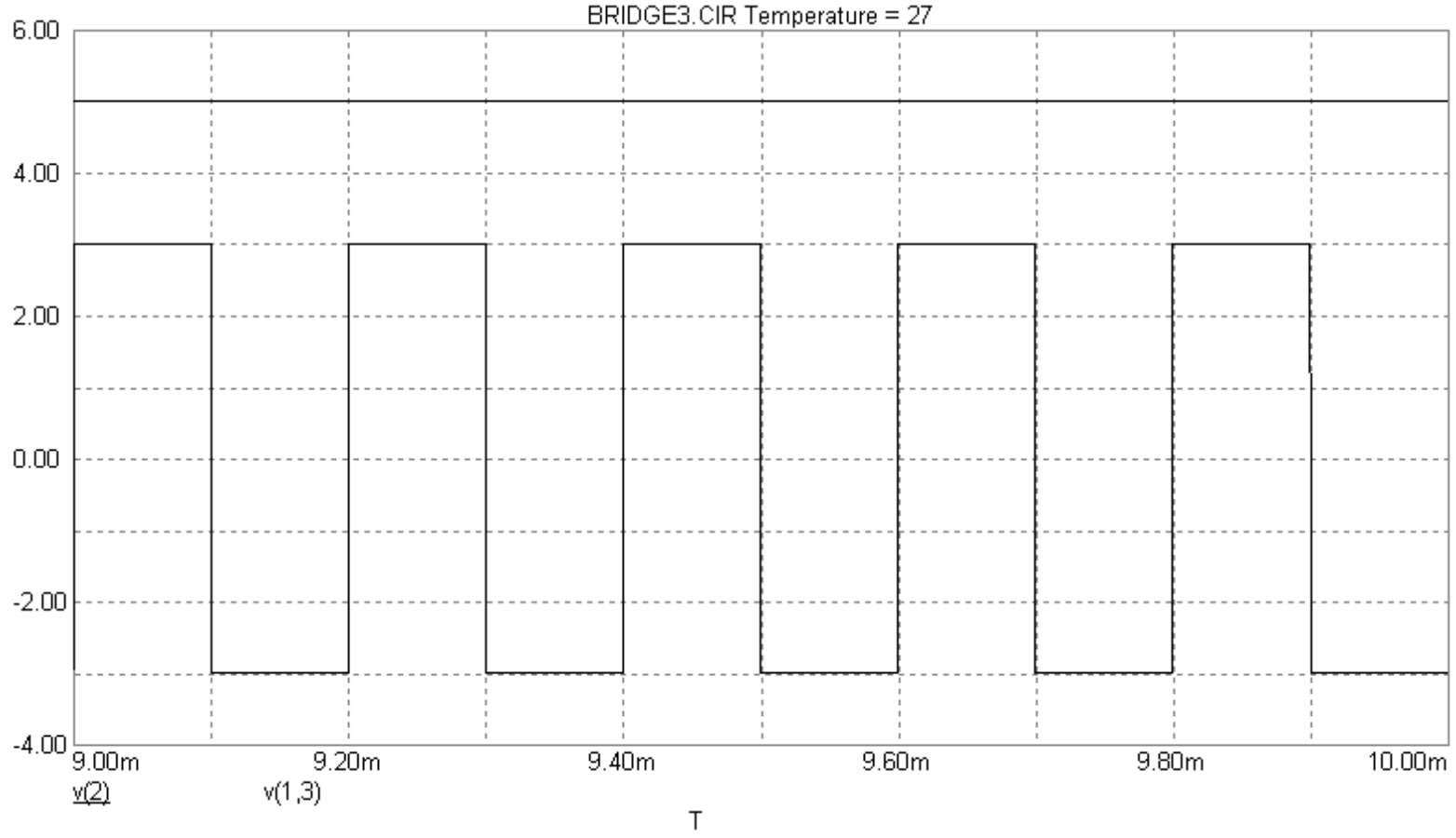
Diode Filenames: 1N4002 (IsSpice) PN4002 (Pspice) MN4002 (Micro-cap) REAL4002 (measured results) quad_res.xls (Excel spreadsheet with results)

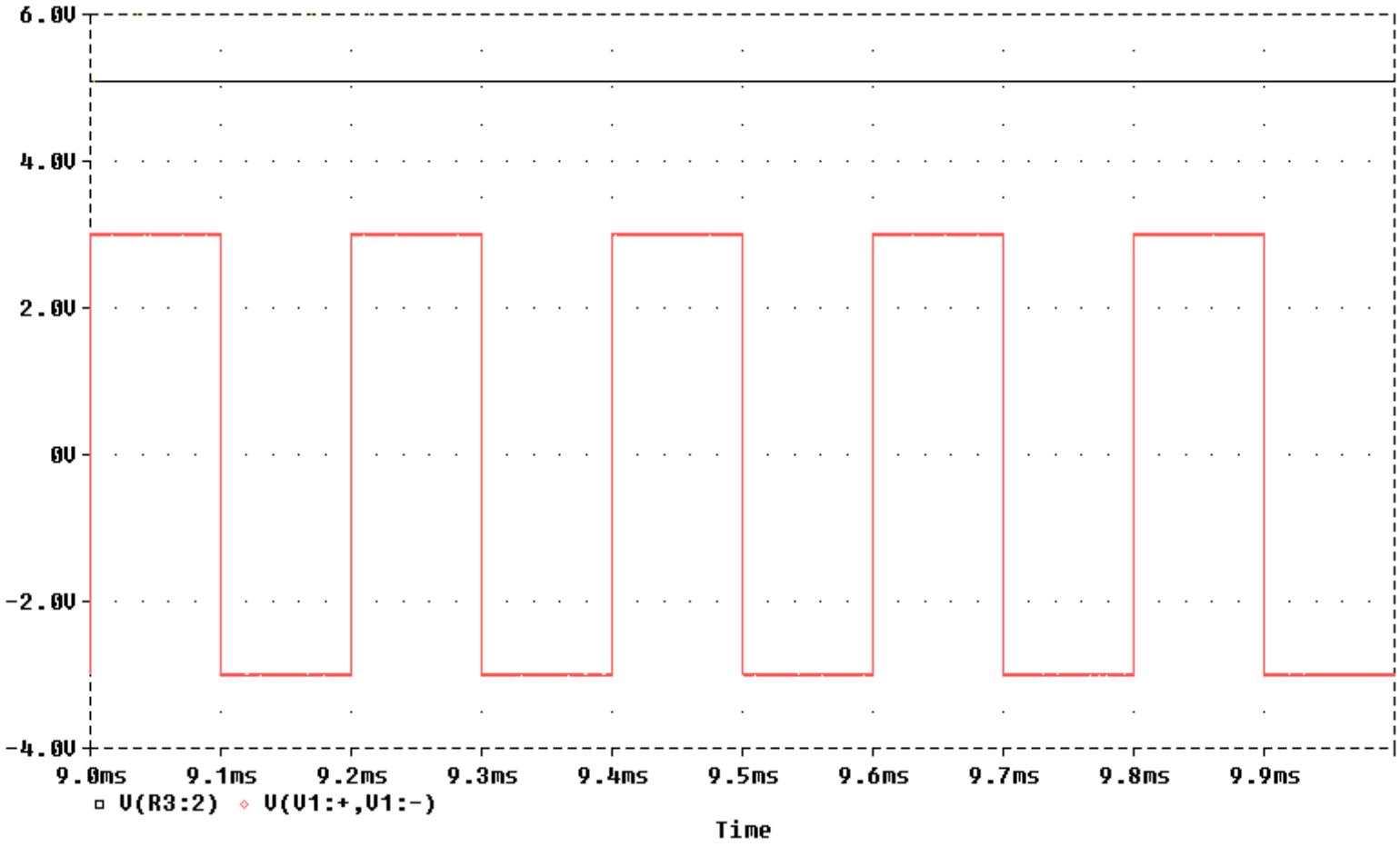

V(1)
OUT
1
D1
DN4002
D2
DN4002
R3
100K
C1
1 uF
D3
DN4002
5
VIN
PULSE
+
2
C2
1 uF
D4
DN4002


V(1)
OUT
1
D1
DN4002
D2
DN4002
C1
1U
R3
100K
4
R1
10M
D3
DN4002
5
VIN
PULSE
+
C2
1U
7
6
R2
10M
D4
DN4002


Tek Stop: 500kS/s
85 Acqs
1→
2→
Ch1 2 V Ch2 2 V∿ M 100µs Ch2 ∫ 520mV
15 Dec 1997
08:24:47


12.00
8.000
4.000
0
-4.000
8.000
4.000
0
-4.000
-8.000
V(5,6) in Volts
OUT in Volts
X 9.501M
< 5.004 >
1
2
9.100M
9.300M
9.500M
9.700M
9.900M
TIME in Secs


BRIDGE3.CIR Temperature = 27
6.00
4.00
2.00
0.00
-2.00
-4.00
9.00m
9.20m
9.40m
9.60m
9.80m
10.00m
v(2)
v(1,3)
T


6.0V
4.0V
2.0V
0V
-2.0V
-4.0V
9.0ms
9.1ms
9.2ms
9.3ms
9.4ms
9.5ms
9.6ms
9.7ms
9.8ms
9.9ms
V(R3:2)
V(V1:+,V1:-)
Time

#49: AC to DC Octupler (x 8)

The final circuit in this family is the AC to DC circuit shown in Figure 49-1. This circuit will create a DC output at 8 times the AC value. This circuit is very flexible. By increasing the number of diode capacitor stages, very high DC voltages can be reached using a 50 ohm function generator. Just as in the previous circuits of this chapter, it polarized capacitors are used, the polarity must be in the proper direction. Although the polarity is not shown in Figure 49-1, the capacitors from left to right are all negative to positive.

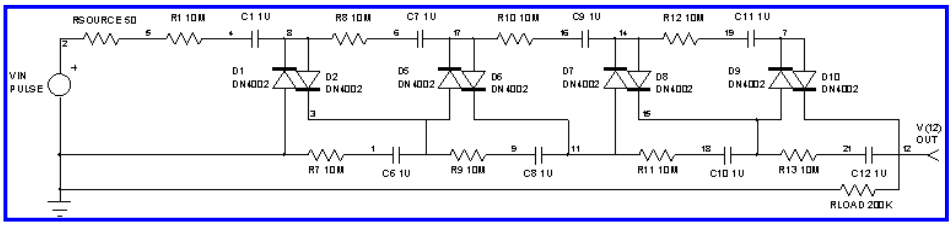


Figure 49-1: AC to DC Octupler circuit (x8)

The pulse, as before, was ± 3 volt square wave at 5 Khz with a 50% duty cycle. The resulting input waveform and output waveform from the breadboard is shown in Figure 49-2. An AC coupled expanded view of the output (and the ripple) is shown in Figure 49-3.

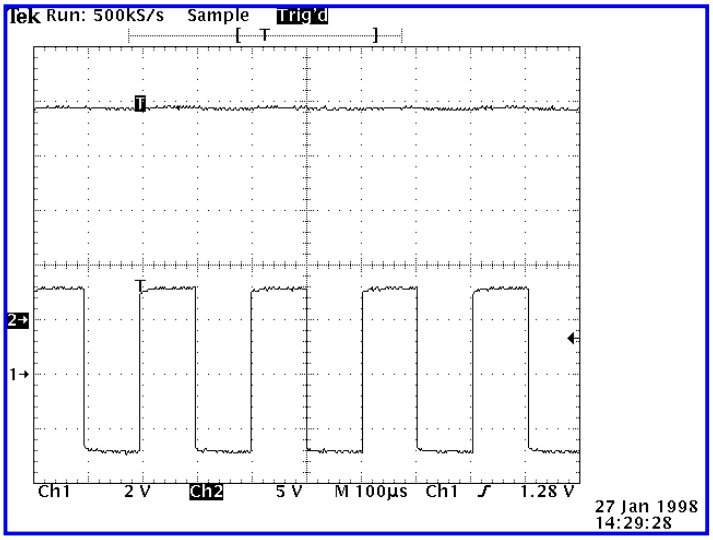


Figure 49-2: Breadboard input and output waveforms

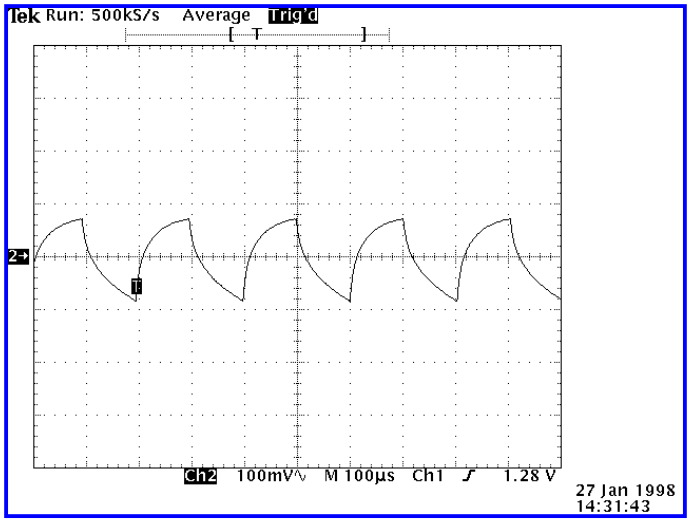


Figure 49-3: Breadboard output waveform (expanded scale)

The load at this condition was 200 Kohm. The results of the IsSpice simulations were very similar to the breadboard results, especially the output ripple in Figure 49-5.

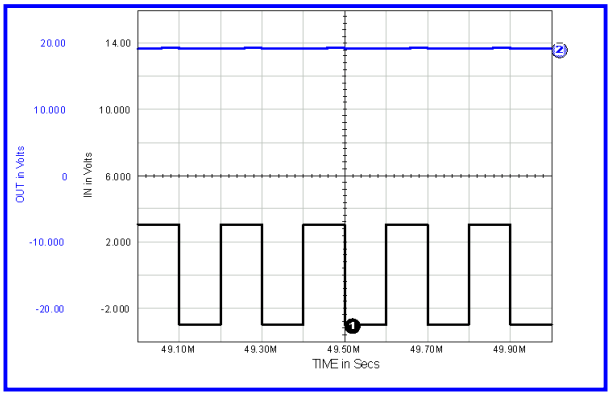


Figure 49-4: IsSpice input and output waveforms

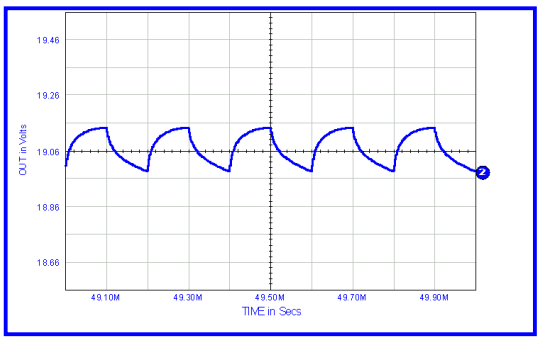


Figure 49-5: IsSpice output waveform (expanded)

The octupler circuit was simulated in all three simulators at three different loading conditions. The results of the ripple of the Pspice and Microcap simulations (at a load of 200 Kohm) are shown in Figures 49-6 and 49-7. The results of the DC output voltage of all three simulators and the breadboard at several loading conditions are shown in Table 49-1.

AC to DC Octupler (x 8)

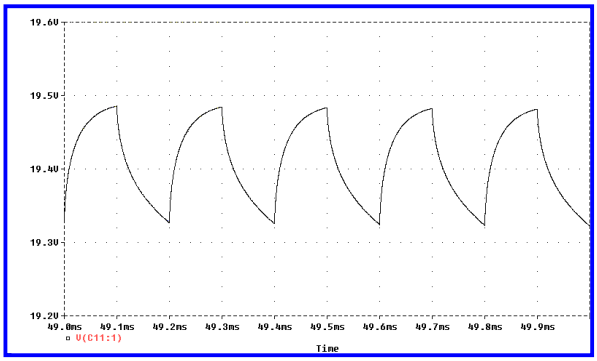


Figure 49-6: Pspice output waveform (expanded)

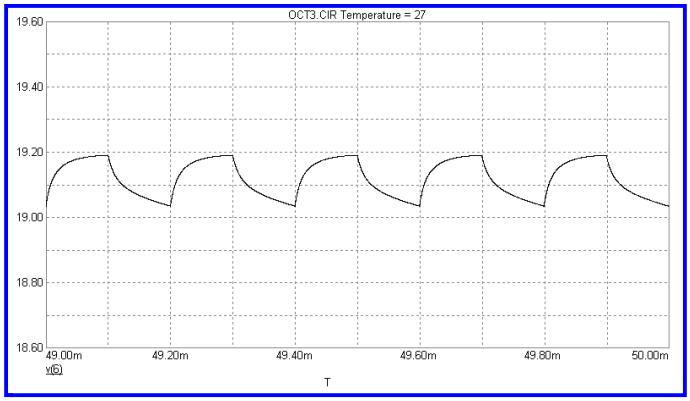


Figure 49-7: Microcap output waveform (expanded)

Output Voltage Results Summary				
Load [ohms]	Breadboard [volts]	IsSpice [volts]	Pspice [volts]	Microcap [volts]
9.88E+05	20.2	20.172	20.569	20.144
4.00E+05	19.75	19.683	20.027	19.686
2.18E+05	19.31	19.071	19.406	19.110

Table 49-1: Output Voltage Results summary of Octupler AC to DC circuit

The measurements for the output ripple at a load of 200 Kohm for each of the simulators and the breadboard was also summarized in table 49-2.

Output Voltage Results Summary				
Breadboard	IsSpice	Pspice	Microcap	Units
155	159	86	35	mV pk-pk

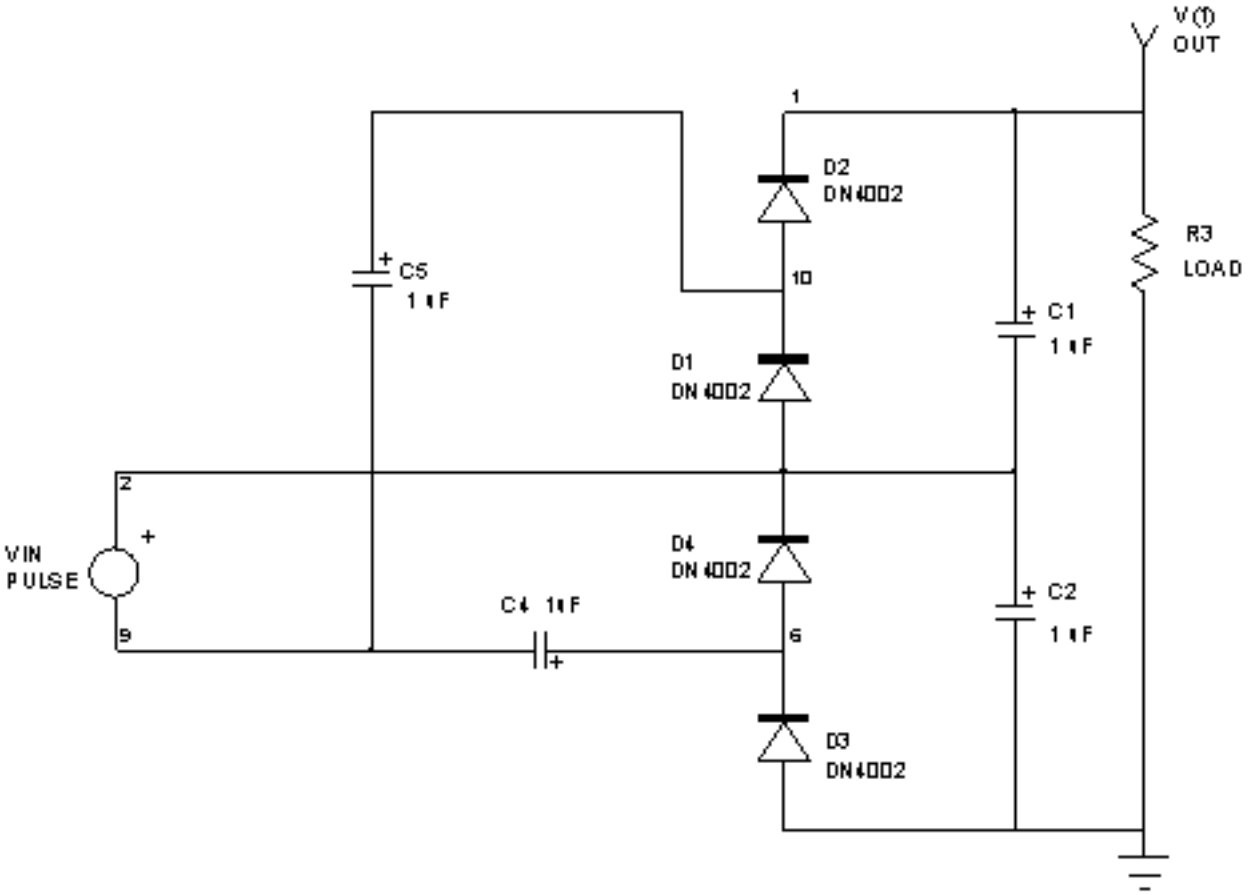
Table 49-2: Output Ripple Results summary of Octupler AC to DC circuit

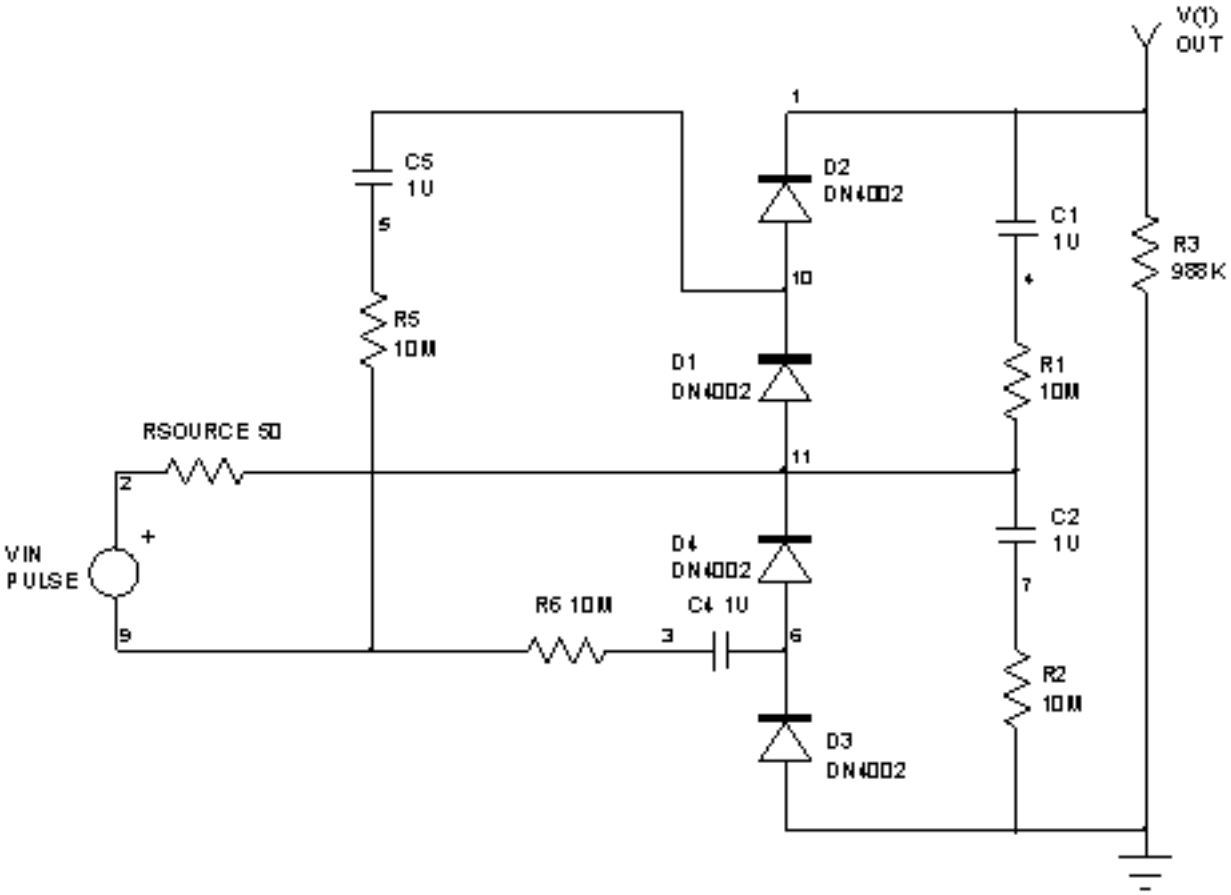
Run Time Summary		
IsSpice v 7.6	PsPice v 6.3	Micro-Cap V v2
590.23 Sec	908.59 Sec	1105.92 Sec

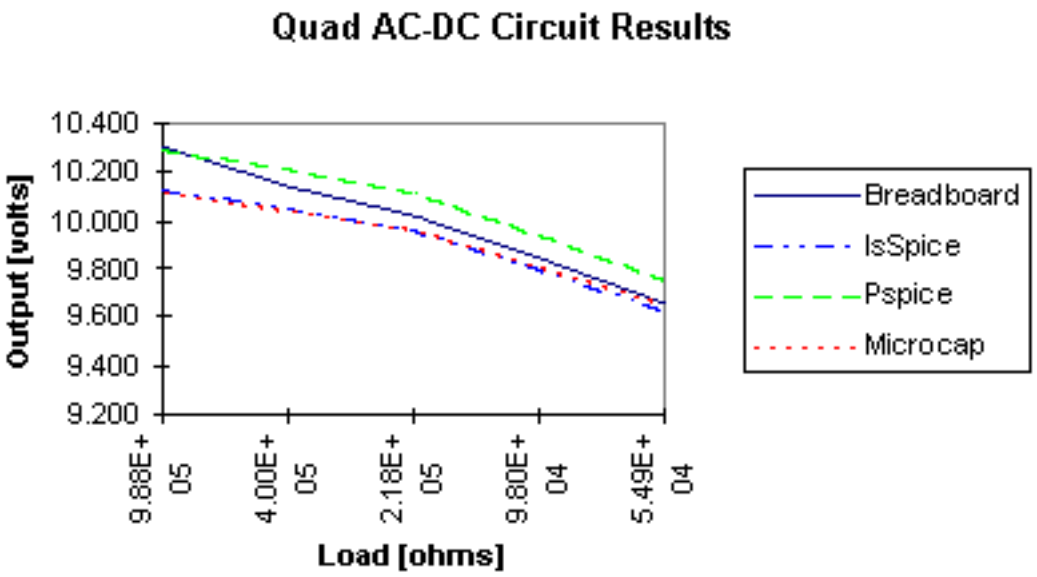
AC to DC Octupler (x 8)

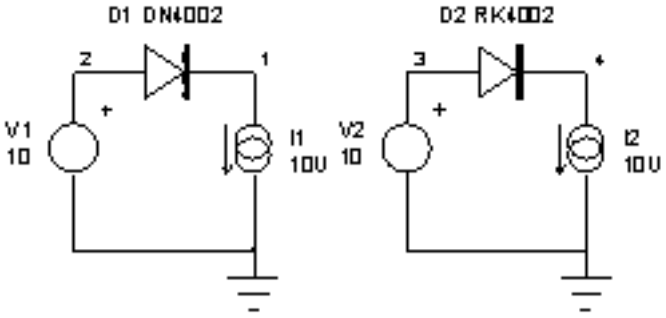
Advantages: Low parts count
Disadvantages: Current capability limited by source, ripple not as controlled as other topologies, no AC/DC isolation, no regulation.

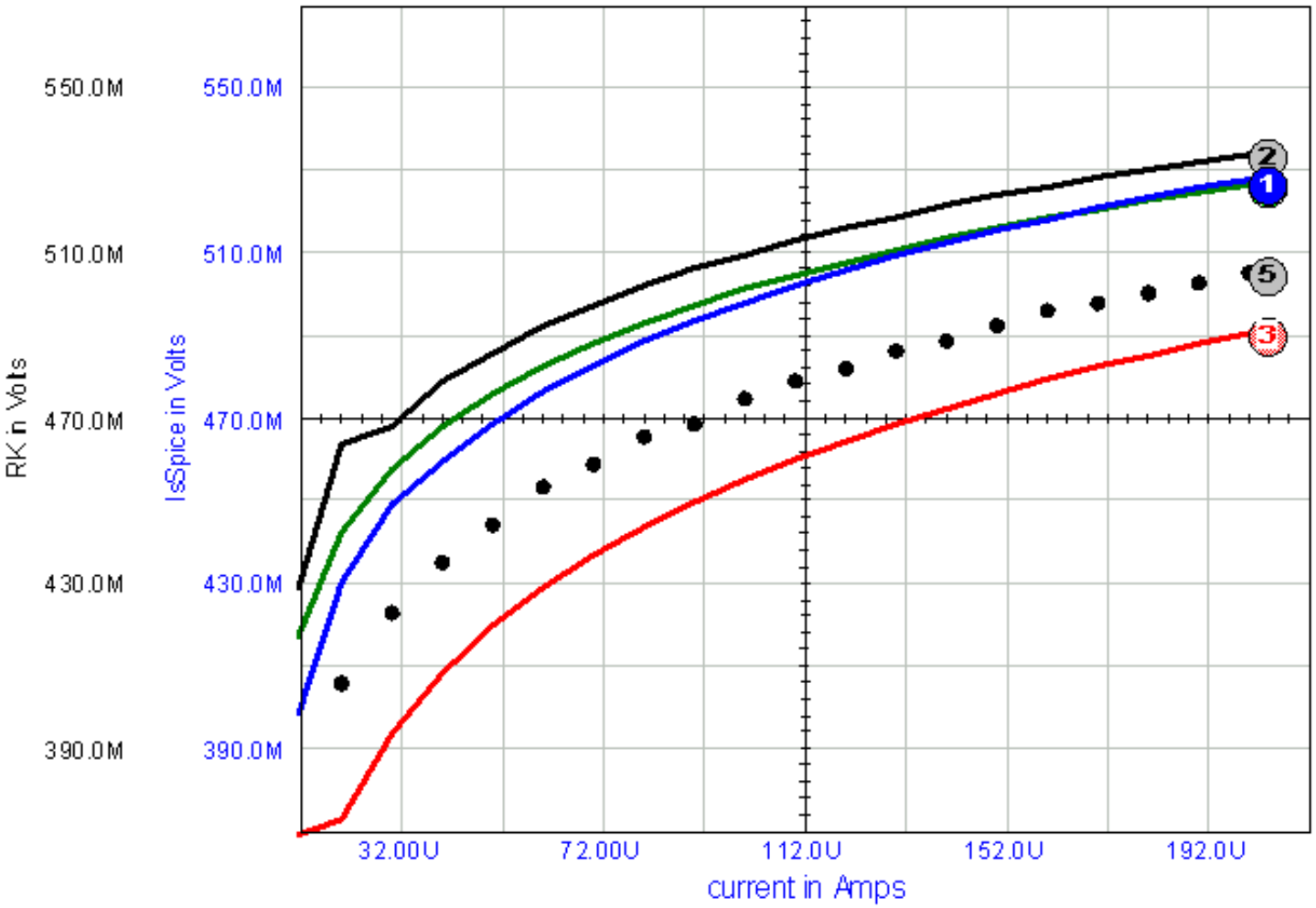
Filenames: oct1 (IsSpice) oct2 (Micro-cap) oct3 (Pspice)


V(1)
OUT
1
D2
DN4002
R3
LOAD
C5
1 µF
10
C1
1 µF
D1
DN4002
2
D4
DN4002
VIN
PULSE
C4 1µF
C2
1 µF
9
6
D3
DN4002


V(1)
OUT
1
C5
1U
5
R5
10M
D2
DN4002
C1
1U
R3
988K
10
4
D1
DN4002
R1
10M
RSOURCE 50
11
2
C2
1U
+
VIN
PULSE
D4
DN4002
7
R6 10M
C4 1U
9
3
6
R2
10M
D3
DN4002


Quad AC-DC Circuit Results
Output [volts]
10.400
10.200
10.000
9.800
9.600
9.400
9.200
9.88E+05
4.00E+05
2.18E+05
9.80E+04
5.49E+04
Load [ohms]
Breadboard
IsSpice
Pspice
Microcap


D1 DN4002
2
1
+
V1
10
I1
10U
D2 RK4002
3
4
+
V2
10
I2
10U


550.0M
510.0M
470.0M
430.0M
390.0M
RK in Volts
550.0M
510.0M
470.0M
430.0M
390.0M
IsSpice in Volts
32.00U
72.00U
112.0U
152.0U
192.0U
current in Amps
2
1
5
3

#50: High voltage, High Current DC to DC doubler

Some of the doubler circuits presented in this chapter have limited current and voltage capabilities. The circuit presented here contains neither of those limitations. The complete breadboard schematic for this circuit is shown in Figure 50-1.

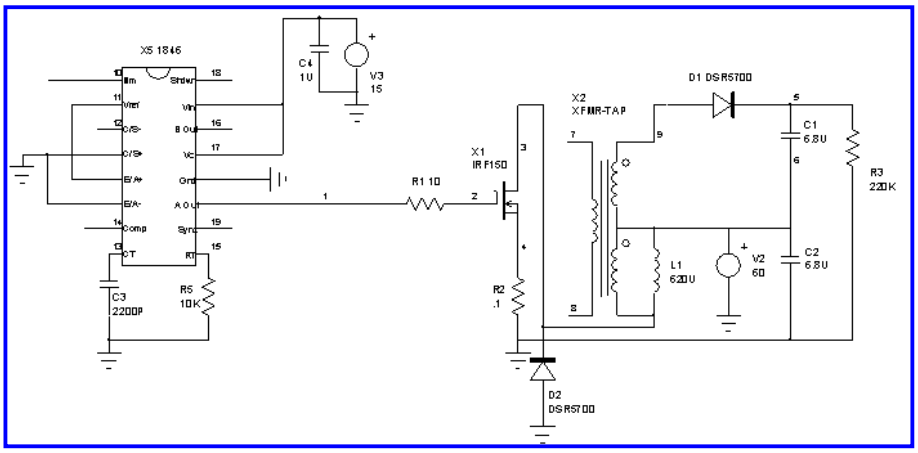


Figure 50-1: DC to DC doubler circuit schematic

Notice the breadboard circuit utilizes an 1846 gate driver circuit described in detail in Chapter 11. The 1846 circuit generates a 0 to 15 volt square wave pulse at 50 Khz with a 50 % duty cycle. This circuit is able to provide enough current to adequately drive the Mosfet. This particular configuration takes a 60 Volt DC signal and doubles the voltage to 120 Volts. The 60 volts is switched by an IRF150 Mosfet and rectified by diode D1. The 60 volts switched signal now appears at capacitor C1 superimposed on the 60 volt signal of capacitor C2, thus generating a 120 Vdc signal. Resistor R9 is a pre-load resistor that keeps the doubler from attempting to operate without a load.

The equivalent SPICE model circuit of the breadboard is shown in Figure 50-2. The most drastic difference is the 1846 circuit has been replaced with a pulsed voltage source. R4 (100 Meg Resistor) was added to the unconnected lead of the transformer to aid convergence. Leakage inductance and DCR of the main transformer was also added (L_Lk, R_LDCR). A 75 Watt light bulb was used as the load in the breadboard. In order to model this light bulb, resistor R_PLOAD was added.

- SPICE TIP: To allow this circuit to converge, the ABSTOL setting in the OPTIONS call line was modified from 1p (default) to 1U. This

was required on all three simulation programs. The UIC statement was also used on the .TRAN line. Initial conditions were set on the output capacitors (60 volts on each).

- SPICE TIP: Although the DSR5700 high speed rectifying diode was used in the breadboard, there was no SPICE model for it. The 1N5806 was used as a substitute in the SPICE model, even though the voltage rating of the 1N5806 is not optimal.

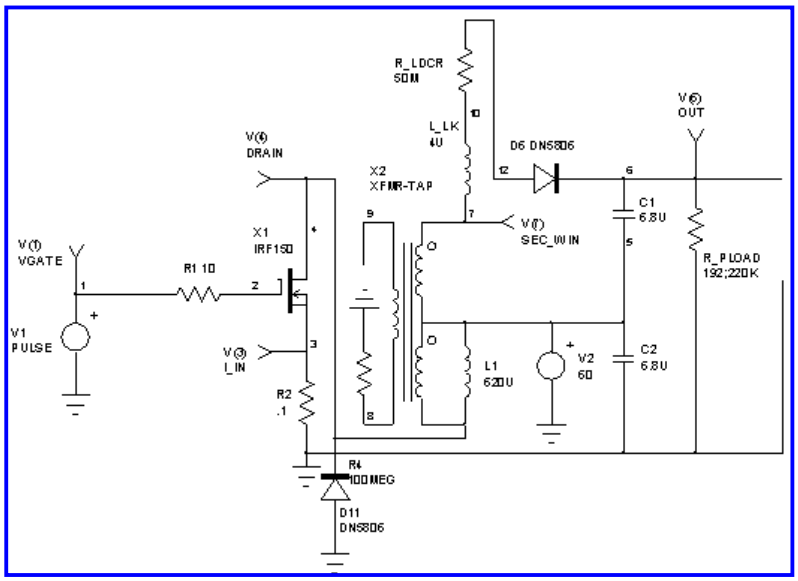


Figure 50-2: DC to DC doubler circuit SPICE equivalent schematic

Several waveforms of this circuit were measured for comparison to SPICE results. The voltage at the anode of diode D6 in Figure 50-2 was compared to the gate voltage waveform, shown below in Figure 50-3A. The voltage (a representation of the switch current) across the sense resistor R2 was also measured and is shown in Figure 50-4. The results from the IsSpice simulations are shown in Figure 50-3B and 50-5.

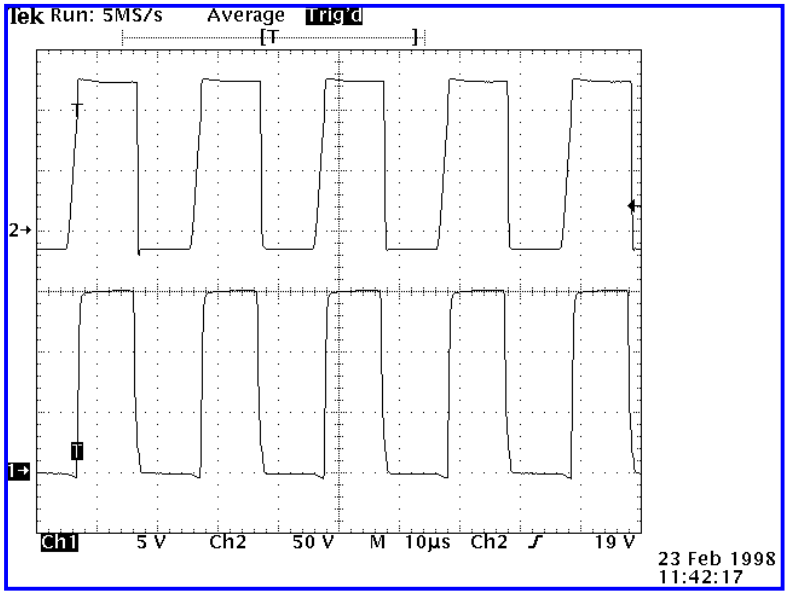


Figure 50-3A: Breadboard results (top-Anode of D6, Bottom - Gate voltage)

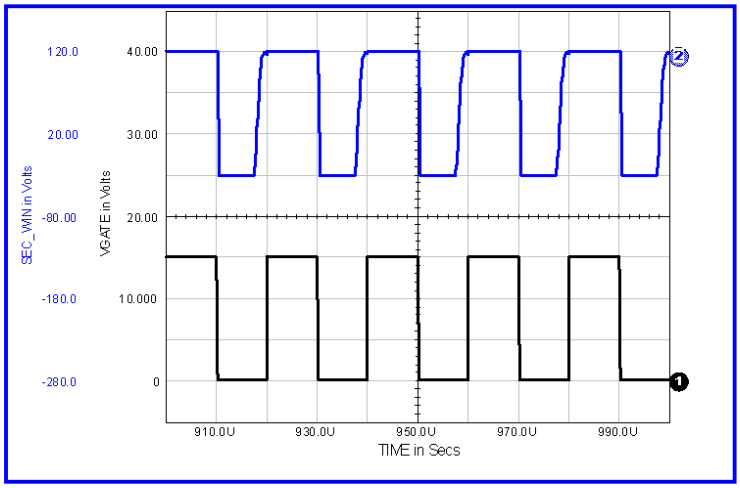


Figure 50-3B: IsSpice results (top-Anode of D6, Bottom - Gate voltage)

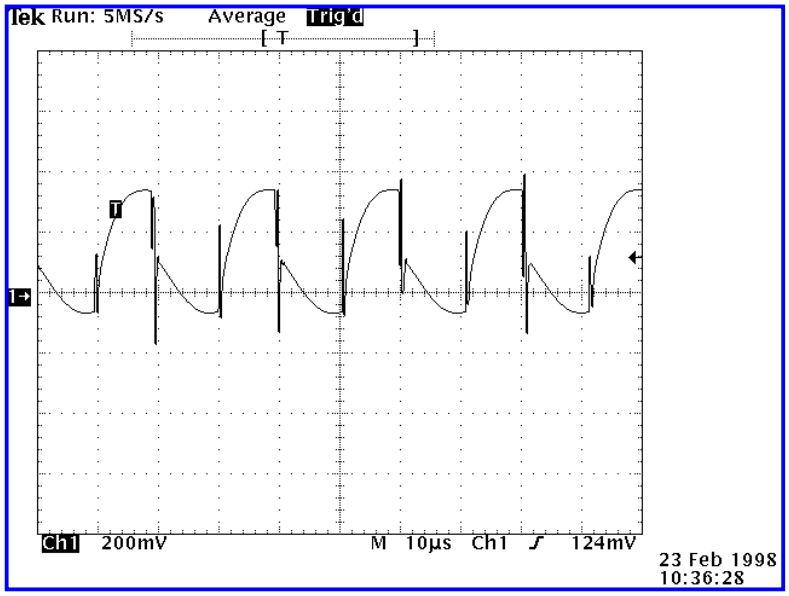


Figure 50-4: Breadboard results (switch current)

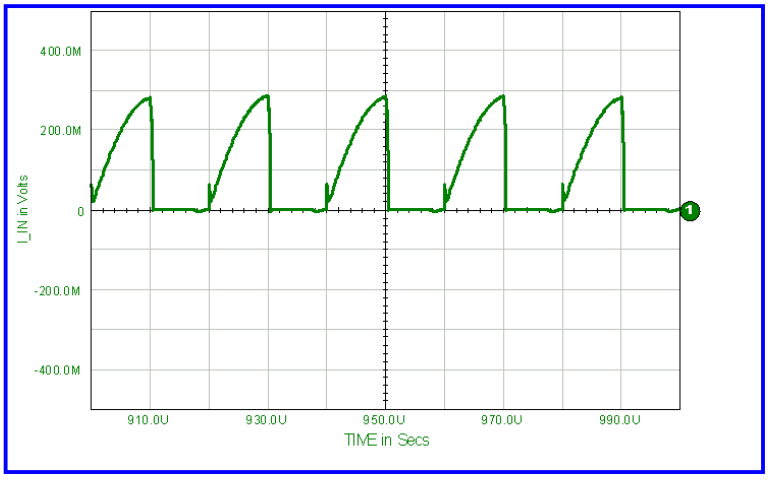


Figure 50-5: IsSpice results (switch current)

The circuit was also simulated using Pspice and Microcap. The Pspice results are shown in Figure 50-6A and 50-6B while the Microcap results are shown in Figure 50-7A and 50-7B.

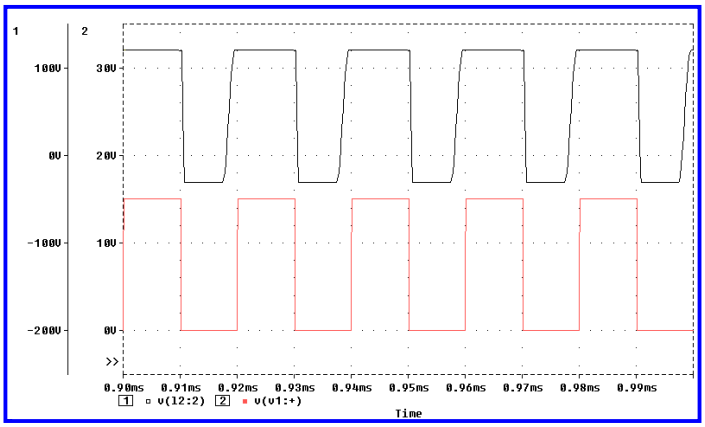


Figure 50-6A: Pspice results (top-Anode of D6, Bottom - Gate voltage)

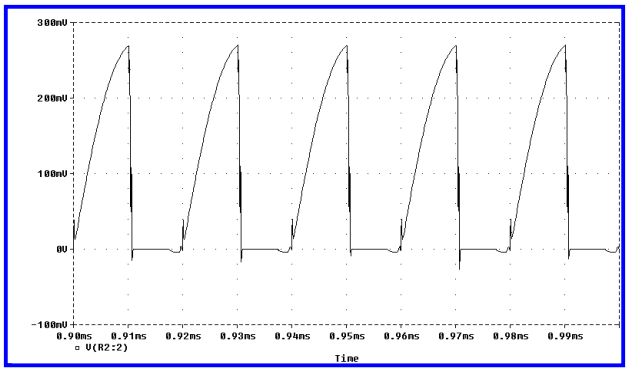


Figure 50-6B: Pspice results (switch current)

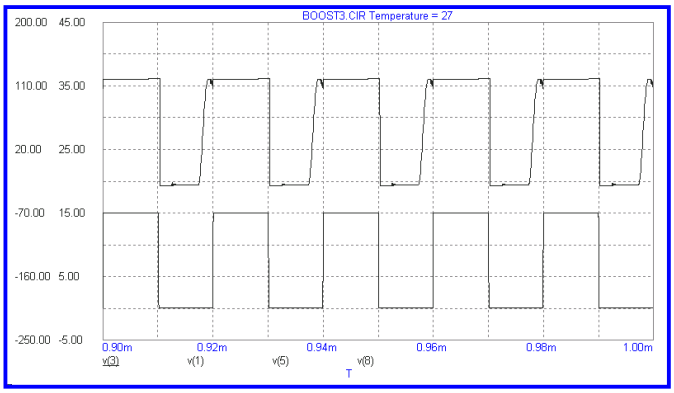


Figure 50-7A: Microcap results (top-Anode of D6, Bottom - Gate voltage)

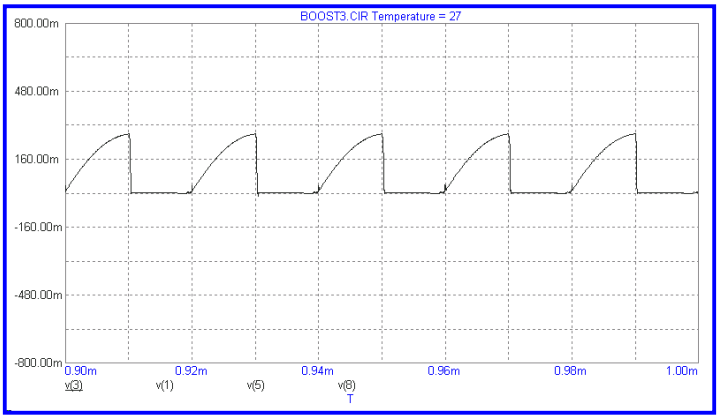


Figure 50-7B: Microcap results (switch current)

- SPICE TIP: In the Microcap simulation, the model for the IRF140 Mosfet was substituted for the IRF150 Mosfet. The IRF150 Mosfet model showed an unusually long turn off time which is believed to be in error.

Run Time Summary		
IsSpice v 7.6	PsPice v 6.3	Micro-Cap V v2
128.55 Sec	118.96 Sec	86.4 Sec
Advantages: medium parts count, good voltage and current range, good way to increase the voltage range of lab power supplies.		
Disadvantages: No isolation from input to output , no automatic line and load regulation		

Filenames:boost1 (IsSpice) Boost2 (Pspice) Boost3 (Microcap)

References

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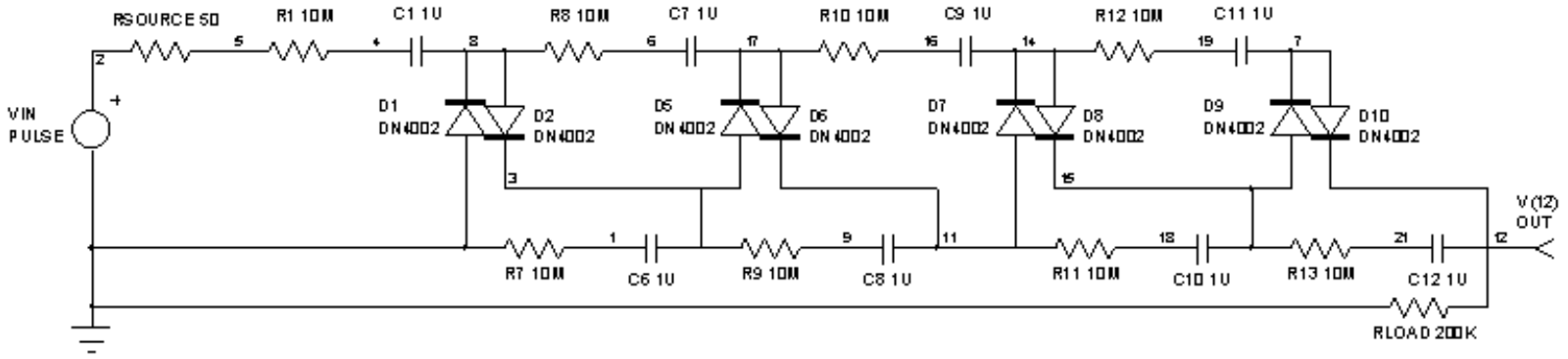
Mimms, Forrest M. III, 1983. Getting Started In Electronics.

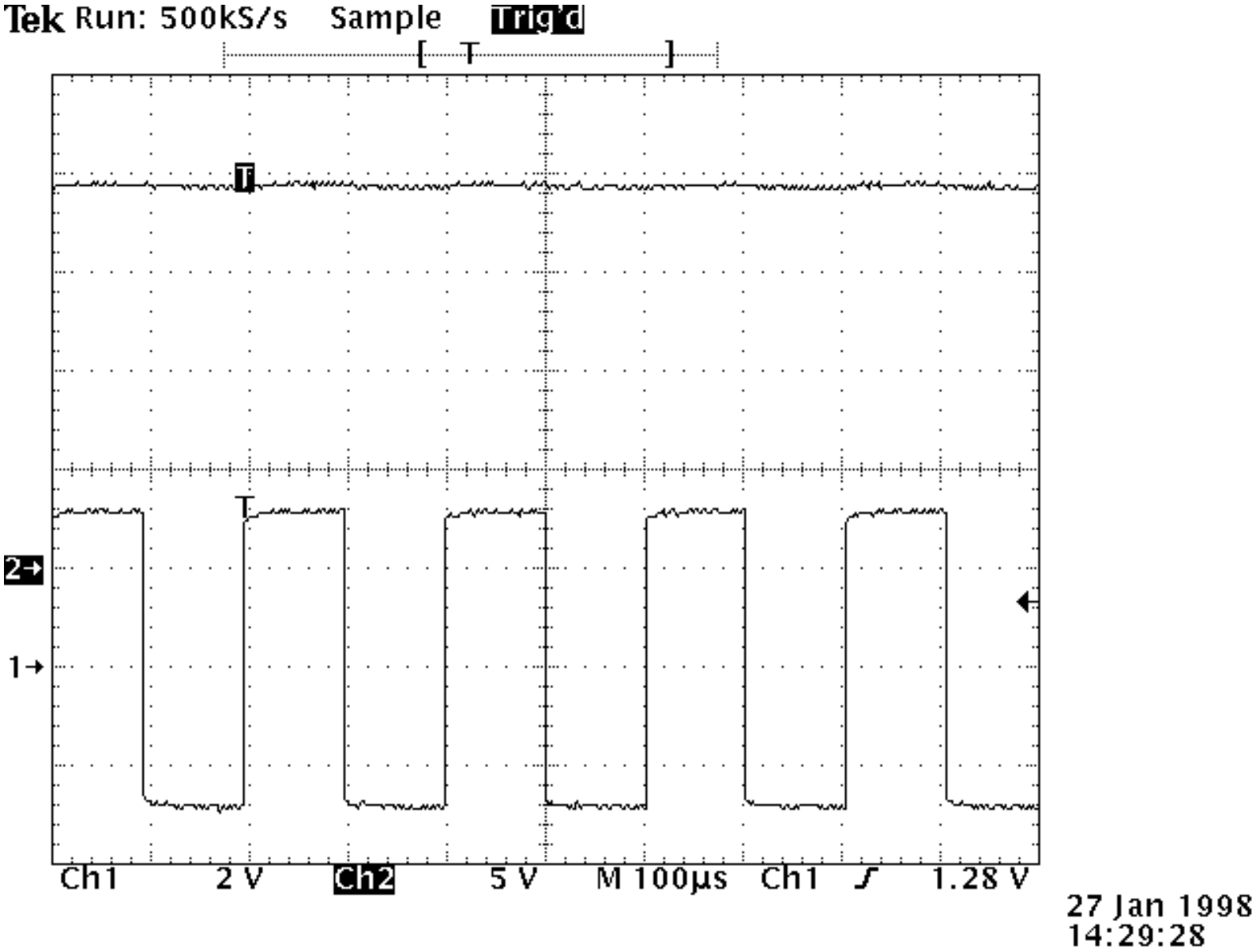
Parker, Sybil, ed. 1984. Concise Encyclopedia of Science and Technology. New York: McGraw Hill

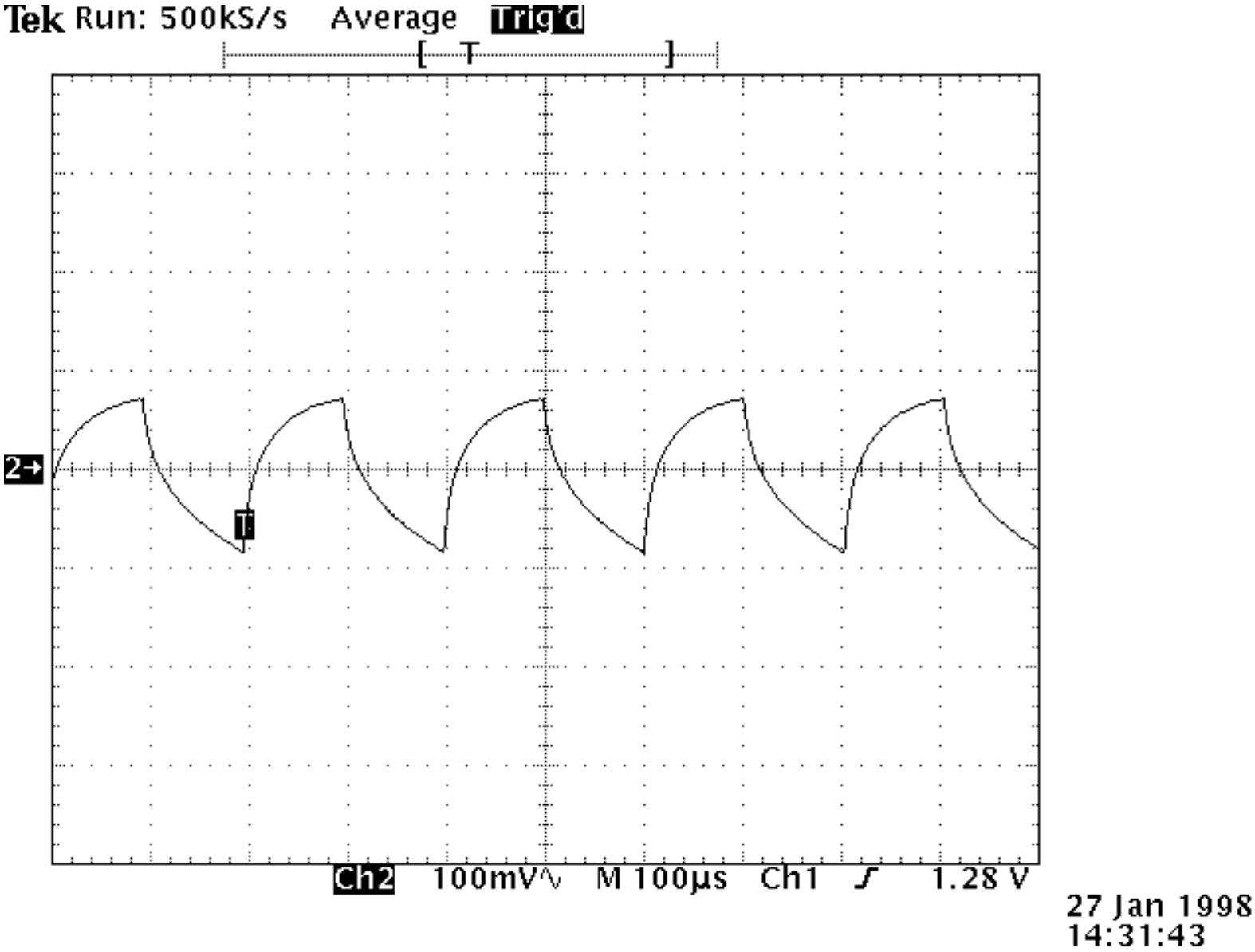
Power IC's Databook, National Semiconductor. 1993.

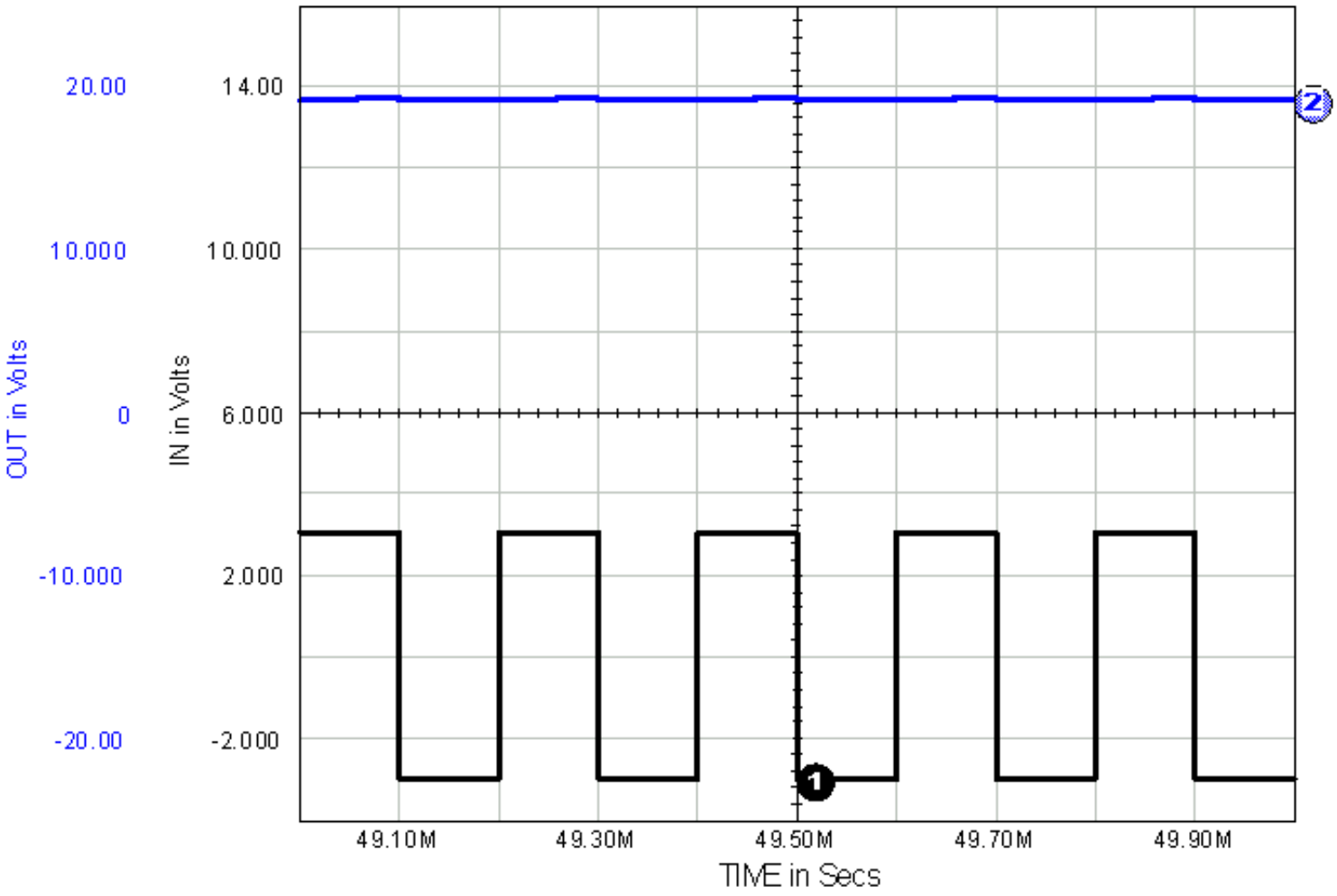
Sandler, Steven M. SMPS Simulation with SPICE. 1996. McGraw Hill.

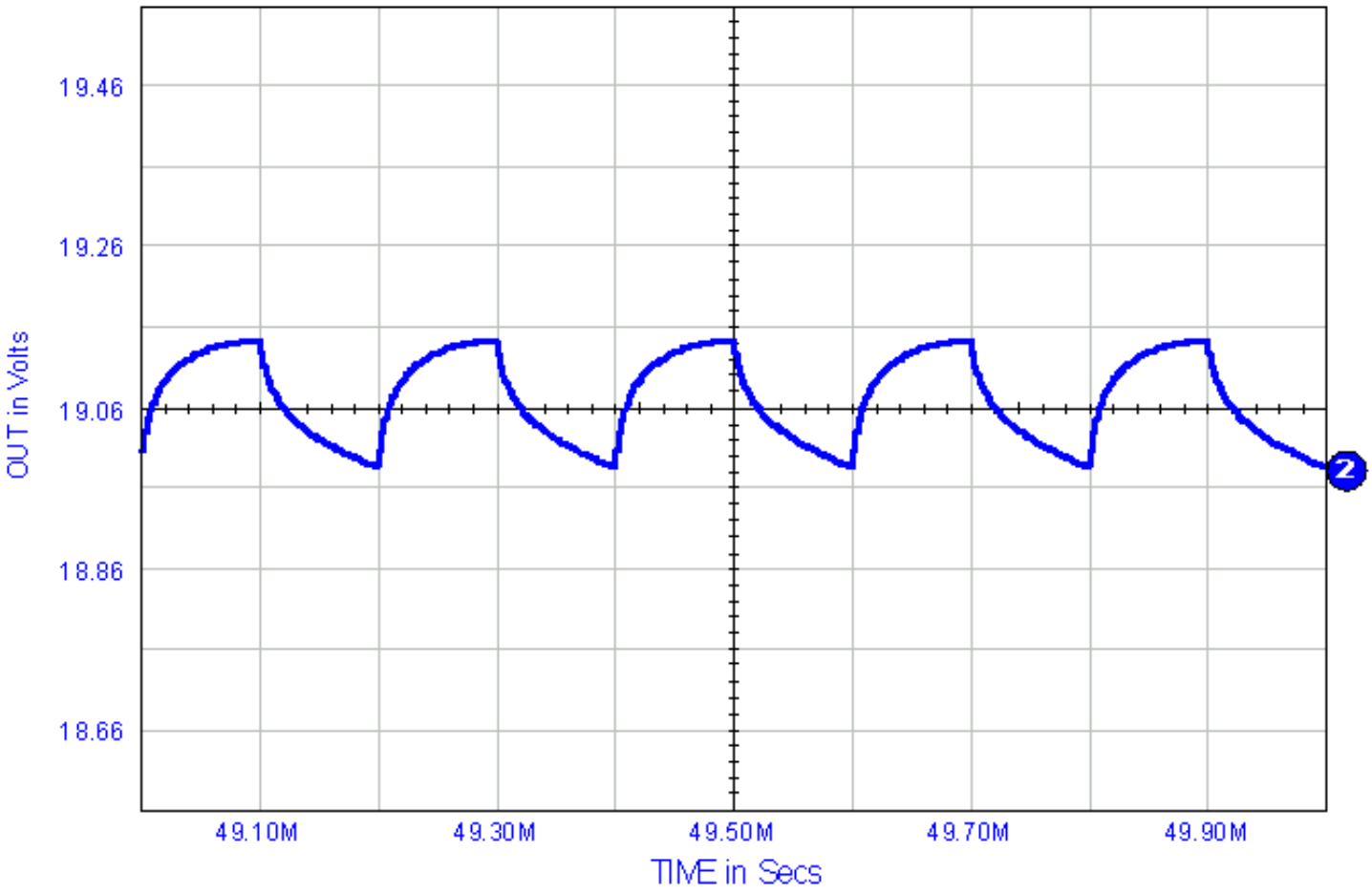
Van Valkenburg, M.E. 1982. Analog Filter Design. New York: Harcort Brace Jovanovich College Publishers.

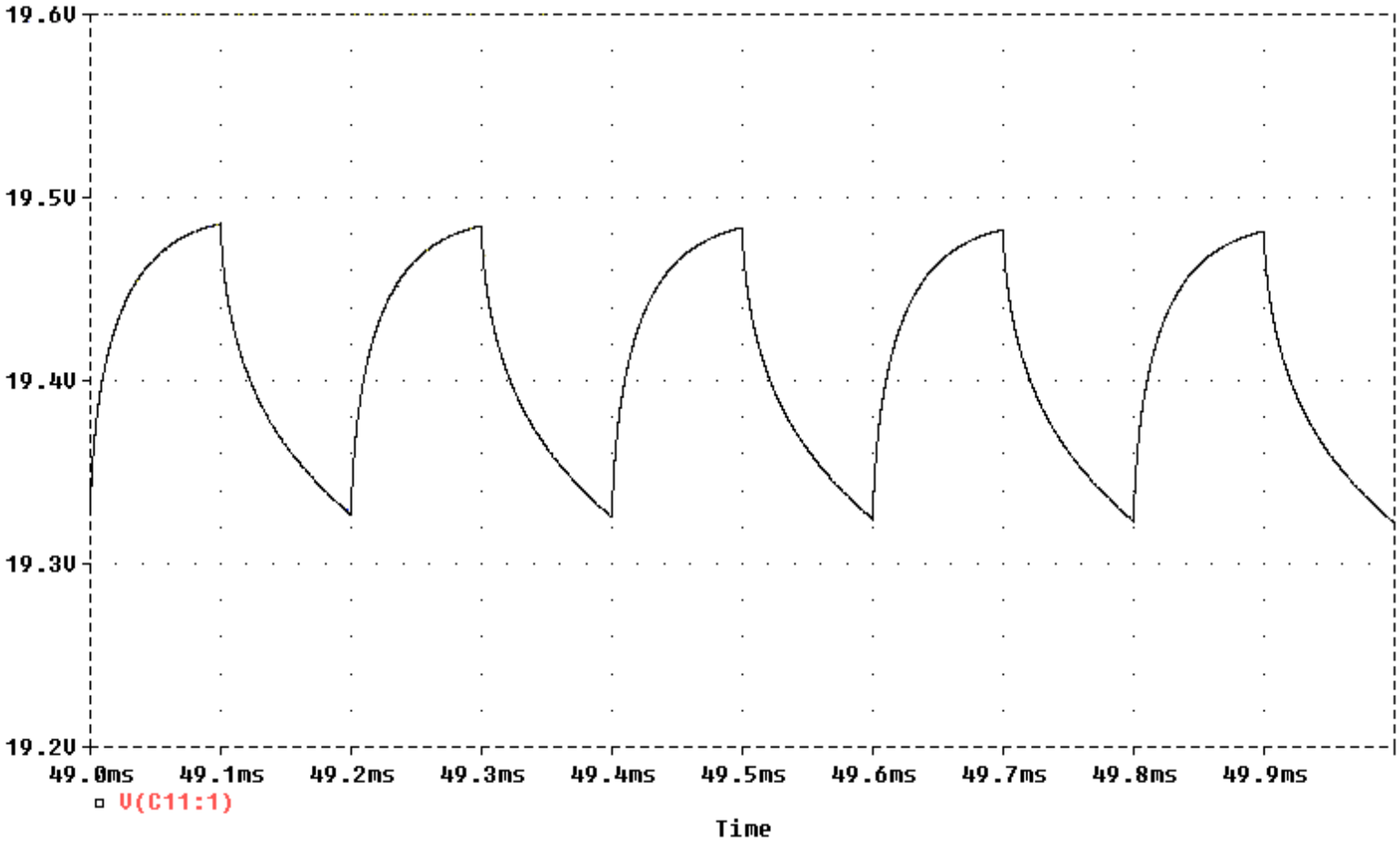

RSOURCE 50
R1 10M
C1 1U
R8 10M
C7 1U
R10 10M
C9 1U
R12 10M
C11 1U
VIN
PULSE
D1
DN4002
D2
DN4002
D5
DN4002
D6
DN4002
D7
DN4002
D8
DN4002
D9
DN4002
D10
DN4002
V(12)
OUT
R7 10M
C6 1U
R9 10M
C8 1U
R11 10M
C10 1U
R13 10M
C12 1U
RLOAD 200K

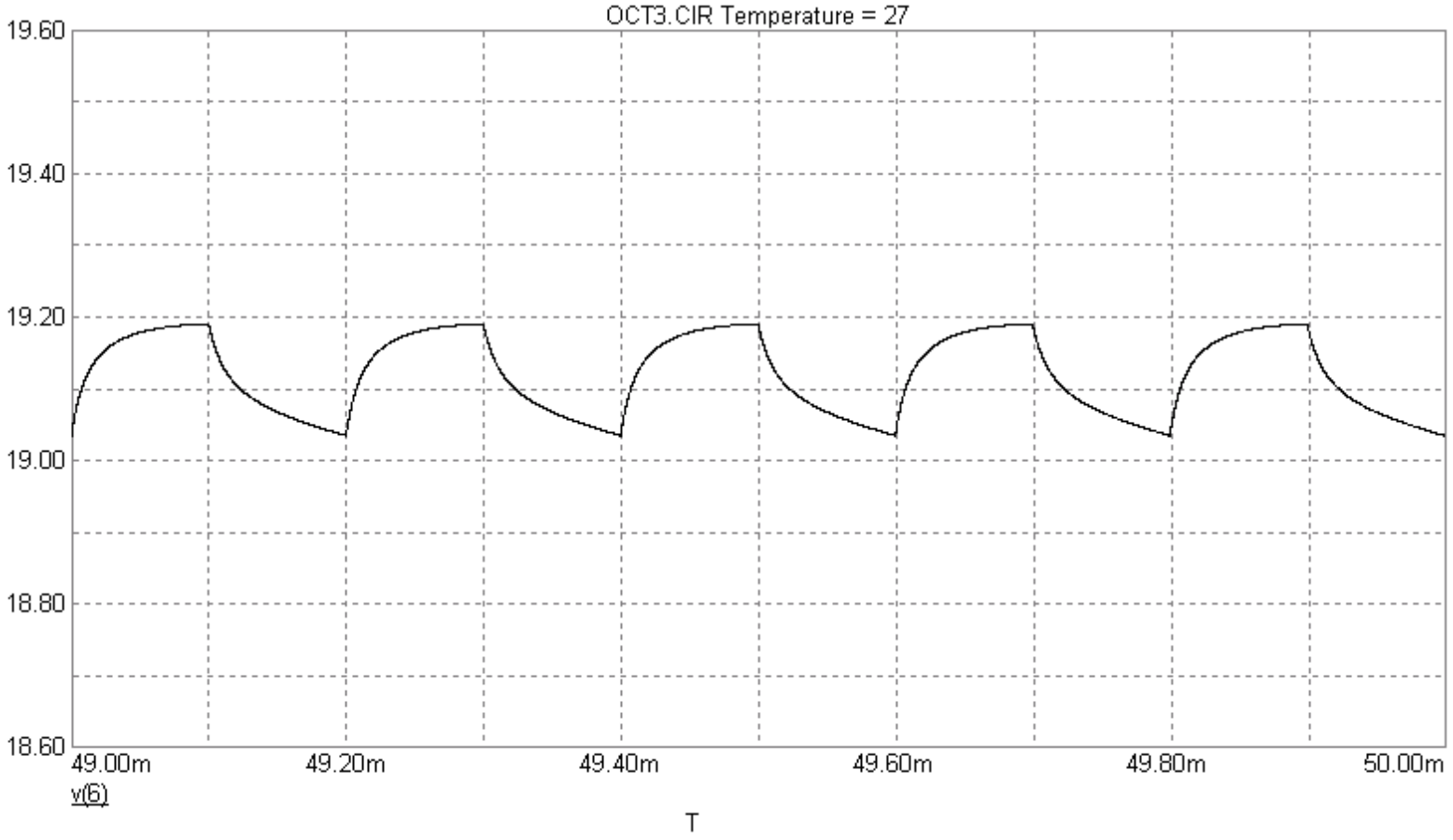

Tek Run: 500kS/s Sample Trig'd
2→
1→
Ch1 2 V Ch2 5 V M 100µs Ch1 ƒ 1.28 V
27 Jan 1998
14:29:28

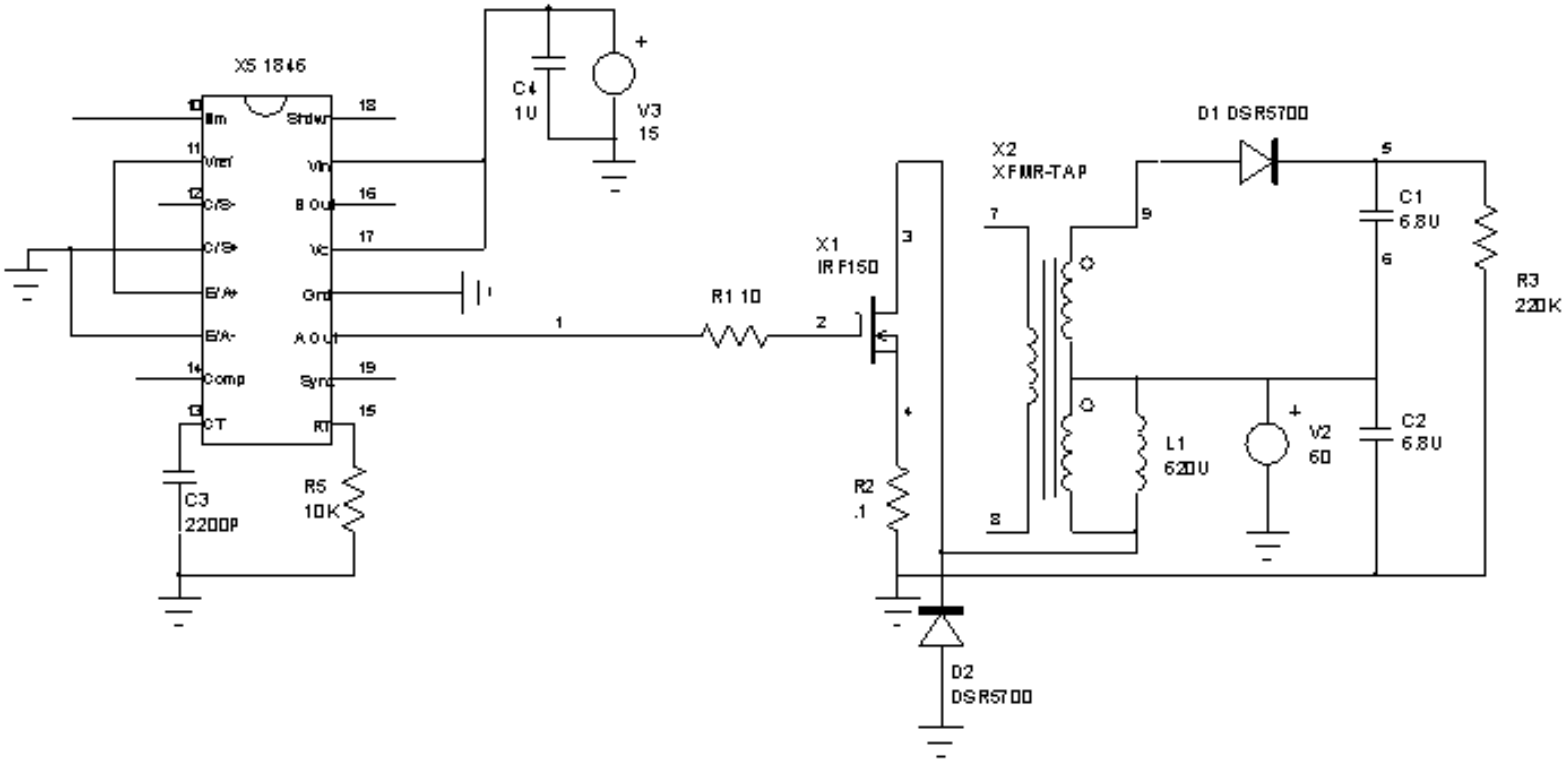

Tek Run: 500kS/s Average Trig'd
T
2→
T
Ch2 100mV∿ M 100µs Ch1 ∫ 1.28 V
27 Jan 1998
14:31:43

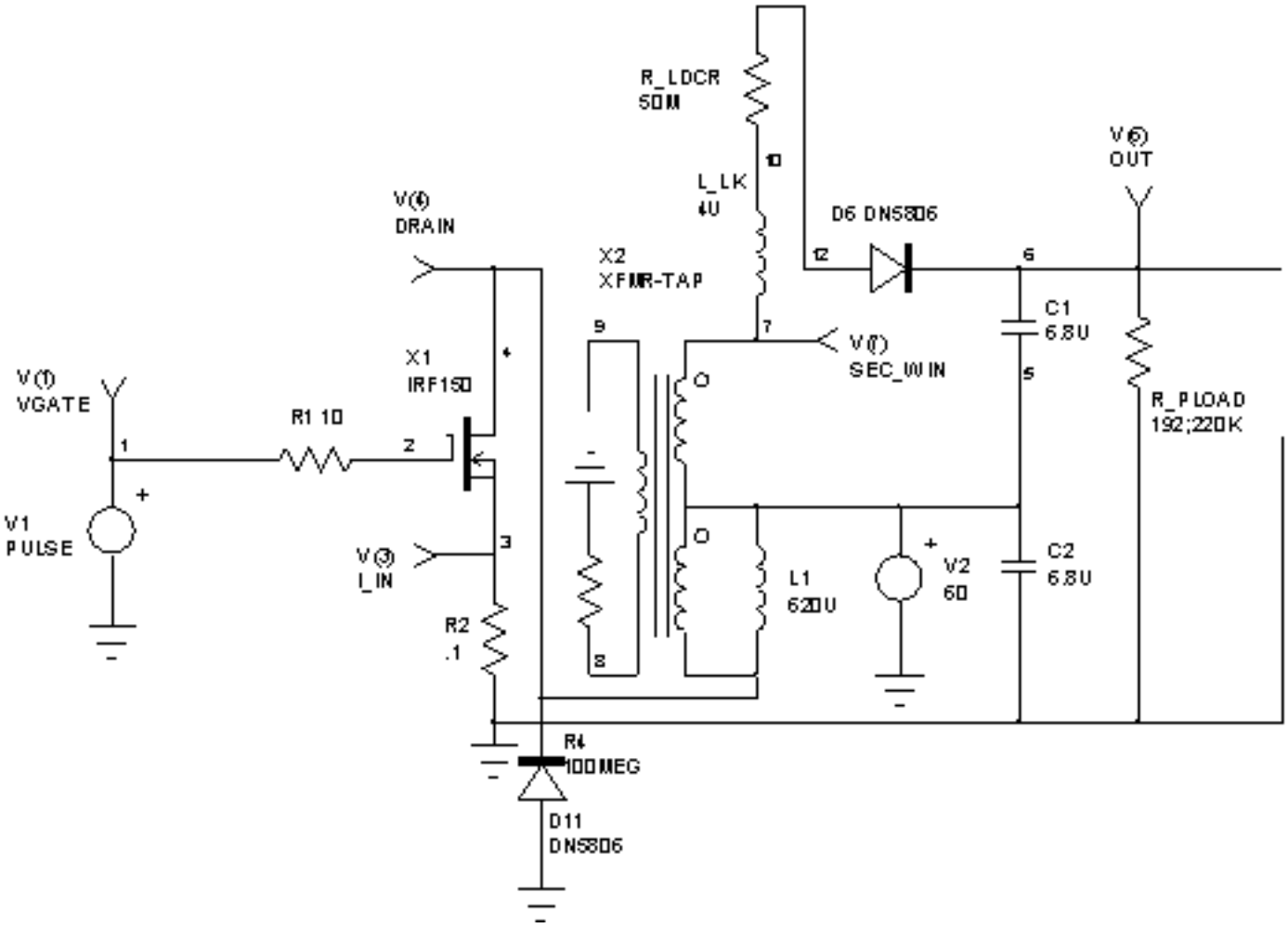

20.00
10.000
0
-10.000
-20.00
OUT in Volts
14.00
10.000
6.000
2.000
-2.000
IN in Volts
2
1
49.10M
49.30M
49.50M
49.70M
49.90M
TIME in Secs

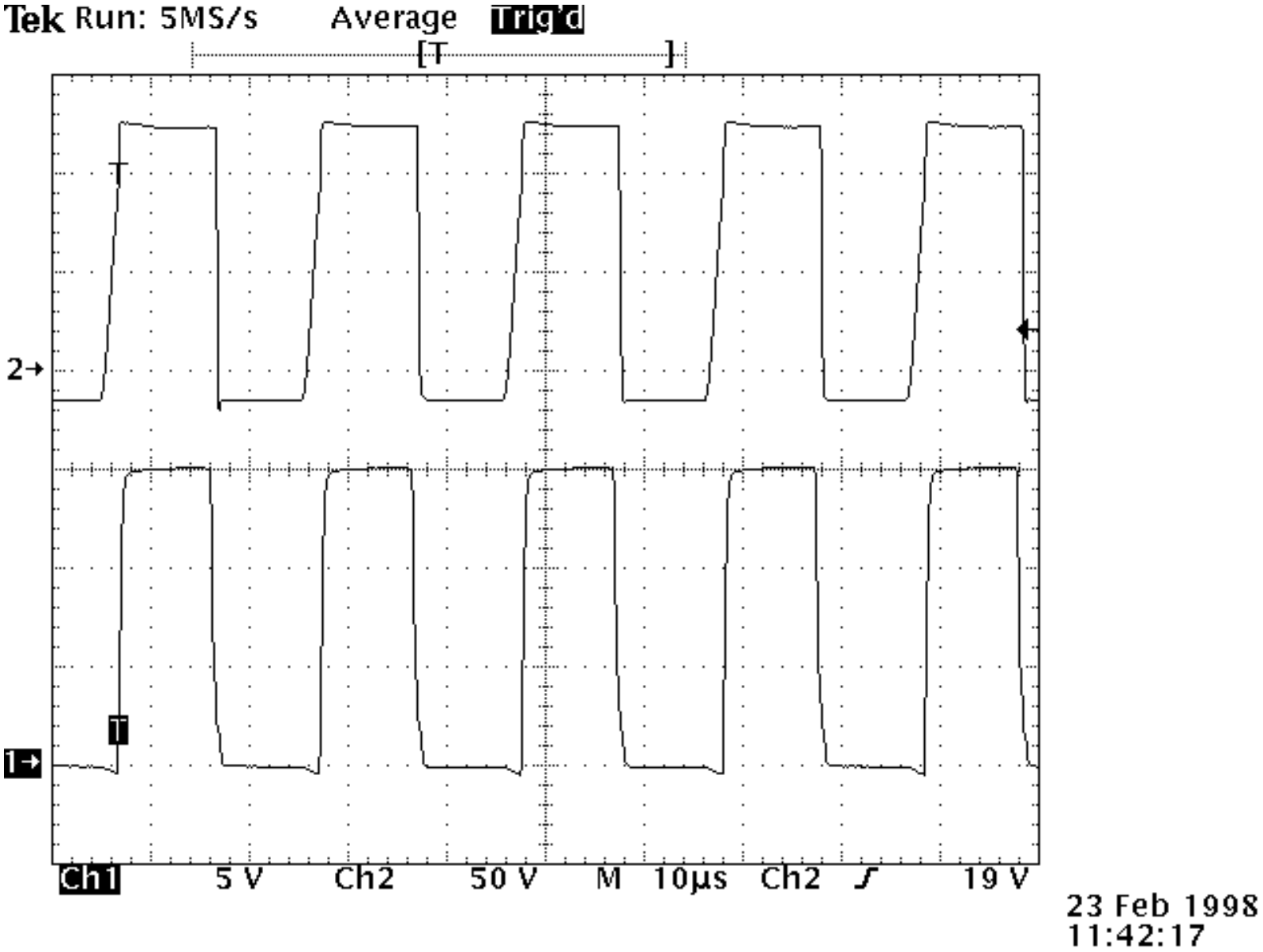

19.46
19.26
19.06
18.86
18.66
OUT in Volts
49.10M
49.30M
49.50M
49.70M
49.90M
TIME in Secs
2

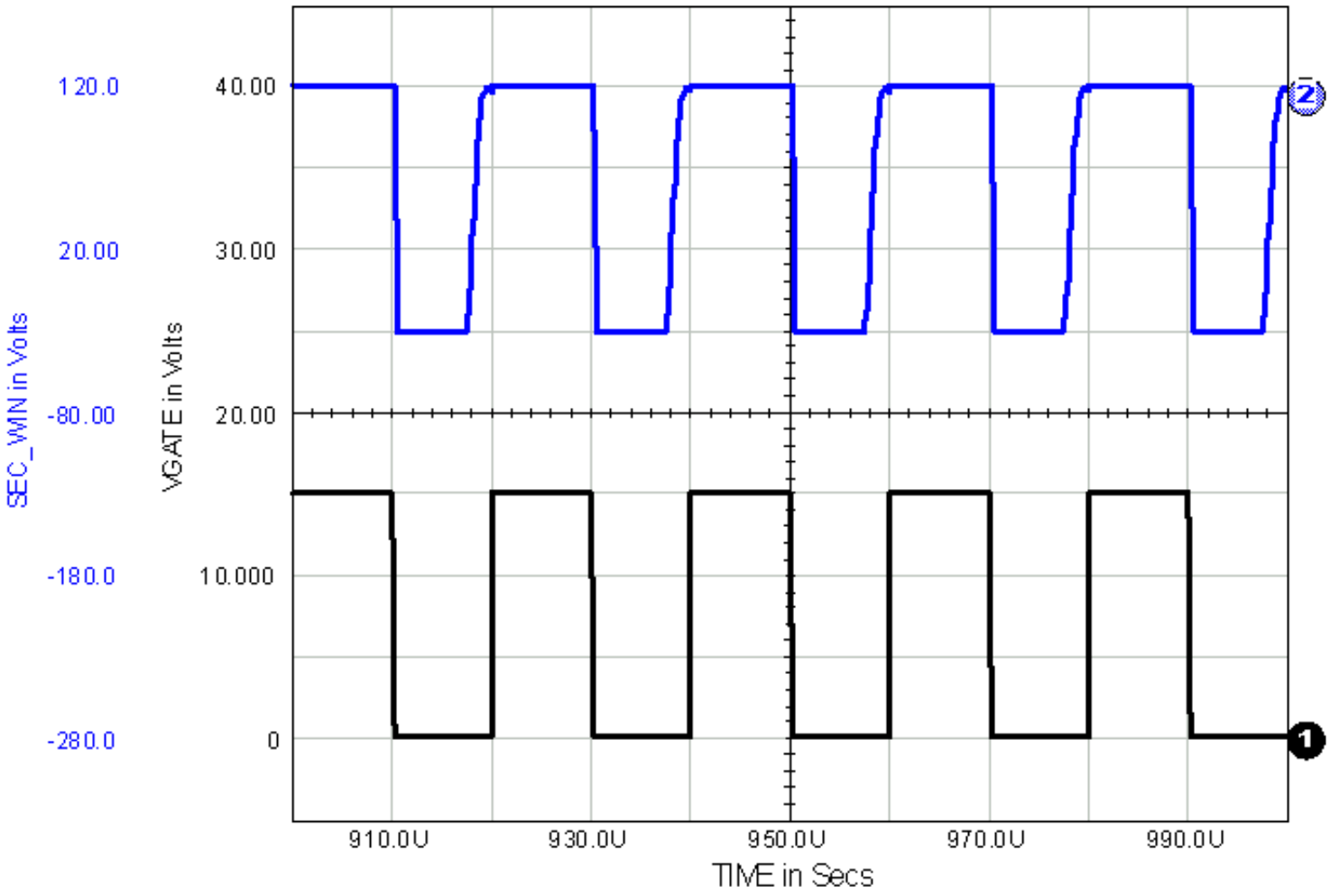

19.6V
19.5V
19.4V
19.3V
19.2V
49.0ms
49.1ms
49.2ms
49.3ms
49.4ms
49.5ms
49.6ms
49.7ms
49.8ms
49.9ms
V(C11:1)
Time

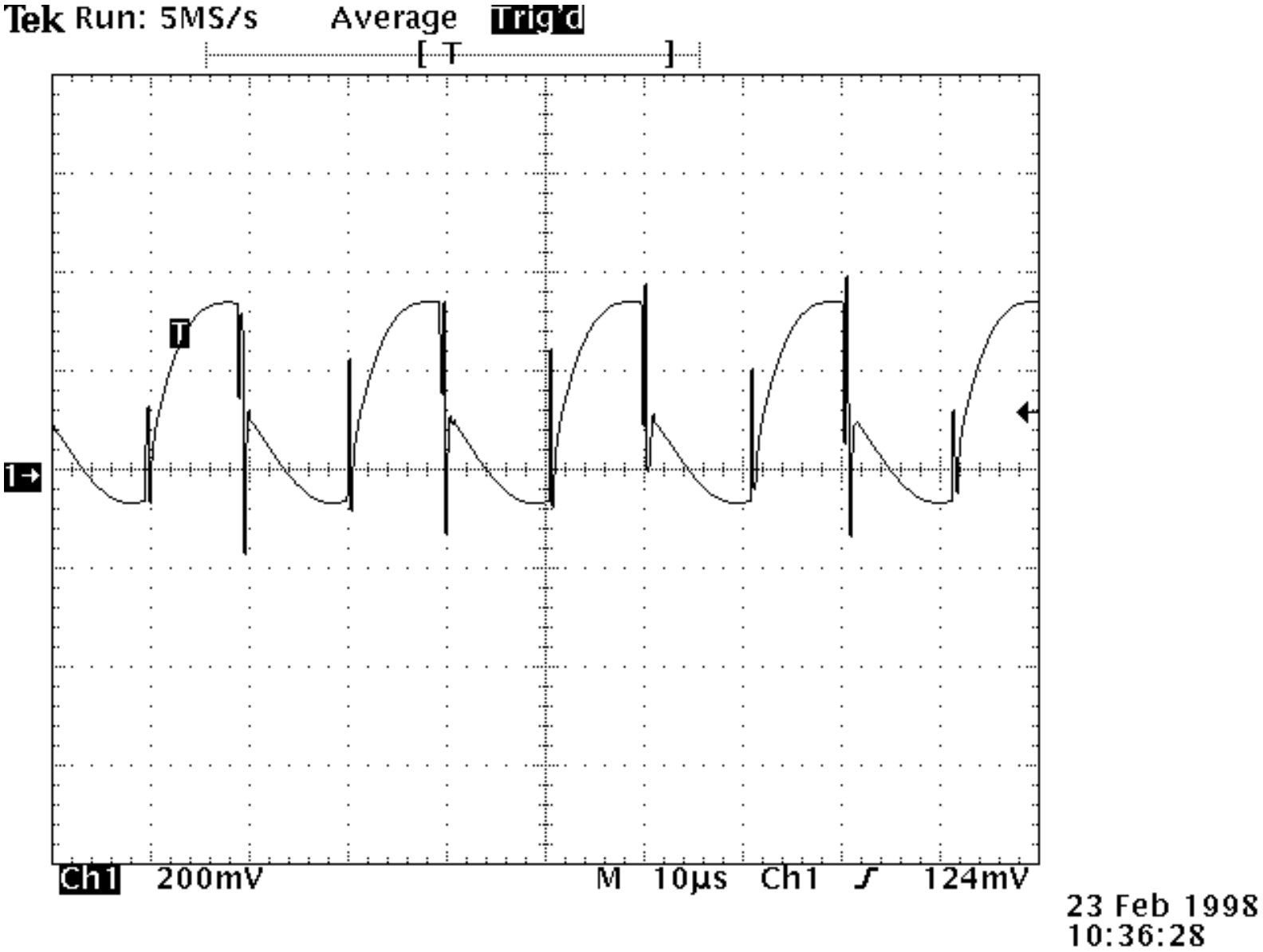

OCT3.CIR Temperature = 27
19.60
19.40
19.20
19.00
18.80
18.60
49.00m
49.20m
49.40m
49.60m
49.80m
50.00m
v(6)
T

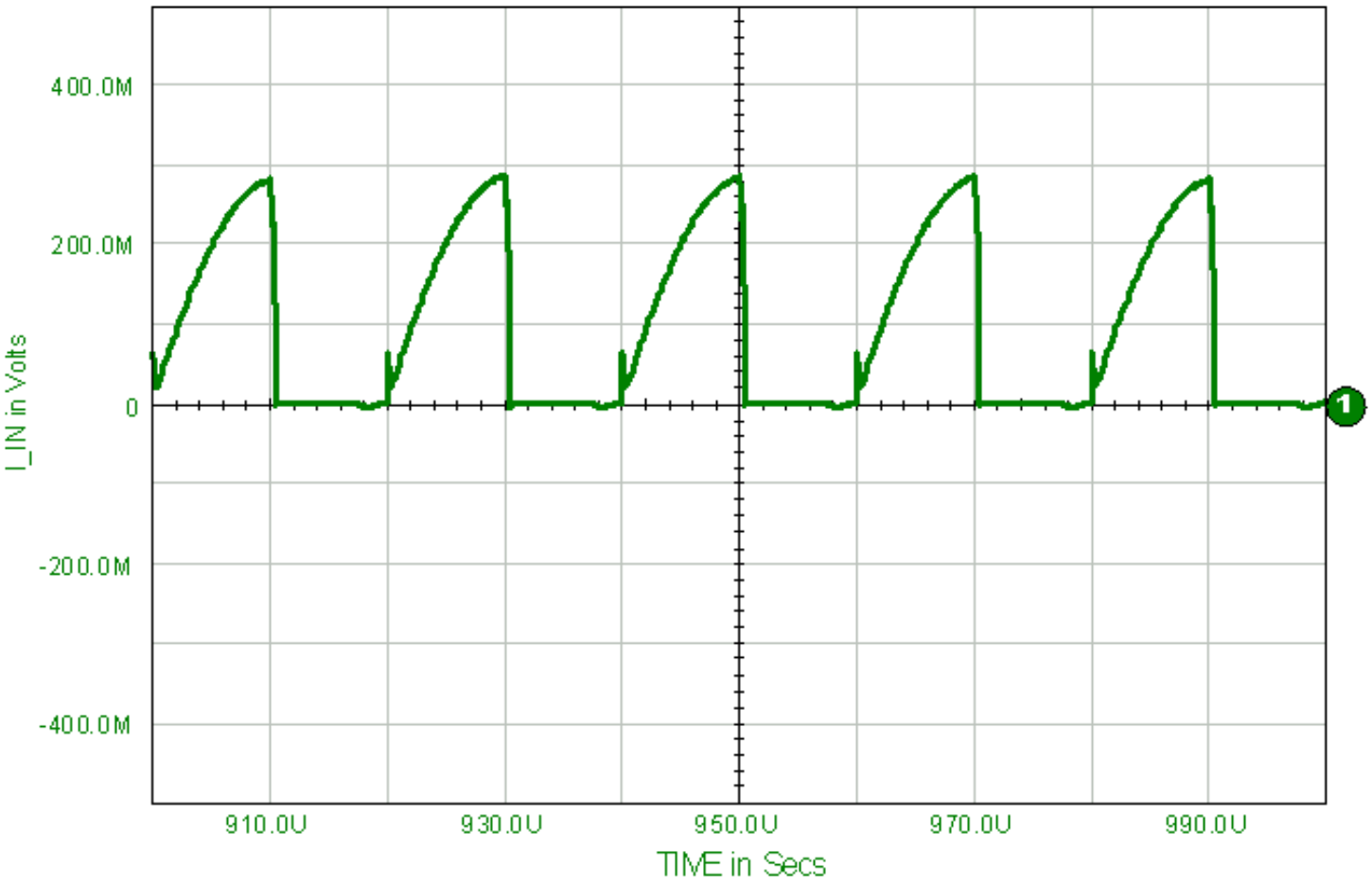

XS 1846
Ilim
Vref
C/S-
C/S+
E/A+
E/A-
Comp
CT
Shdwn
Vin
B Out
Vc
Gnd
A Out
Sync
RT
C4
1U
V3
15
R1 10
X1
IRF150
R2
.1
D1 DSR5700
X2
XFMR-TAP
C1
6.8U
R3
220K
L1
620U
V2
60
C2
6.8U
C3
2200P
R5
10K
D2
DSR5700

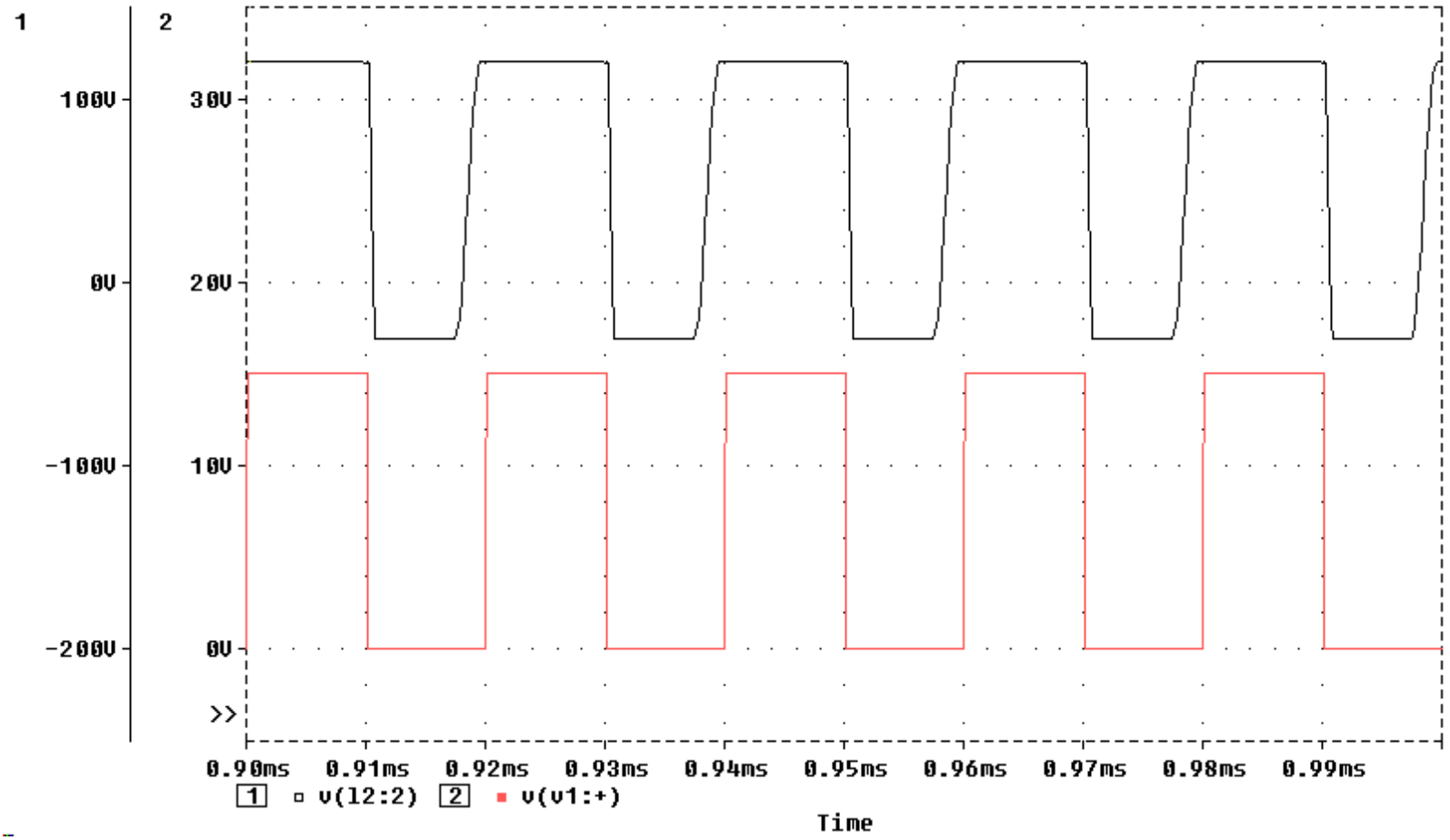

R_LDCR
50M
10
L_LK
4U
V(6)
OUT
V(4)
DRAIN
X2
XFMR-TAP
D6 DN5806
12
6
C1
6.8U
9
7
V(7)
SEC_WIN
X1
IRF150
4
V(1)
VGATE
R1 10
1
2
5
R_PLOAD
192;220K
V1
PULSE
V(3)
I_IN
3
L1
620U
V2
60
C2
6.8U
R2
.1
8
R4
100MEG
D11
DN5806

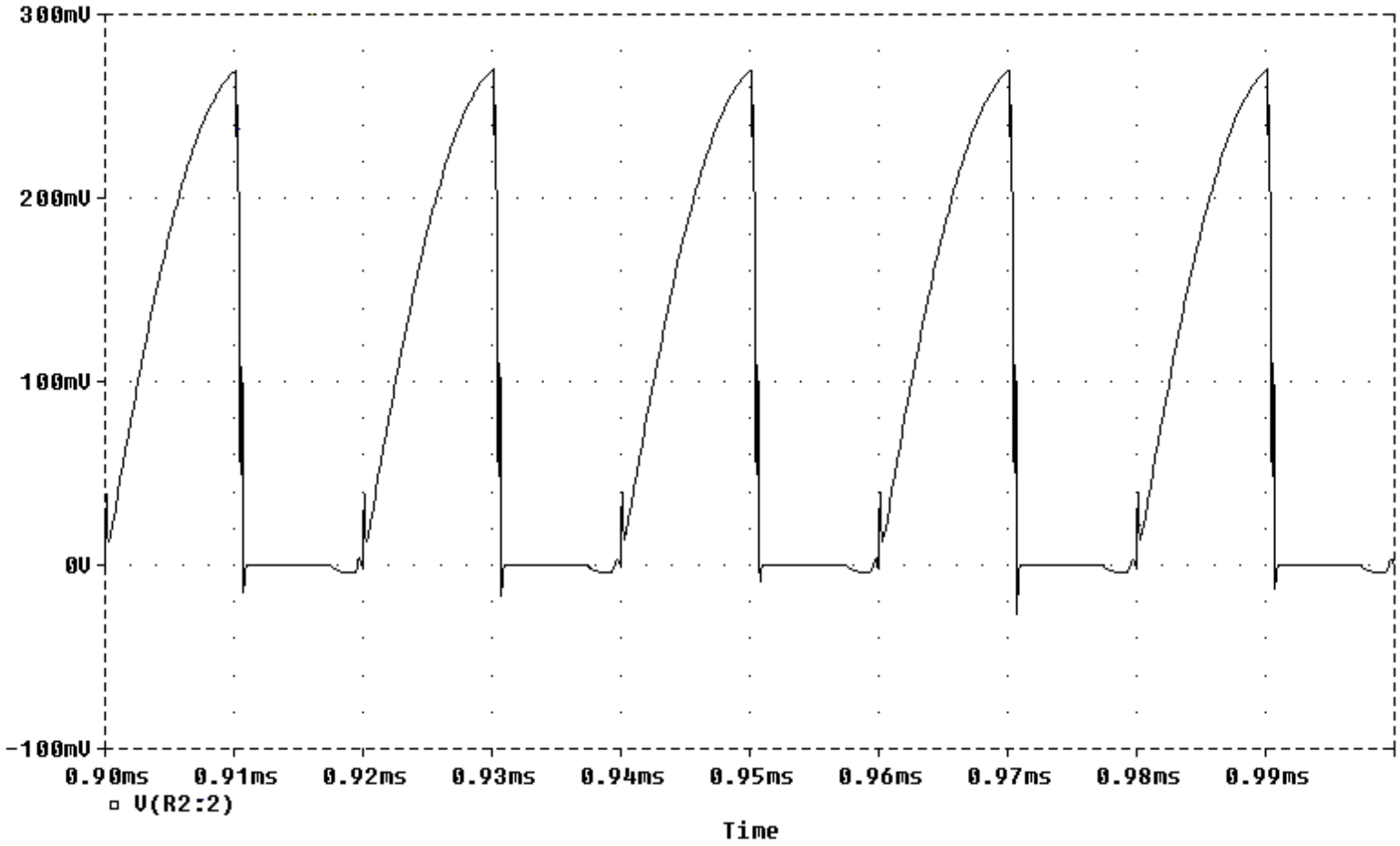

Tek Run: 5MS/s Average Trig'd
[T]
2→
1→
Ch1 5 V Ch2 50 V M 10µs Ch2 ∫ 19 V
23 Feb 1998
11:42:17

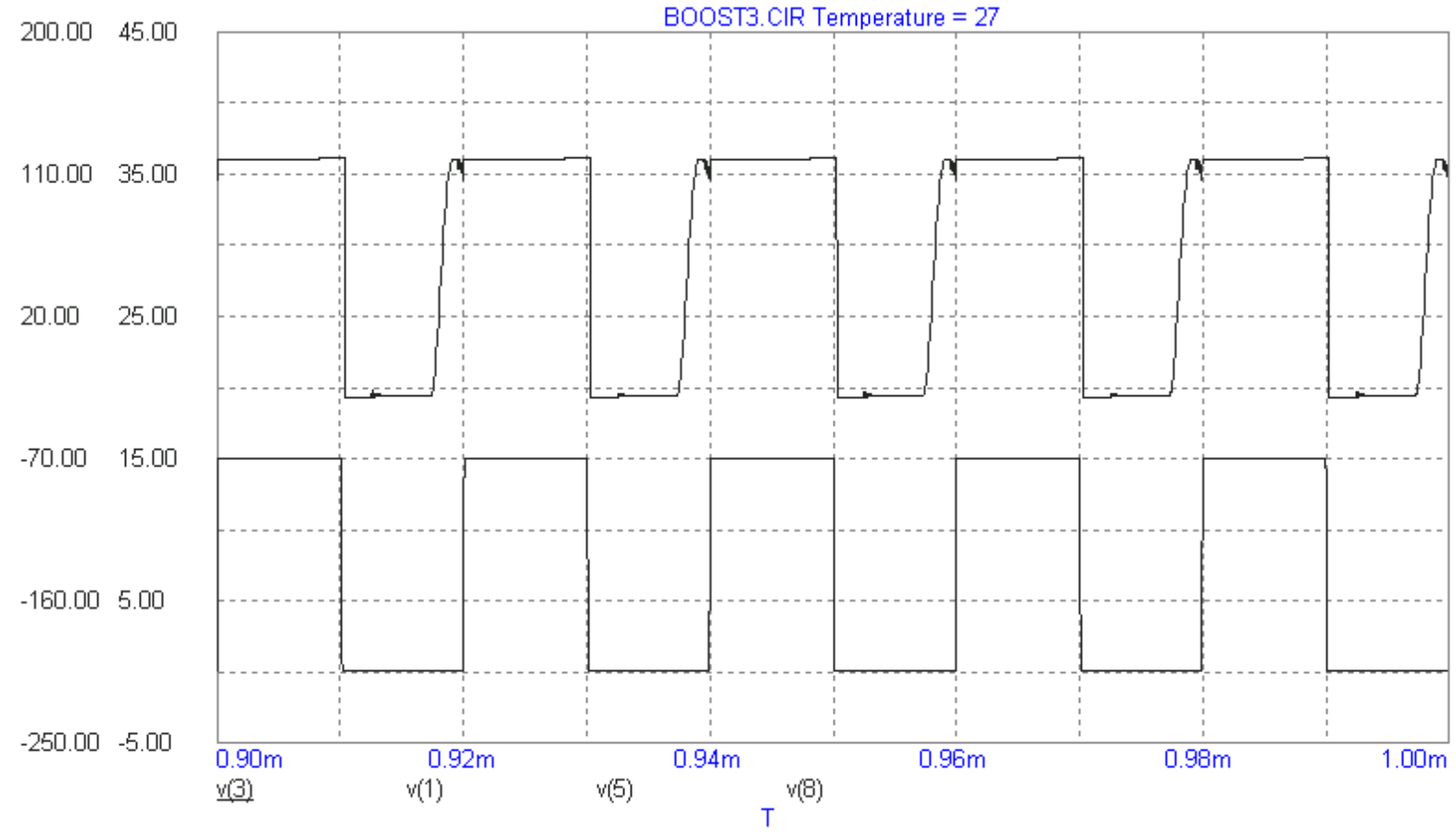

120.0
20.00
-80.00
-180.0
-280.0
SEC_WIN in Volts
40.00
30.00
20.00
10.000
0
VGATE in Volts
910.0U
930.0U
950.0U
970.0U
990.0U
TIME in Secs
2
1

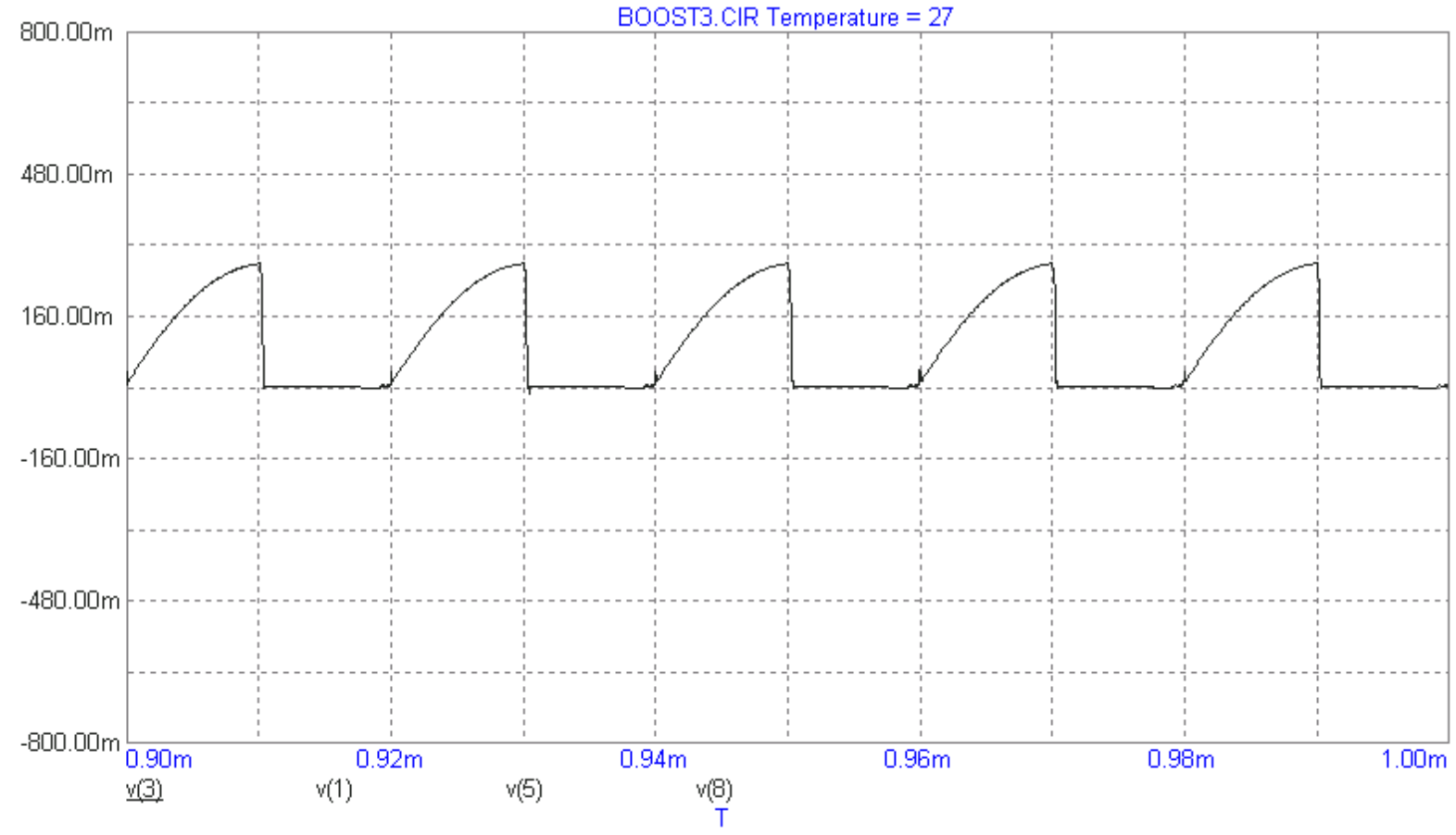

Tek Run: 5MS/s Average Trig'd
T
Ch1 200mV
M 10µs Ch1 ƒ 124mV
23 Feb 1998
10:36:28


400.0M
200.0M
0
-200.0M
-400.0M
I_IN in Volts
910.0U
930.0U
950.0U
970.0U
990.0U
TIME in Secs
1


1
2
100V
0V
-100V
-200V
30V
20V
10V
0V
>>
0.90ms
0.91ms
0.92ms
0.93ms
0.94ms
0.95ms
0.96ms
0.97ms
0.98ms
0.99ms
1 v(12:2) 2 v(v1:+)
Time


300mV
200mV
100mV
0V
-100mV
0.90ms
0.91ms
0.92ms
0.93ms
0.94ms
0.95ms
0.96ms
0.97ms
0.98ms
0.99ms
V(R2:2)
Time


BOOST3.CIR Temperature = 27
200.00
45.00
110.00
35.00
20.00
25.00
-70.00
15.00
-160.00
5.00
-250.00
-5.00
0.90m
0.92m
0.94m
0.96m
0.98m
1.00m
v(3)
v(1)
v(5)
v(8)
T


BOOST3.CIR Temperature = 27
800.00m
480.00m
160.00m
-160.00m
-480.00m
-800.00m
0.90m
0.92m
0.94m
0.96m
0.98m
1.00m
v(3)
v(1)
v(5)
v(8)
T